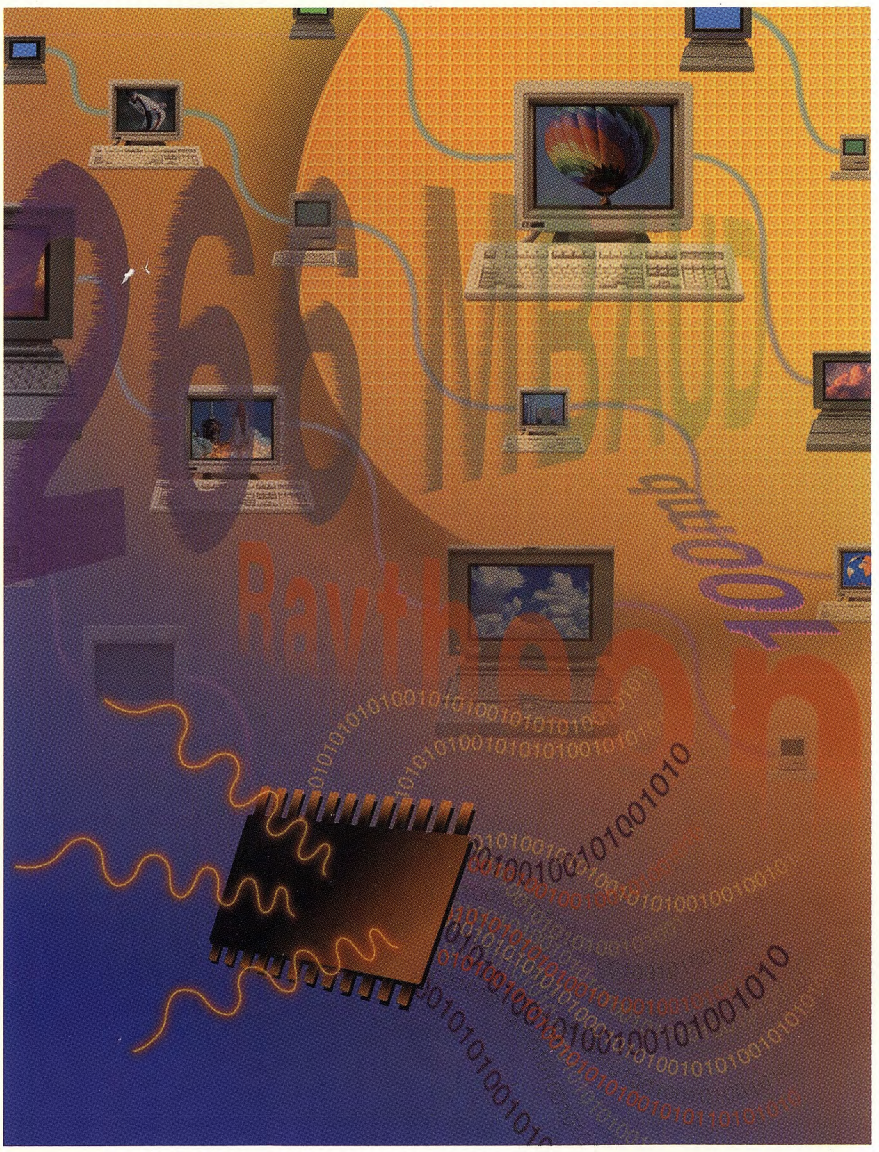
Raytheon Electronics

Semiconductor Division

1996 Data Book



1996 **Data Book**

Analog

Broadcast Video

High Speed Communications

Personal Computers

Set Top Box

PRELIMINARY INFORMATION describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact Raytheon for current information.

ADVANCED INFORMATION data sheets provide specification for products not yet complete or characterized. They provide design target information for customer planning purposes.

DISCLAIMER:

The information contained in this data book has been carefully compiled; however, it shall not by implication or otherwise become part of the terms and conditions of any subsequent sale. Raytheon's liability shall be determined solely by its standard terms and conditions of sale. No representation as to application or use or that the circuits are either licensed or free from patent infringement is intended or implied. Raytheon reserves the right to change the circuitry and any other data at any time without notice and assumes no liability for errors.

LIFE SUPPORT POLICY:

Raytheon's products are not designed for use in life support applications, wherein a failure or malfunction of the component can reasonably be expected to result in personal injury. The user of Raytheon components in life support applications assumes all risk of such use and indemnifies Raytheon Company against all damages.

Preface

Introduction

Raytheon Electronics Semiconductor Division is a business unit of Raytheon Company—a Fortune 50, $12 billion High Technology company headquartered in Lexington, Massachusetts.

For more than 30 years, the Division has been producing a variety of electronic components for commercial and defense applications. Recently, we have been manufacturing custom analog and mixed signal ASICs, as well as a number of standard products for the broadcast video market, resulting in a broad repertoire of analog and digital functional blocks. Our current product lines make extensive use of these proven, high-performance building blocks.

Our dedicated manufacturing and test facilities support our design capabilities, giving us complete control over production and test operations.

Markets

Raytheon Electronics Semiconductor Division is applying its proven expertise to the design and production of analog, digital and mixed-signal standard products for four converging, high growth semiconductor markets:

- Personal Computers
- High Speed Communications
- Broadcast Video
- Digital Set-top Boxes

Personal Computers

The personal computer market is the fastest-growing segment of the semiconductor market. The industry will ship over 60 million computers in 1995, more than doubling the global revenue in this market during the period between 1994 and 1997.

Raytheon Electronics Semiconductor Division is focused in three areas of the personal computer market:

- power conversion, supervision, and management for Pentium Class, P6, and PowerPC microprocessors.
- audio signal processing and amplification for PC motherboards and add-in cards
- video signal processing and conversion for the multimedia PC, game and home entertainment segments.

High Speed Communications

The rapidly growing communications market, particularly the networking section, is fueled by major advances in powerful computing. Several new high speed networking standards have been adopted, alleviating the bottlenecks that exist in current computer networks. The Division provides semiconductor solutions for the major high speed networking standards:

- Fibre Channel
- Fibre Distributed Data Interface (FDDI)
- Enterprise Systems Connection Architecture (ESCON)
- Fast Ethernet
- Asynchronous Transfer Mode (ATM)

We have developed a family of transceiver circuits which integrates our expertise in high speed clock multipliers, clock/data recovery, and equalizers for the twisted pair copper medium. By using state-of-the-art CMOS technology for most of the physical layer blocks, we can offer very economical solutions for high speed networking standards.

Broadcast Video

For eighteen years, Raytheon Electronics Semiconductor Division has been a major force in supplying leading-edge components t the Broadcast Television industry. Our data conversion products have provided the input and output processing systems since their start in the 1970s (a technology for which we were awarded an Emmy.)

Combined with a broad line of digital filters, mixers, encoders, decoders and special effects generators, the Division provides the creative, quality solutions that designers of advanced television broadcast systems demand.

Digital Set-Top Boxes

The key to interactivity. The Digital Set-Top Box is an emerging market. Over the next 10 years, television will change from an analog, terrestrial broadcast and dedicated cable environment, into an all-digital format conveyed via satellite, cable. Fibre, microwave, and cellular transports. The hub of this migration is the Set-Top Box, designed to accept one or several of these signal sources, provide value added processing and routing, and interface to current and future television systems, personal computers, and other "client" devices.

Raytheon Electronics Semiconductor Division is developing integrated solutions for the following emerging applications:

- Set-Top Boxes for Digital Cable and Direct Broadcast Satellite (DBS)
- Internet Cable Modems for World Wide Web access
- Interactive Television Set-Top Boxes

The Division offers IF-to-Digital converters for all the existing cable transmission formats, including QAM for digital cable and VSB for High Definition TV (HDTV). Additionally, we provide Digital Video Encoders which convert the signal to standard NTSC or PAL for display on TV sets worldwide.

Contents

Section 1 – Analog

Operational Amplifiers

Video

Voltage Regulators

DC-DC Converters

Specialty Functions

Section 2 – Broadcast Video

Digital Video Input

Digital Video Output

Video Signal Processing

A/D Converters

D/A Converters

Section 3 – High Speed Communications

Fibre Channel/ESCON

Section 4 – Personal Computers

DC-DC Converters

Sound Drivers

Video Products

Section 5 – Set Top Box

Section 6 – Packaging

Section 7 – Quality & Reliability

Section 8 – Sales Office Listings

For other Raytheon Electronics Semiconductor Division products not included in this Data Book, refer to the Alphanumeric Index for instructions on obtaining updated information.

Alphanumeric Index

The alphanumeric index lists all Raytheon Electronics Semiconductor Division integrated circuits. This list is complete and accurate at the time of printing. Information that is not in this short form catalog can be obtained using RayFax™, Raytheon Electronics Semiconductor Division's automated document distribution system. To reach RayFax™ call 415.988.2123.

Section 1 – Analog

Operational Amplifiers

Video

Voltage Regulators

DC-DC Converters

Specialty Functions

RC3403A

Ground Sensing Quad Operational Amplifier

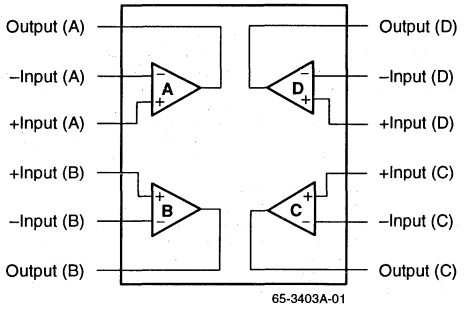
Features

- Class AB output stage – no crossover distortion
- Output voltage swings to ground in single supply operation
- High slew rate – 1.2 V/µS
- Single or split supply operation
- Wide supply operation – +2.5V to +36V or ±1.25V to ±18V
- Pin compatible with LM324 and MC3403
- Low power consumption – 0.8 mA/amplifier
- Common mode range includes ground

Description

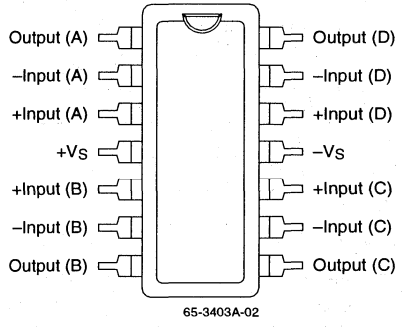
The RC3403A is a high performance ground sensing quad operational amplifier featuring improved dc specifications equal to or better than the standard 741 type general purpose op amp. The ground sensing differential input stage of this op amp provides increased slew rate compared to 741 types.

Block Diagram



65-3403A-01

Pin Assignments



65-3403A-02

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Supply Voltage			+36 or ±18	V
Input Voltage	-0.3		36	V
Differential Voltage			36	V
$P_D T_A < 50°C$			468	mW
Operating Temperature	0		70	°C
Storage Temperature	-65		150	°C
Junction Temperature			125	°C
Lead Soldering Temperature (60 seconds)			300	°C
For $T_A > 50°C$ Derate at 6.25mW/°C				

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
θ_{JA}	Thermal resistance		160		°C/W

Low Voltage Electrical Characteristics

$+V_S = +5V$, $-V_S = GND$, and $T_A = +25°C$

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage			2.0	10	mV
Input Bias Current			-150	-500	nA
Input Offset Current			30	50	nA
Supply Current	$R_L = \infty$ All Amplifiers		2.5	5.0	mA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	20	200		V/mV
Output Voltage Swing[1]	$R_L \geq 10k\Omega$	3.5			V_{p-p}
Channel Separation	$1kHz \leq F \leq 200kHz$ (Input referred)		120		dB
Power Supply Rejection Ratio		76			dB

Note:

1. Output will swing to ground.

Electrical Characteristics

$+V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage				10	mV
Input Bias Current				-800	nA
Input Offset Current				200	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			V

Electrical Characteristics $+V_S = \pm15V, T_A = +25°C$

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage			2.0	6.0[1]	mV
Input Bias Current			-150	-500	nA
Input Offset Current			30	50	nA
Input Voltage Range		0		$+V_S - 2$	V
Supply Current	$R_L = \infty$ On All Op Amps		3.0	5.0[1]	mA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	25[1]	100		V/mV
Output Voltage Swing[1]	$R_L \geq 10k\Omega$	±13	±14		V
Common Mode Rejection Ratio	DC	70	90		dB
Channel Separation	±1 kHz to 20kHz		120		dB
Output Source Current	$+V_{IN} = 1V, -V_{IN} = 0V$	20	40		mA
Output Sink Current		10	20		mA
Unity Gain Bandwidth			1.0		MHz
Slew Rate	$A_V = 1, -10 \leq V_{IN} < +10$		1.2[1]		V/µS
Distortion (Crossover)	$F = 20kHz, V_{OUT} = 10V_{p-p}$		1.0		%
Power Bandwidth	$V_{OUT} = 10V_{p-p}$		40		kHz
Power Supply Rejection Ratio		80	94		dB

Note:
1. Significantly improved performance.

Electrical Characteristics Comparison – RC3403A, MC3403, LM324

MAX Ratings	RC3403A			MC3403			LM324			Unit
Supply Voltage	+36 or ±18			+36 or ±18			+32 or ±16			V
Differential Input Voltage	36			36			32			V
Input Voltage	36			36			32			V
Electrical Characteristics	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Test Conditions		±15			±15			+5.0		V
Input Offset Voltage		2.0	6.0		2.0	8.0		2.0	7.0	mV
Input Offset Current		±30	±50		±30	±50		±5.0	±50	nA
Input Bias Current		150	500		200	500		45	500	nA
Input Voltage Range	0		$+V_S-2$	0		$+V_S-2$	0		$+V_S-1.5$	V
Supply Current		3.0	5.0		2.8	7.0		0.8	2.0	mA
Large Signal Voltage Gain	25	100		20	200			100		V/mV
Output Voltage Swing	±13	±14		±10	±13		0		$+V_S-1.5$	V
Common Mode Rejection Ratio	70	90		70	90			85		dB
Power Supply Rejection Ratio	80	94		76	90			85		dB
Unity Gain Bandwidth		1.0			1.0			1.0		MHz
Slew Rate		1.2			0.6			0.4		V/µS
Output Sink Current	10	20						20		mA
Output Source Current	20	40					20	40		mA
Channel Separation		120			120			120		dB
Distortion (Crossover)		1.0			1.0					%

Typical Performance Characteristics

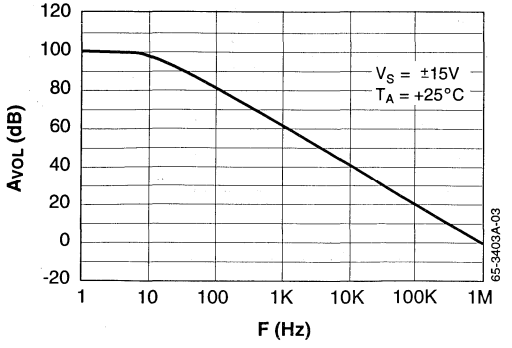


Figure 1. Open Loop Gain vs. Frequency

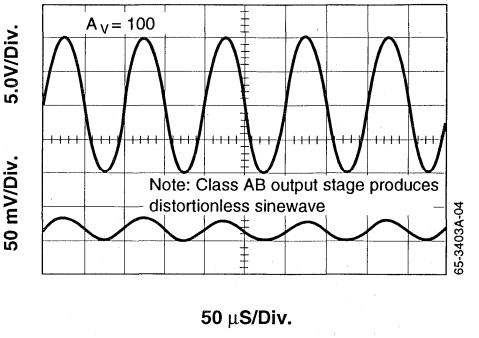


Figure 2. Sinewave Response

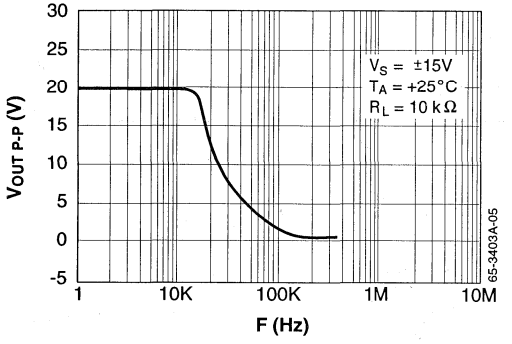


Figure 3. Output Voltage vs. Frequency

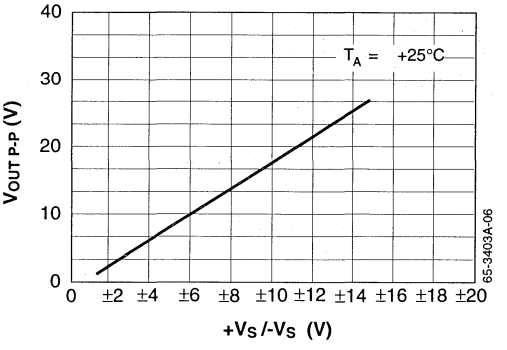


Figure 4. Output Swing vs Supply Voltage

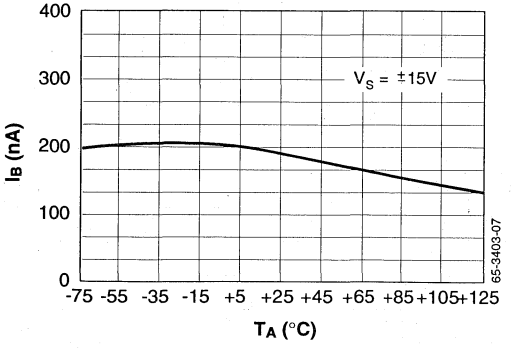


Figure 5. Input Bias Current vs. Temperature

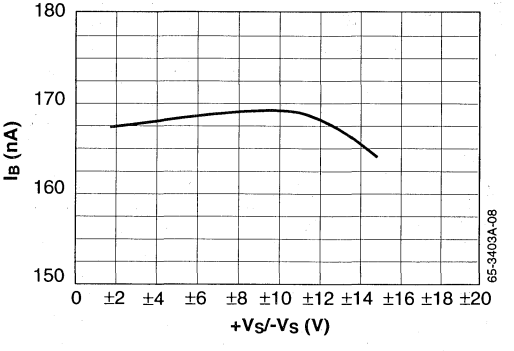


Figure 6. Input Bias Current vs. Supply Voltage

Typical Applications

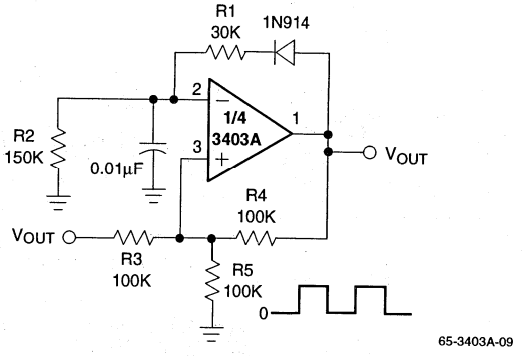


Figure 7. Pulse Generator

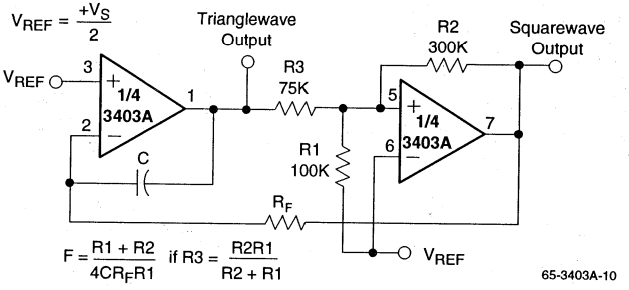


Figure 8. Function Generator

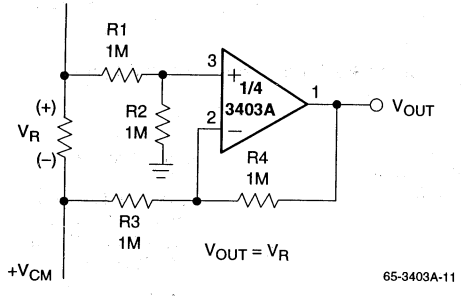


Figure 9. Ground Referencing a Differential Input Signal

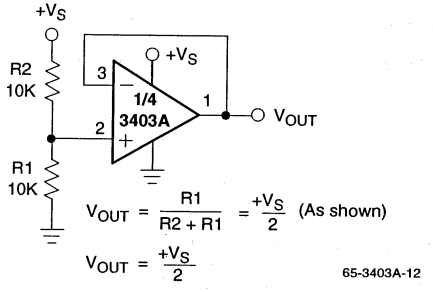


Figure 10. Voltage Reference

Typical Applications (continued)

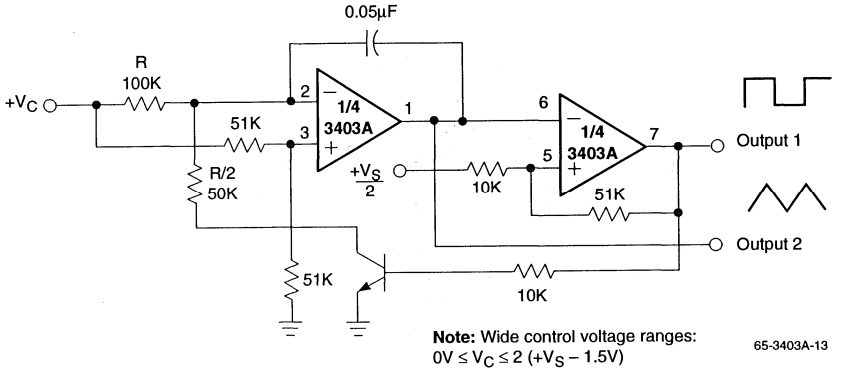


Figure 11. Voltage Controlled Oscillator

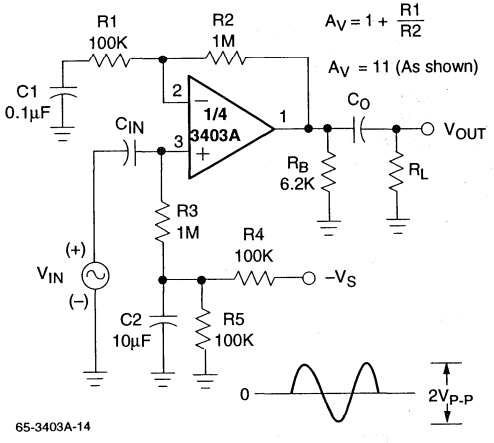


Figure 12. AC Coupled Non-Inverting Amplifier

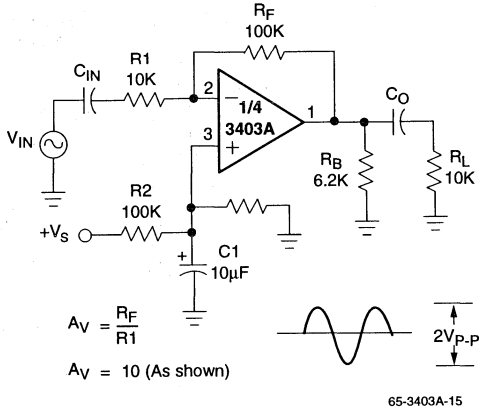
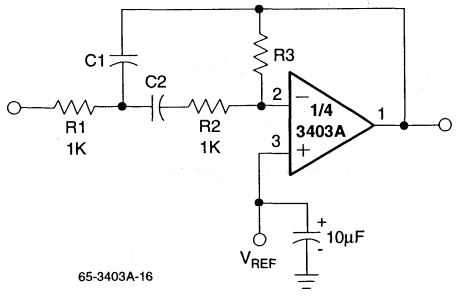


Figure 13. AC Coupled Inverting Amplifier



FO ΔCenter Frequency
BW ΔBandwidth
R in kΩ
C in µF

$Q = \frac{F_O}{BW} < 10$

$C1 = C2 = \frac{Q}{3}$

R1 = R2 = 1
R3 = $9Q^2 - 1$

} Use scaling factors in these expressions.

Design Example:

Given: Q = 5, F_O = 1 kHz
Let R1 = R2 = 10 k Ω
Then R3 = $9 (5)^2 - 10$
R3 = 215 k Ω

$C = \frac{5}{3} = 1.6$ nF

If source impedance is high or varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

Figure 14. Multiple Feedback Bandpass FIlter

Typical Applications (continued)

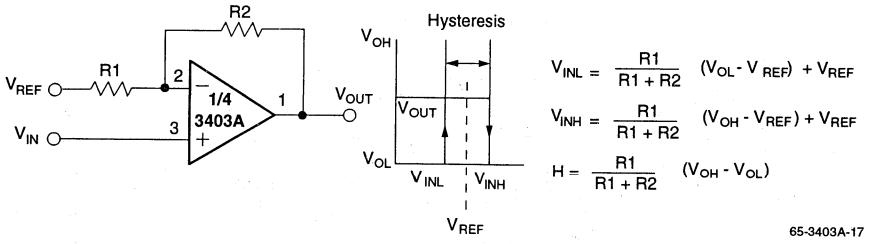


Figure 15. Comparator with Hysteresis

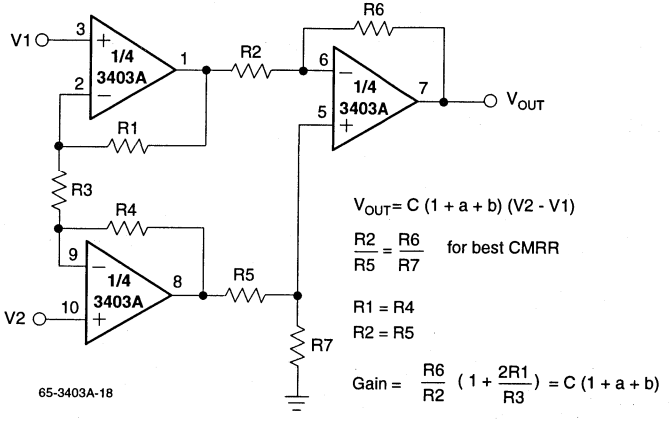


Figure 16. High Impedance Differential Amplifier

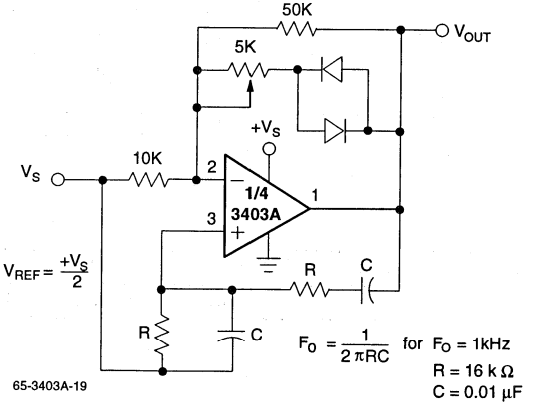
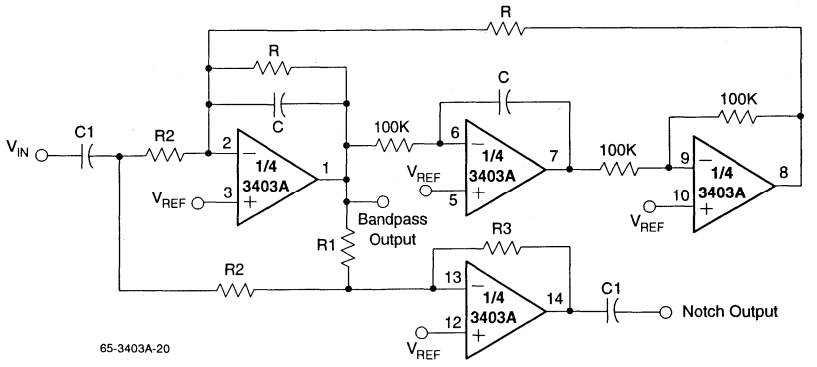


Figure 17. Wein Bridge Oscillator

Typical Applications (continued)



$Q = \frac{F_O}{BW}$

Where:

T_{BP} = Center Frequency Gain

T_N = Bandpass Notch Gain

$F_O = \frac{1}{2\pi RC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N R2$

$C1 = 10C$

Example:

F_O = 1000 Hz

BW = 100 Hz

T_{BP} = 1

T_N = 1

R = 160 kΩ

R1 = 1.6 MΩ

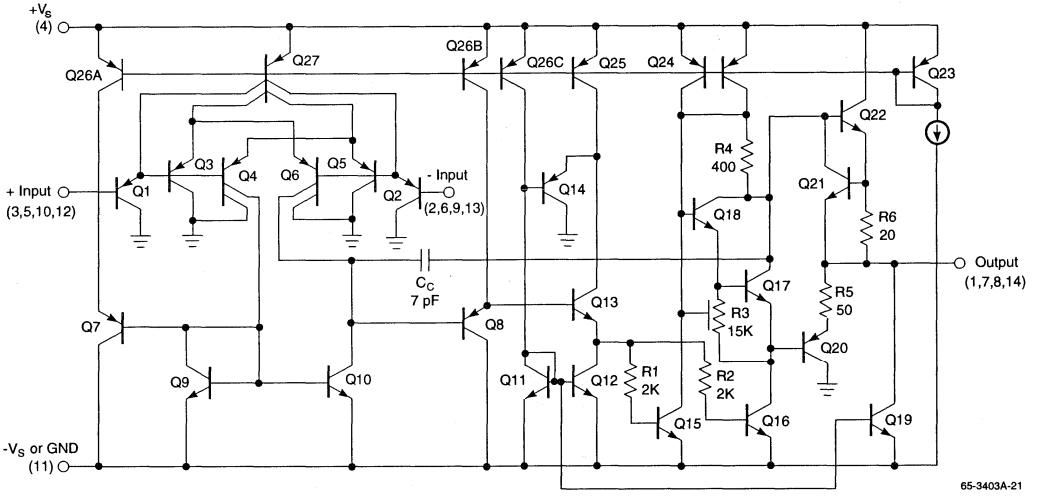
R2 = 1.6 MΩ

R3 = 1.6 MΩ

C = 0.001μF

Figure 18. Bi-Quad Filter

Simplified Schematic Diagram (1/4 Shown)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC3403AN	0° to 70°C	Commercial	14 Pin Plastic DIP	RC3403AN

RC4136

General Performance Quad 741 Operational Amplifier

Features

- Unity gain bandwidth – 3 MHz
- Short circuit protection
- No frequency compensation required
- No latch-up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

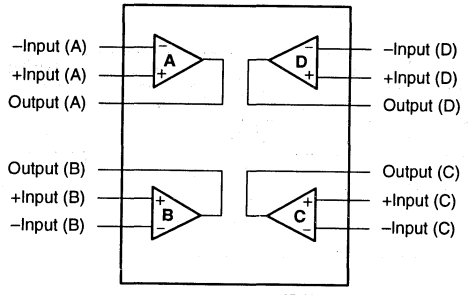
Description

The RC4136 is made up of four 741 type independent high gain operational amplifiers internally compensated and constructed on a single silicon chip using the planar epitaxial process.

This amplifier meets or exceeds all specifications for 741 type amplifiers. Excellent channel separation allows the use of the RC4136 quad amplifier in all 741 operational amplifier applications providing the highest possible packaging density.

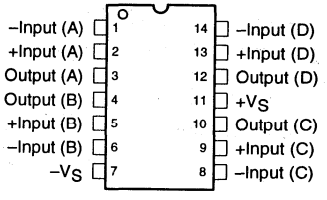
The specially designed low noise input transistors allow the RC4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners.

Block Diagram



65-4136-01

Pin Assignments



65-4136-02

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage	RC4136			±18	V
	RM4136			±22	V
Input Voltage[2]				±30	V
Differential Input Voltage				30	V
Output Short Circuit Duration[3]		Indefinite			
P_D T_A < 50°C	SOIC			300	mW
	PDIP			468	mW
	CerDIP			1042	mW
Operating Temperature	RC4136	0		70	°C
	RM4136	-55		125	°C
Storage Temperature		-65		150	°C
Junction Temperature	SOIC, PDIP			125	°C
	CerDIP			175	°C
Lead Soldering Temperature (60 seconds)	DIP			300	°C
	SOIC			260	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground, typically 45 mA.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance			60		°C/W
θ_{JA}	Thermal resistance	SOIC		200		°C/W
		PDIP		160		°C/W
		CerDIP		120		°C/W
For T_A > 50°C Derate at		SOIC		5.0		mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C, unless otherwise noted)

Parameters	Test Conditions	RM4136			RC4136			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		0.5	5.0		0.5	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	5.0		0.3	5.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		
Input Voltage Range		±12	±14		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	100		76	100		dB
Power Consumption	$R_L = \infty$, All Outputs		210	340		210	340	mW
Transient Response								
Rise Time	V_{IN} = 20mV, R_L = 2kΩ		0.13			0.13		µS
Overshoot	$C_L \leq 100pF$		5.0			5.0		%
Unity Gain Bandwidth			3.0			3.0		MHz
Slew Rate	$R_L \geq 2k\Omega$		1.5			1.0		V/µS
Channel Separation	F = 1.0kHz, R_S =1kΩ		90			90		dB

Electrical Characteristics

(RM = -55°C ≤ T_A ≤ = 125°, RC = 0°C ≤ T_A ≤ = 70°, V_S = ± 15V)

Parameters	Test Conditions	RM4136			RC4136			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Power Consumption			240	400		240	400	mW

Electrical Characteristics Comparison

(V_S = ±15V and T_A +25°C unless otherwise noted)

Parameter	RC4136 (Typ.)	RC741 (Typ.)	LM324 (Typ.)	Units
Input Offset Voltage	0.5	2.0	2.0	mV
Input Offset Current	5.0	10	5.0	nA
Input Bias Current	40	80	55	nA
Input Resistance	5.0	2.0		MΩ
Large Signal Voltage Gain (R_L = 2kΩ)	300	200	100	V/mV
Output Voltage Swing (R_L= 2kΩ)	±13V	±13V	I+V_S – 1.2VI to –V_S	V
Input Voltage Range	±14V	±13V	I+V_S – 1.5VI to –V_S	V
Common Mode Rejection Ratio	100	90	85	dB
Power Supply Rejection Ratio	100	90	100	dB
Transient Response				
Rise Time	0.13	0.3		µS
Overshoot	5.0	5.0		%
Unity Gain Bandwidth	3.0	0.8	0.8	MHz
Slew Rate	1.0	0.5	0.5	V/µS
Input Noise Voltage Density (F= 1kHz)	10	22.5		nV/√Hz
Short Circuit Current	±45	±25		mA

Typical Performance Characteristics

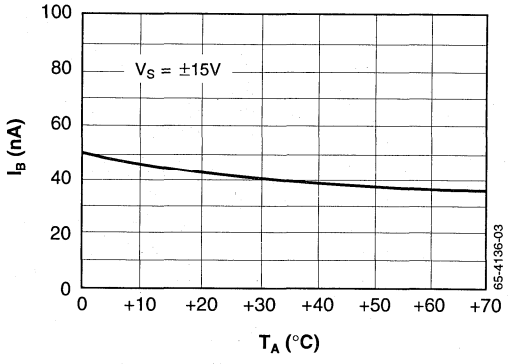


Figure 1. Input Bias Current vs. Temperature

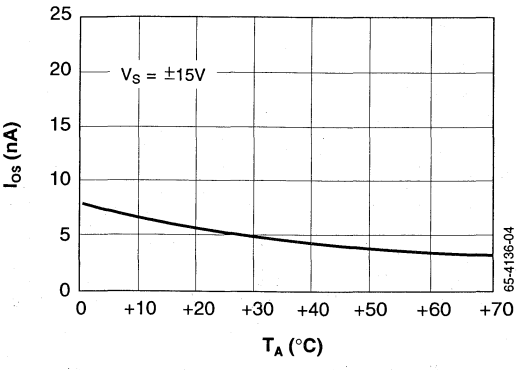


Figure 2. Input Offset Current vs. Temperature

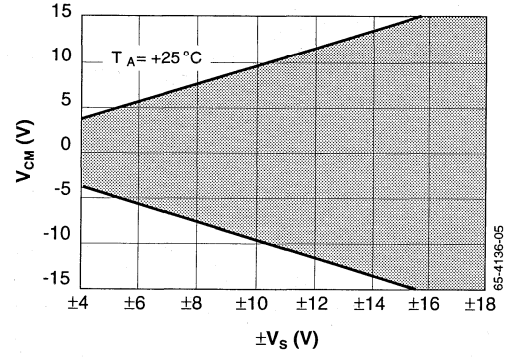


Figure 3. Input Common Mode Voltage Range vs. Supply Voltage

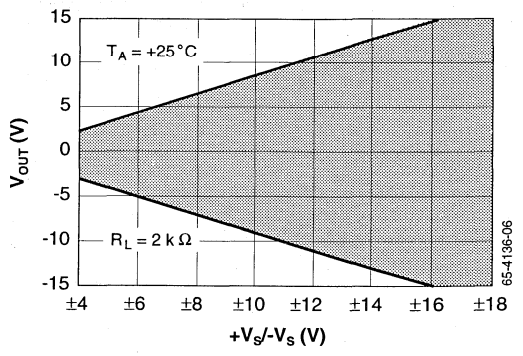


Figure 4. Output Voltage vs. Supply Voltage

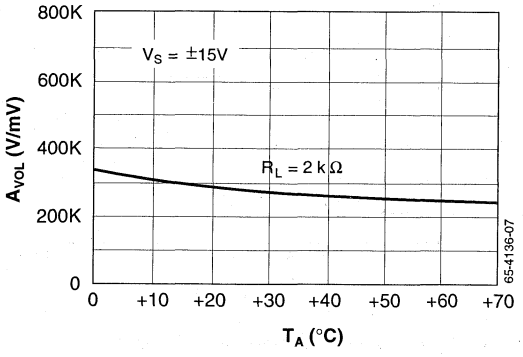


Figure 5. Open Loop Gain vs. Temperature

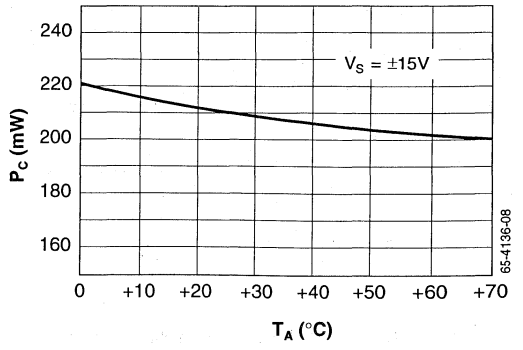


Figure 6. Power Consumption vs. Temperature

Typical Performance Characteristics (continued)

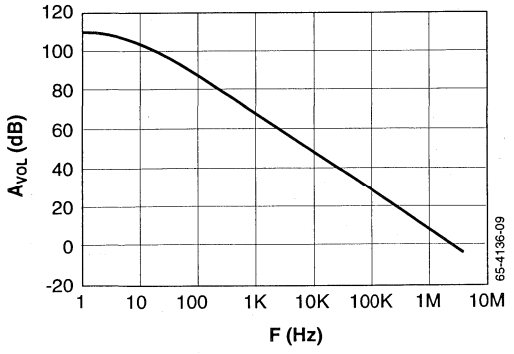


Figure 7. Open Loop Gain vs. Frequency

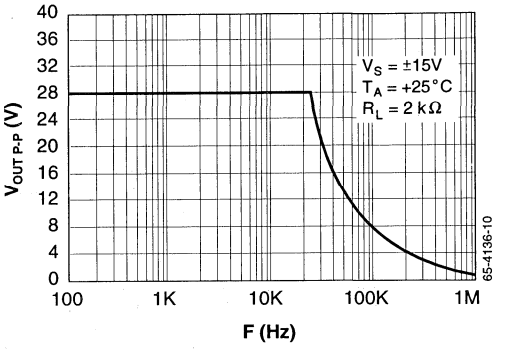


Figure 8. Output Voltage Swing vs. Frequency

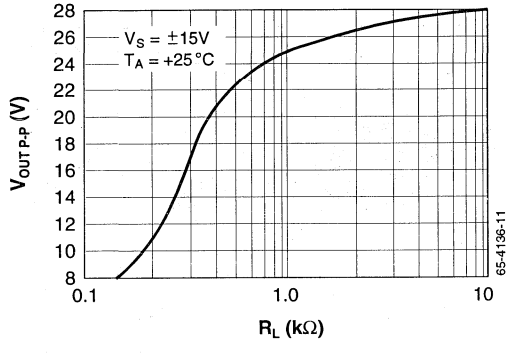


Figure 9. Output Voltage Swing vs. Load Resistance

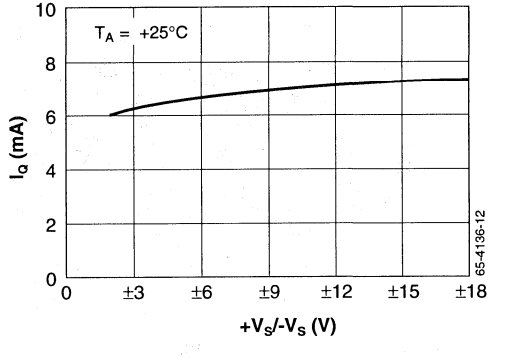


Figure 10. Quiescent Current vs. Supply Voltage

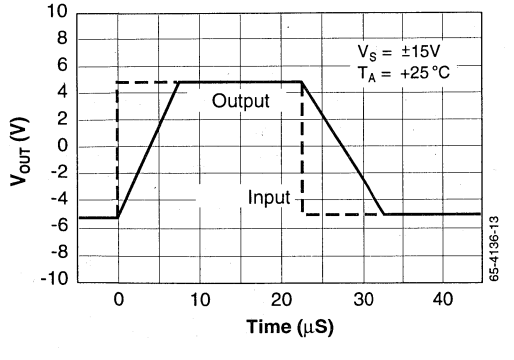


Figure 11. Follower Large Signal Pulse Response

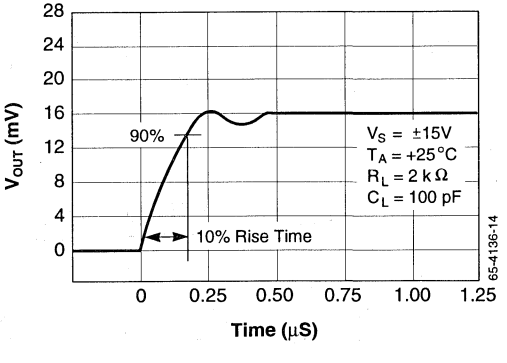


Figure 12. Transient Response Output Voltage vs. Time

Typical Performance Characteristics (continued)

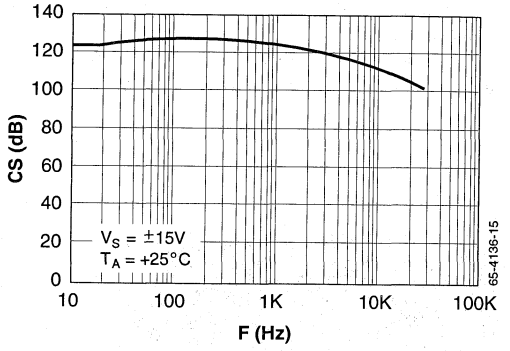


Figure 13. Channel Separation vs. Frequency

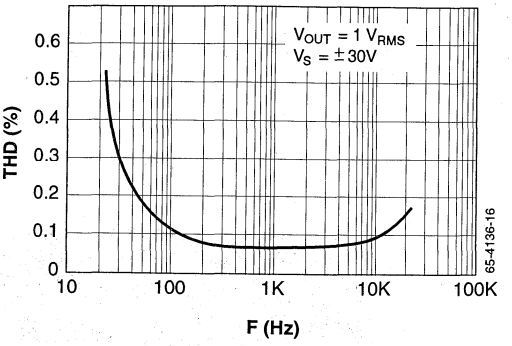


Figure 14. Total Harmonic Distortion vs. Frequency

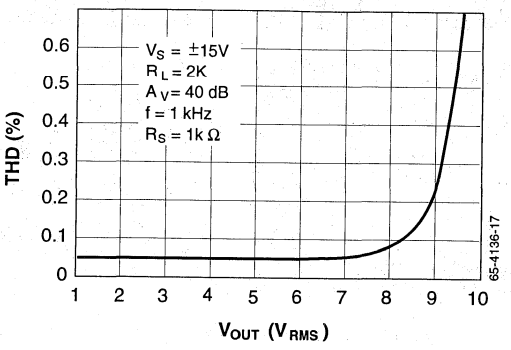


Figure 15. Total Harmonic Distortion vs. Output Voltage

RC4136 Versus LM324

Although the LM324 is an excellent device for single-supply applications where ground sensing is important, it is a poor substitute for four 741s in split supply circuits. The simplified input circuit of the RC4136 exhibits much lower noise than that of the LM324 and exhibits no crossover distortion as compared with the LM324 (see Figure 16). The LM324 shows significant crossover distortion and pulse delay in attempting to handle a large signal input pulse.

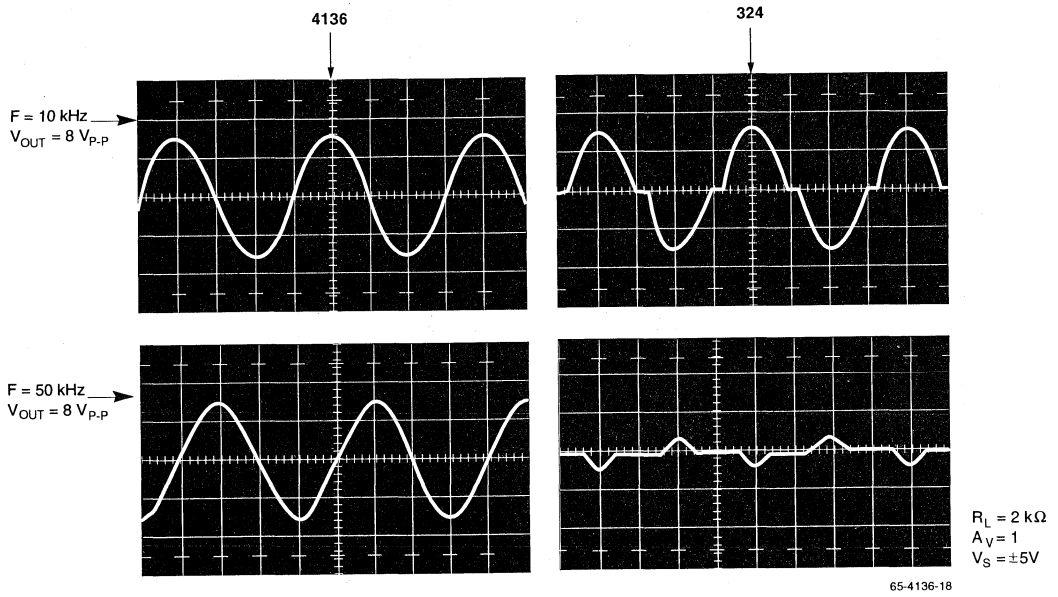


Figure 16. Comparative Crossover Distortion

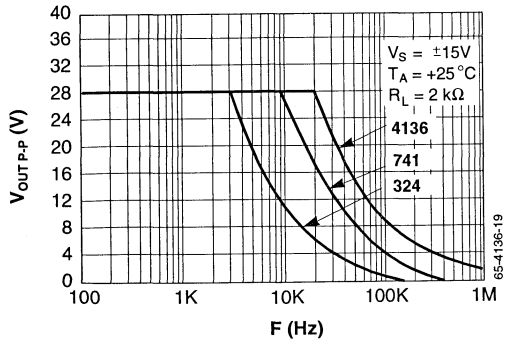


Figure 17. Output Voltage Swing vs. Frequency

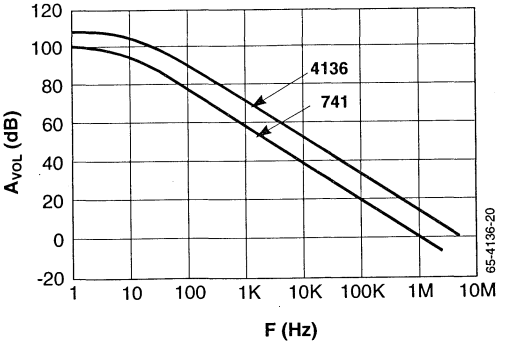


Figure 18. Open Loop Gain vs. Frequency

RC4136 Versus LM324 (continued)

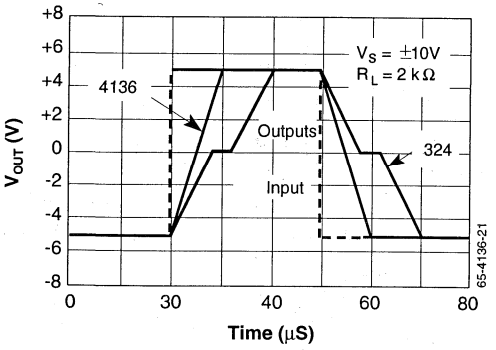


Figure 19. Follower Large Signal Pulse Response Output Voltage vs. Time

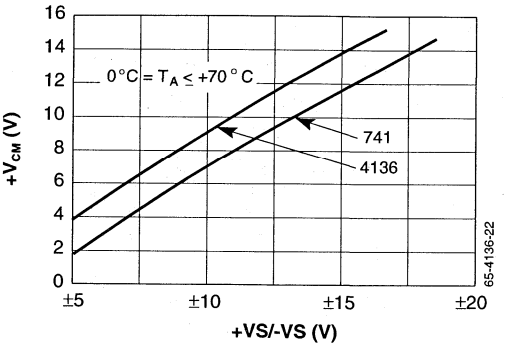


Figure 20. Input Common Mode Voltage Range vs. Supply Voltage

Typical Applications

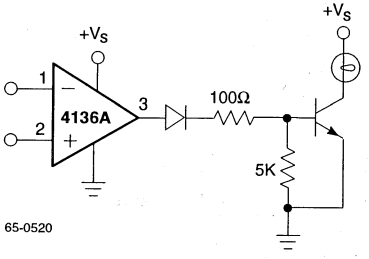


Figure 21. Lamp Driver

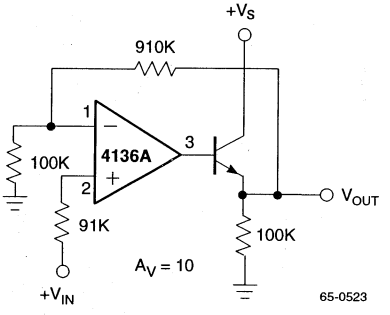


Figure 22. Power Amplifier

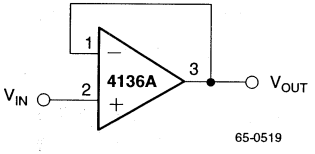


Figure 23. Voltage Follower

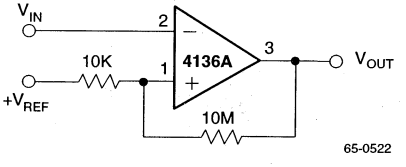


Figure 24. Comparator with Hysteresis

Typical Applications (continued)

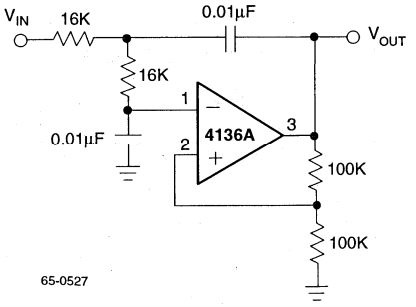


Figure 25. DC Coupled 1kHz Lowpass Active Filter

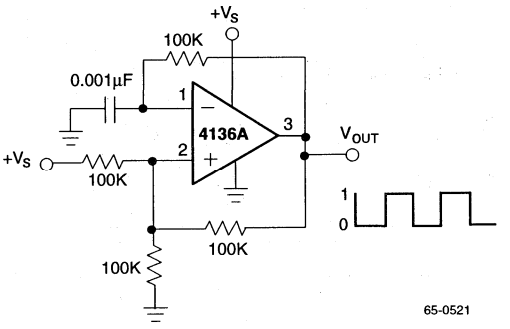


Figure 26. Squarewave Oscillator

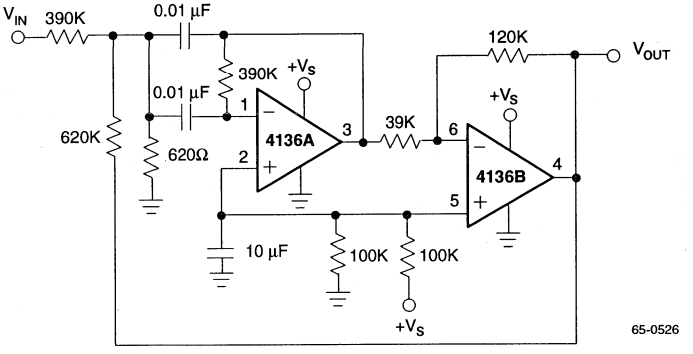


Figure 27. 1kHz Bandpass Active Filter

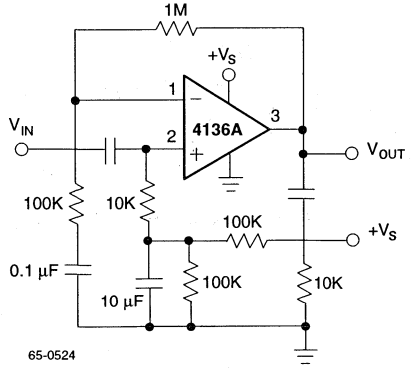


Figure 28. AC Coupled Non-Inverting Amplifier

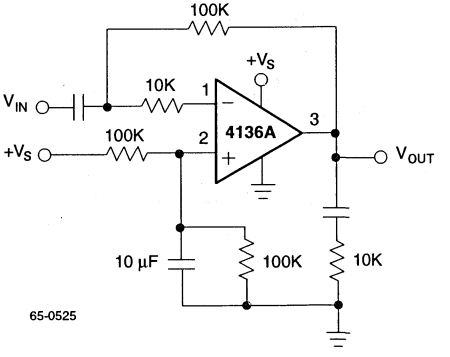
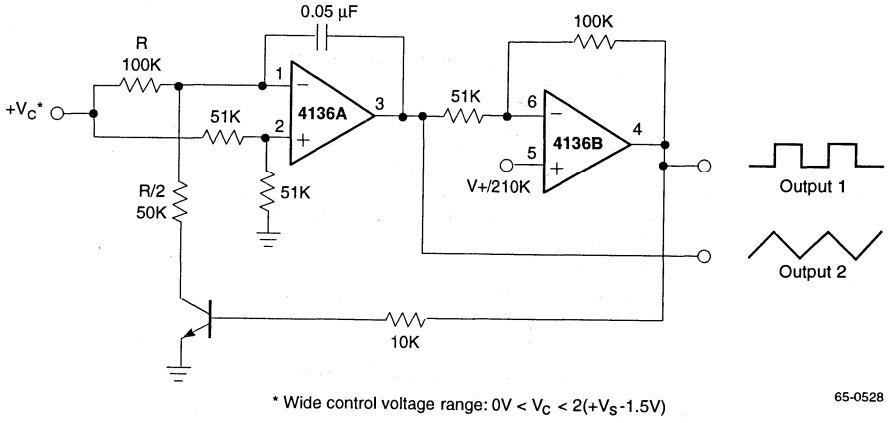


Figure 29. AC Coupled Inverting Amplifier

Typical Applications (continued)



* Wide control voltage range: $0V < V_C < 2(+V_S - 1.5V)$

Figure 30. Voltage Control Oscillator (VCO)

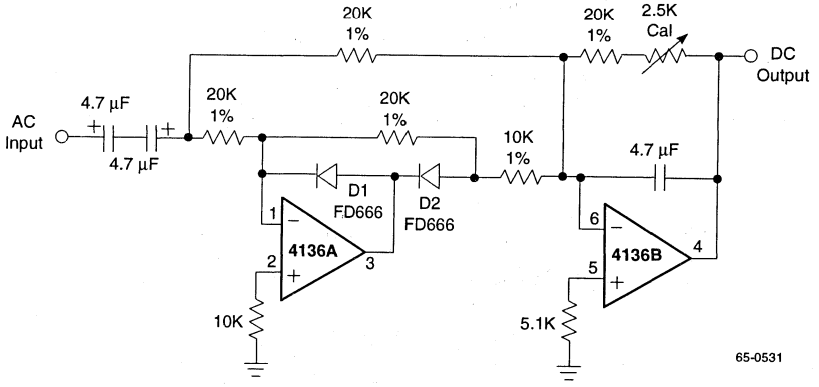


Figure 31. Full-Wave Rectifier and Averaging Filter

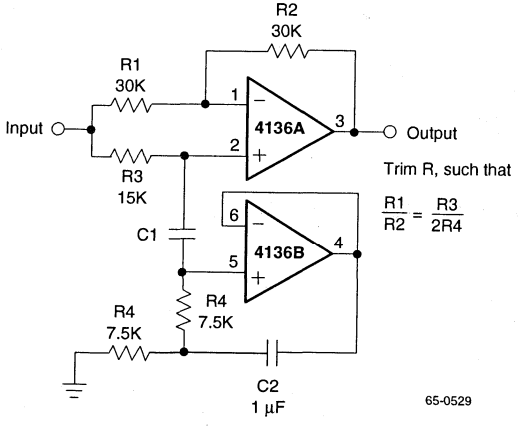


Figure 32. Notch Filter Using the RC4136 as a Gyrator

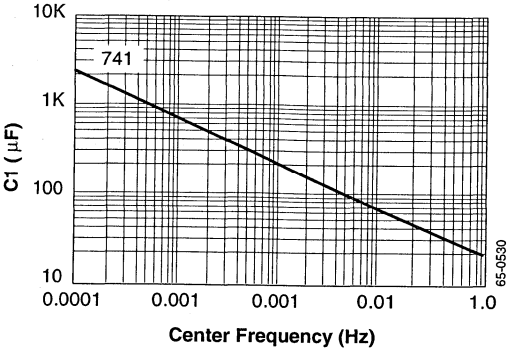


Figure 33. Notch Frequency vs. C1

Typical Applications (continued)

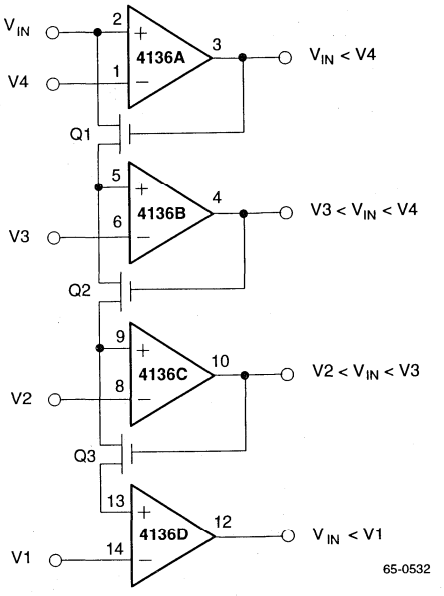


Figure 34. Multiple Aperture Window Discriminator

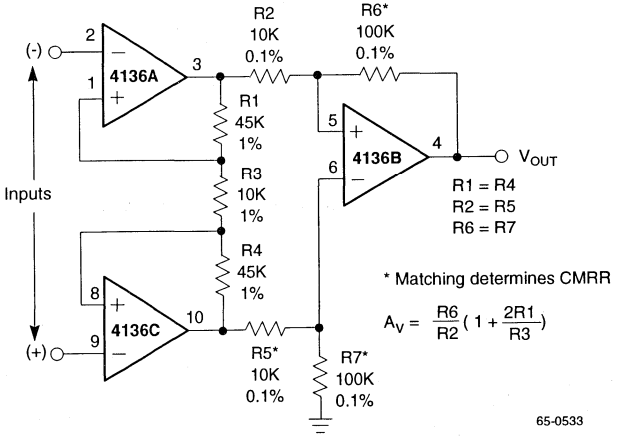


Figure 35. Differential Input Instrumentation Amplifier with High Common Mode Rejection

Typical Applications (continued)

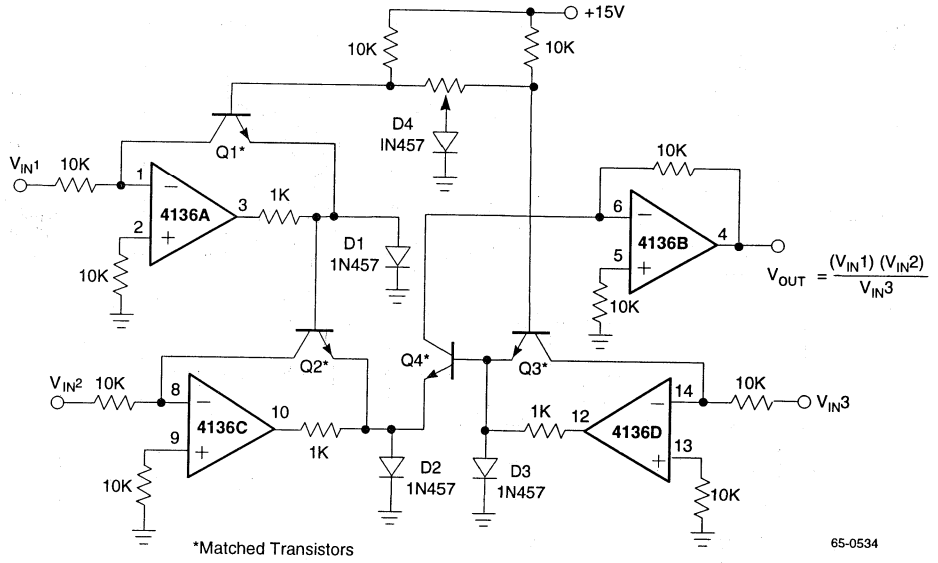


Figure 36. Analog Multiplier/Divider

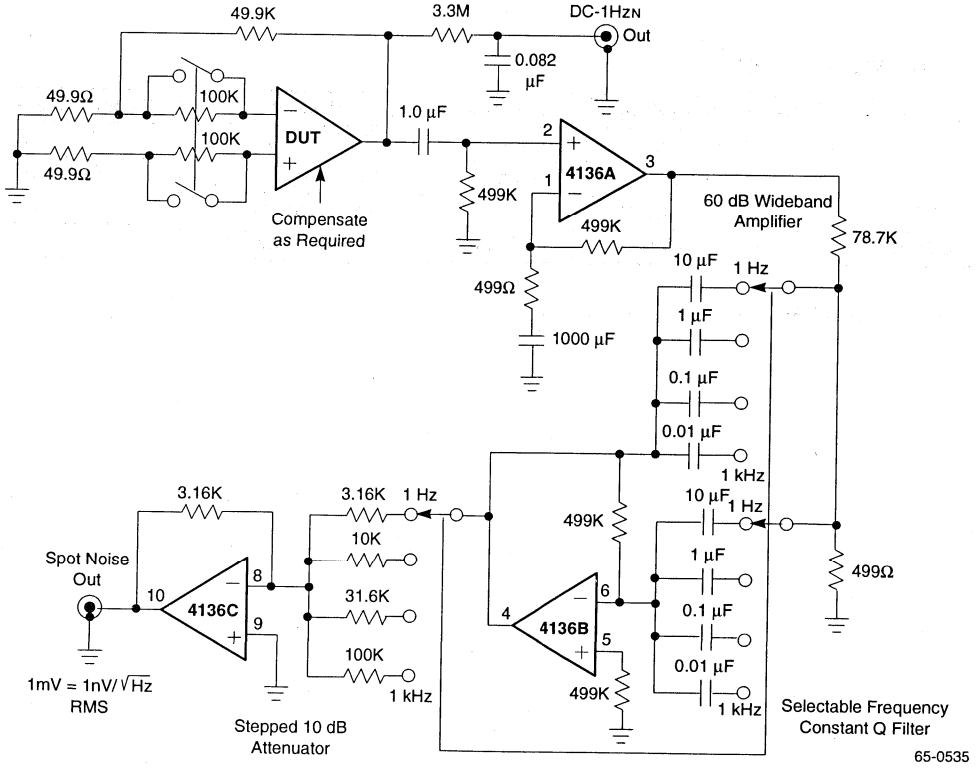
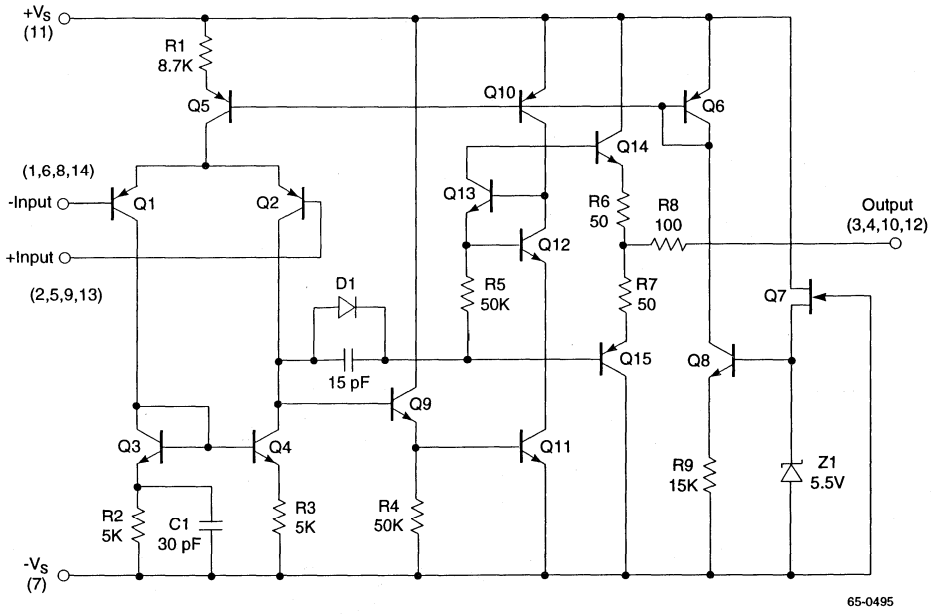


Figure 37. Spot Noise Measurement Test Circuit

Simplified Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC4136N	0° to 70°C	Commercial	14 Pin Plastic DIP	RC4136N
RC4136M	0° to 70°C	Commercial	14 Pin Narrow SOIC	RC4136M
RM4136D	-55°C to +125°C		14 Pin Ceramic DIP	
RM4136D/883[1]	-55°C to +125°C	Military	14 Pin Ceramic DIP	

Note:

1. /883 denotes MIL-STD-883, Par. 1.2.1 compliant device.

RC4156/RC4157

High Performance Quad Operational Amplifiers

Features

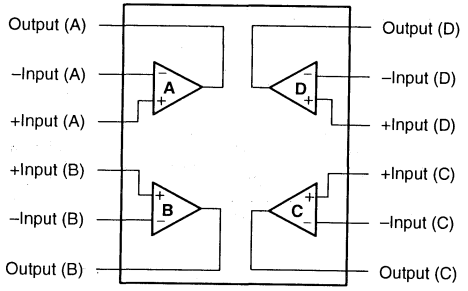
- Unity gain bandwidth for RC4156 – 3.5 MHz
- Unity gain bandwidth for RC4157 – 19 MHz
- High slew rate for RC4156 – 1.6 V/µS
- High slew rate for RC4157 – 8.0V/µS
- Low noise voltage – 1.4 µVRMS
- Indefinite short circuit protection
- No crossover distortion

Description

The RC4156 and RC4157 are monolithic integrated circuits, consisting of four independent high performance operational amplifiers constructed with an advanced epitaxial process.

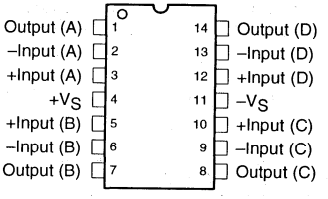
These amplifiers feature improved AC performance which far exceeds that of the 741 type amplifiers. Also featured are excellent input characteristics and low noise, making this device the optimum choice for audio, active filter and instrumentation applications. The RC4157 is a decompensated version of the RC4156 and is AC stable in gain configurations of -5 or greater.

Block Diagram



65-3463-01

Pin Assignments



65-3463-02

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±20	V
Input Voltage[2]				±15	V
Differential Input Voltage				30	V
Output Short Circuit Duration[3]		Indefinite			
$P_D T_A$ < 50°C	SOIC			300	mW
	PDIP			468	mW
	CerDIP			1042	mW
Operating Temperature	RC4156/RC4157	0		70	°C
	RM4156/RM4157	-55		+125	°C
Storage Temperature		-65		150	°C
Junction Temperature	SOIC, PDIP			125	°C
	CerDIP			175	°C
Lead Soldering Temperature (60 seconds)	DIP			300	°C
	SOIC			260	°C
For T_A > 50°C Derate at	SOIC		5.0		mW/°C
	PDIP		6.25		mW/°C
	CerDIP		8.38		mW/°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit to ground on one amplifier only.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance			60		°C/W
θ_{JA}	Thermal resistance	SOIC		200		°C/W
		PDIP		160		°C/W
		CerDIP		120		°C/W

Electrical Characteristics

(V_S = ±15V, RM = -55°C ≤ T_A ≤ +125°C, RC = 0°C ≤ T_A ≤ +70°C)

Parameters	Test Conditions	RM4156/4157			RC4156/4157			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	R_S ≤ 10 kΩ			5.0			6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				320			400	nA
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} ±10V	25			15			V/mV
Output Voltage Swing	R_L ≥ 2 kΩ	±10			±10			V
Supply Current			10			10		mA
Average Input Offset Voltage Drift			5.0			5.0		µV/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RM4156/4157			RC4156/4157			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10$ kΩ		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} ±10V	50	100		25	100		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Output Resistance			230			230		Ω
Short Circuit Current			25			25		mA
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	80			80			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ	80			80			dB
Supply Current (All Amplifiers)	$R_L = \infty$		4.5	5.0		5.0	7.0	mA
Transient Response (4156)								
Rise Time			60			60		nS
Overshoot			25			25		%
Slew Rate		1.3	1.6		1.3	1.6		V/μS
Unity Gain Bandwidth (4156)		2.8	3.5		2.8	3.5		MHz
Phase Margin (4156)	R_L = 2 kΩ, C_L = 50 pF		50			50		%
Transient Response (4157)	A_V = -5							
Rise Time			50			50		nS
Overshoot			25			25		%
Slew Rate		6.5	8.0		6.5	8.0		V/μS
Unity Gain Bandwidth (4157)	A_V = -5	15	19		15	19		MHz
Phase Margin (4157)	A_V = -5, R_L = 2 kΩ, C_L = 50 pF		50			50		%
Power Bandwidth	$V_{OUT} = 20V_{p-p}$	20	25		20	25		kHz
Input Noise Voltage [1]	F = 20 Hz to 20 kHz		1.4	5.0		1.4	5.0	μV_{RMS}
Input Noise Current	F = 20 Hz to 20 kHz		15			15		pA_{RMS}
Channel Separation			108			108		dB

Note:

1. Sample tested only.

Typical Performance Characteristics

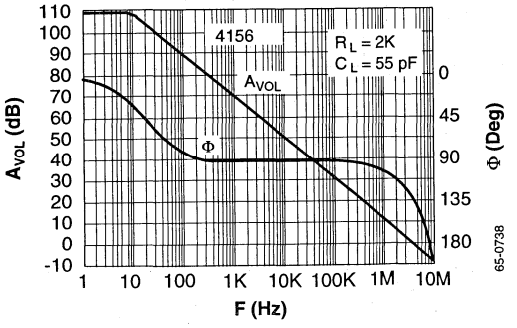


Figure 1. Open Loop Gain, Phase vs. Frequency

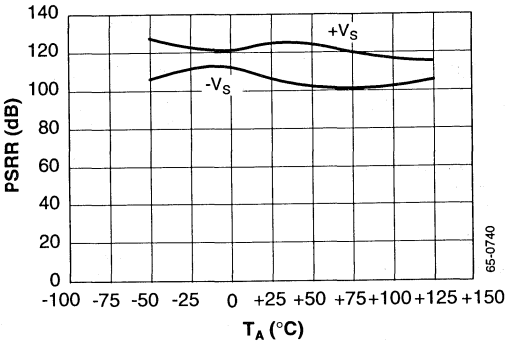
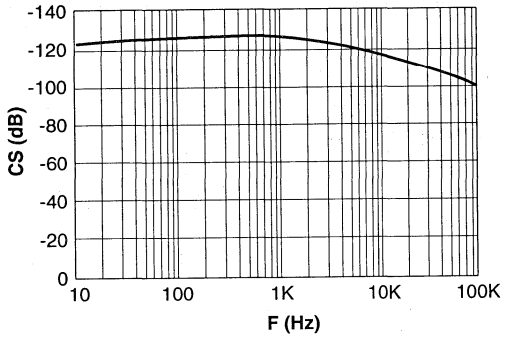


Figure 2. PSRR vs. Temperature



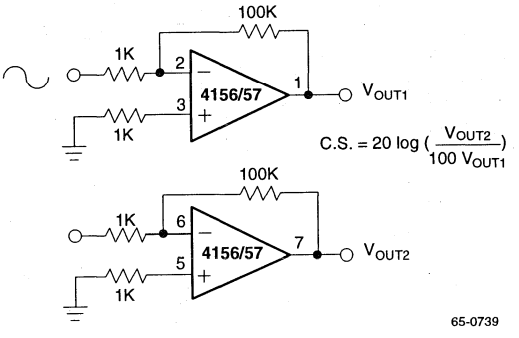


Figure 3. Channel Separation vs. Frequency

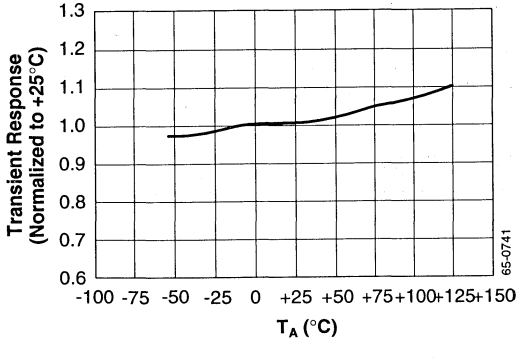


Figure 4. Transient Response vs. Temperature

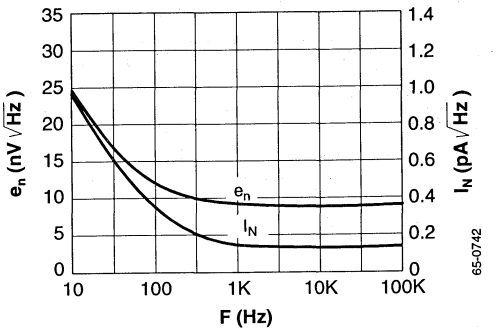


Figure 5. Input Noise Voltage, Current Density vs. Frequency

Typical Performance Characteristics (continued)

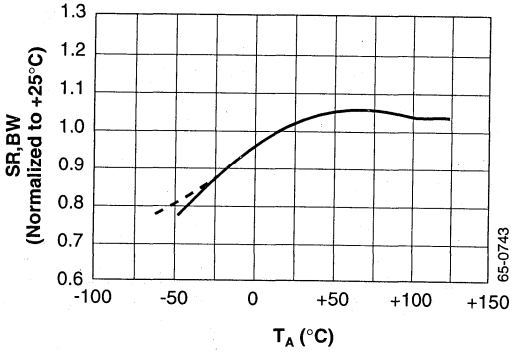


Figure 6. Slew Rate, Bandwidth vs. Temperature

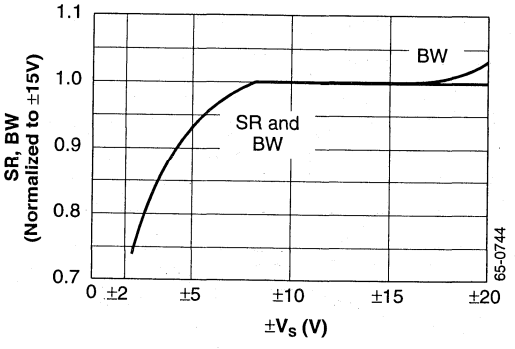


Figure 7. Slew Rate, Bandwidth vs. Supply Voltage

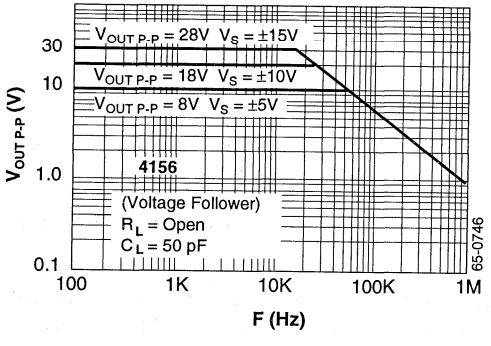


Figure 8. Output Voltage Swing vs. Frequency

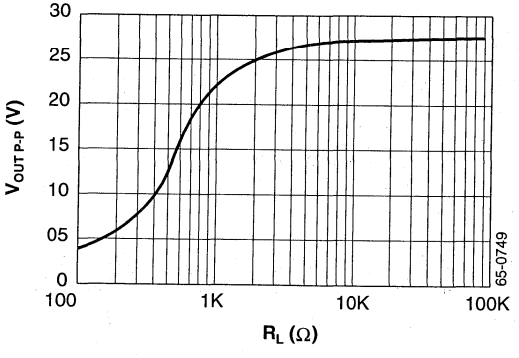


Figure 9. Output Voltage Swing vs. Load Resistance

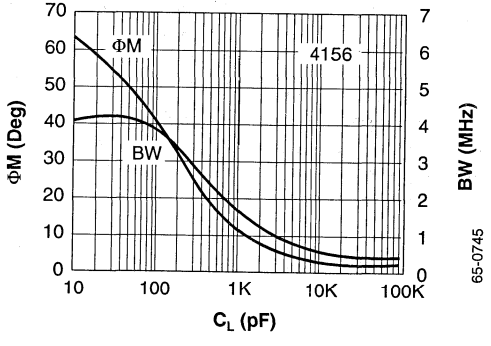


Figure 10. Small Signal Phase Margin, Unity Gain Bandwidth vs. Load Capacitance

Typical Performance Characteristics (continued)

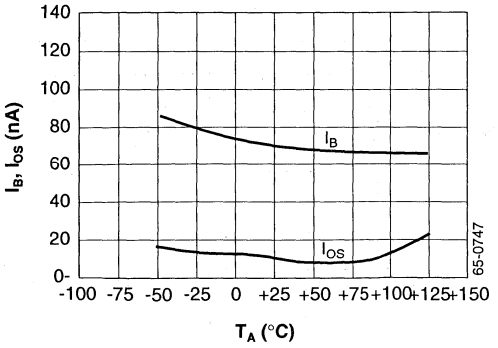


Figure 11. Input Bias, Offset Current vs. Temperature

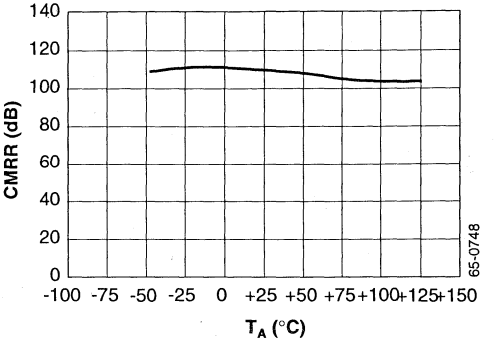


Figure 12. CMRR vs. Temperature

Applications

The RC4156 and RC4157 quad operational amplifiers can be used in almost any 741 application and will provide superior performance. The higher unity gain bandwidth and slew rate make it ideal for applications requiring good frequency response, such as active filter circuits, oscillators and audio amplifiers.

The following applications have been selected to illustrate the advantages of using the Raytheon RC4156 and RC4157 quad operational amplifiers.

Triangle and Square Wave Generator

The circuit of Figure 13 uses a positive feedback loop closed around a combined comparator and integrator. When power is applied the output of the comparator will switch to one of two states, to the maximum positive or maximum negative voltage. This applies a peak input signal to the integrator, and the integrator output will ramp either down or up, opposite of the input signal. When the integrator output (which is connected to the comparator input) reaches a threshold set by R1 and R2, the comparator will switch to the opposite polarity. This cycle will repeat endlessly, the integrator charging positive then negative, and the comparator switching in a square wave fashion.

The amplitude of V_2 is adjusted by varying R1. For best operation, it is recommended that R1 and V_R be set to obtain a triangle wave at V_2 with ±12V amplitude. This will then allow A3 and A4 to be used for independent adjustment of output-offset and amplitude over a wide range.

The triangle wave frequency is set by C0, R0, and the maximum output voltages of the comparator. A more symmetrical waveform can be generated by adding a back-to-back Zener diode pair as shown in Figure 14.

An asymmetric triangle wave is needed in some applications. Adding diodes as shown by the dashed lines is a way to vary the positive and negative slopes independently.

The frequency range can be very wide and the circuit will function well up to about 10 kHz. The square wave transition time at V_1 is less than 21 µS when using the RC4156.

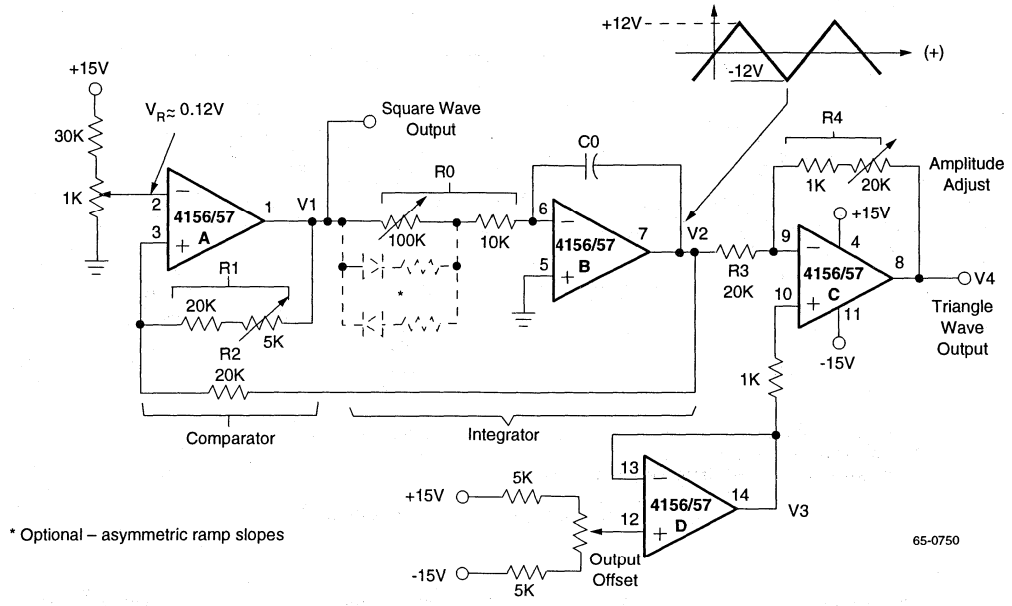


Figure 13. Triangle and Square Wave Generator

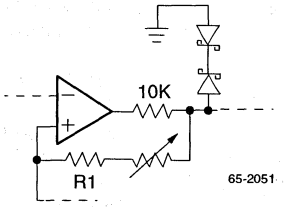


Figure 14. Triangle Generator—Symmetrical Output Option

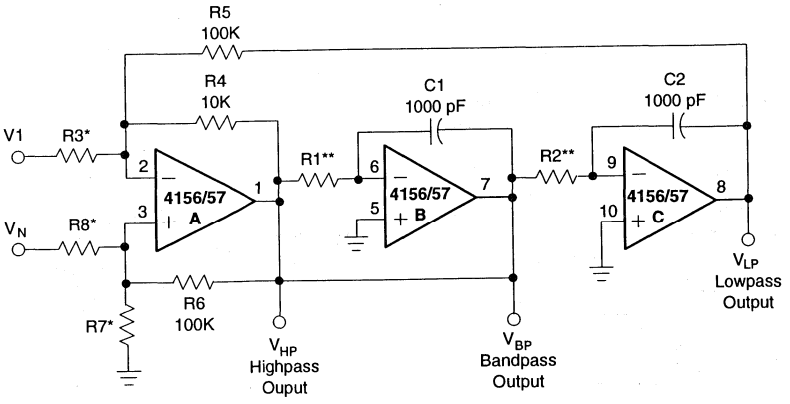
Active Filters

The introduction of low-cost quad op amps has had a strong impact on active filter design. The complex multiple-feedback, single op amp filter circuits have been rendered obsolete for most applications. State-variable active-filter circuits using three to four op amps per section offer many advantages over the single op amp circuits. They are relatively insensitive to the passive-component tolerances and variations. The Q, gain, and natural frequency can be independently adjusted. Hybrid construction is very practical because resistor and capacitor values are relatively low and the filter parameters are determined by resistance ratios rather than by single resistors. A generalized circuit diagram of the 2-pole state-variable active filter is shown in Figure 15. The particular input connections and component-values can be calculated for specific applications. An important feature of the state-variable filter is that it can be inverting or non-inverting and can simultaneously provide three outputs: lowpass, bandpass, and highpass. A notch filter can be realized by adding one summing op amp.

The RC4156 was designed and characterized for use in active filter circuits. Frequency response is fully specified with minimum values for unity-gain bandwidth, slew-rate, and full-power response. Maximum noise is specified.

Output swing is excellent with no distortion or clipping. The RC4156 provides full, undistorted response up to 20 kHz and is ideal for use in high-performance audio and telecommunication equipment.

In the state-variable filter circuit, one amplifier performs a summing function and the other two act as integrators. The choice of passive component values is arbitrary, but must be consistent with the amplifier operating range and input signal



* Input connections are chosen for inverting or non-inverting response. Values of R3,R7,R8 determine gain and Q.
** Values of R1 and R2 determine natural frequency.

65-0751

Figure 15. 2-Pole State-Variable Active Filter

characteristics. The values shown for C1, C2, R4, R5 and R6 are arbitrary. Pre-selecting their values will simplify the filter tuning procedures, but other values can be used if necessary.

The generalized transfer function for the state-variable active filter is:

$$T(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0}$$

Filter response is conventionally described in terms of a natural frequency ω_0 in radians/sec, and Q, the quality of the complex pole pair. The filter parameters ω_0 and Q relate to the coefficients in T(s) as:

$$\omega_0 = \sqrt{b_0} \text{ and } Q = \frac{\omega_0}{b_0}$$

The input configuration determines the polarity (inverting or non-inverting), and the output selection determines the type of filter response (lowpass, bandpass, or highpass).

Notch and all-pass configurations can be implemented by adding another summing amplifier.

Bandpass filters are of particular importance in audio and telecommunication equipment. A design approach to bandpass filters will be shown as an example of the state-variable configuration.

Design Example Bandpass Filter

For the bandpass active filter (Figure 16) the input signal is applied through R3 to the inverting input of the summing amplifier and the output is taken from the first integrator (V_{BP}). The summing amplifier will maintain equal voltage at the inverting and non-inverting inputs (see Equation 1).

$$\frac{\frac{R3R5}{R3+R5}}{R4+\frac{R3R5}{R3+R5}} V_{HP}(s) + \frac{\frac{R3R4}{R3+R4}}{R5+\frac{R3R4}{R3+R4}} V_{LP}(s) + \frac{\frac{R4R5}{R4+R5}}{R3+\frac{R4R5}{R4+R5}} V_{IN}(s) + \frac{R7}{R6+R7} V_{BP}(s)$$

Equation 1.

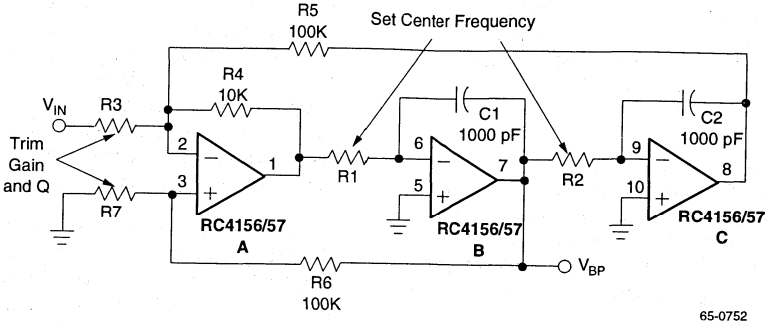


Figure 16. Bandpass Active Filter

These equations can be combined to obtain the transfer function:

$$V_{BP}(s) = -\frac{1}{R1C1S}V_{HP}(s) \quad \text{and} \quad V_{LP}(s) = -\frac{1}{R2C2S}V_{BP}(s)$$

$$\frac{V_{BP}(s)}{V_{IN}(s)} = \frac{\frac{R4}{R3}\cdot\frac{1}{R1C1}S}{S^2 + \frac{R7}{R6+R7}\left(1+\frac{R4}{R5}+\frac{R4}{R3}\right)\left(\frac{1}{R1C1}\right)S + \left(\frac{R4}{R5}\right)\left(\frac{1}{R1C1R2C2}\right)}$$

Defining 1/R1C1 as ω1, 1/R2C2 as ω2, and substituting in the assigned values for R4, R5, and R6, then the transfer function simplifies to:

$$\frac{V_{BP}(s)}{V_{IN}(s)} = \frac{\frac{10^4}{R3}\cdot\omega_1 s}{S^2 + \left[\frac{1.1+\frac{10^4}{R3}}{1+\frac{10^5}{R7}}\right]\omega_1 s + \frac{1}{\omega_1\omega_2}}$$

This is now in a convenient form to look at the center-frequency ω0 and filter Q.

$$\omega_0 = \sqrt{0.1\omega_1\omega_2}$$

$$\omega_0 = 10^{-9}\sqrt{0.1R1R2} \quad \text{and}$$

$$Q = \left[\frac{1+\frac{10^5}{R7}}{1.1+\frac{10^4}{R3}}\right]\omega_0$$

The frequency responses for various values of Q are shown in Figure 17.

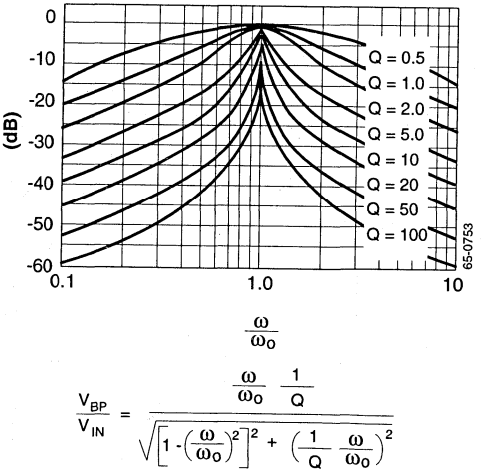


Figure 17. Bandpass Transfer Characteristics Normalized for Unity Gain and Frequency

These equations suggest a tuning sequence where ω is first trimmed via R1 or R2, then Q is trimmed by varying R7 and/or R3. An important advantage of the state-variable bandpass filter is that Q can be varied without affecting center frequency ω_0.

This analysis has assumed ideal op amps operating within their linear range, which is a valid design approach for a reasonable range of ω_0 and Q. At extremes of ω_0 and at high values of Q, the op amp parameters become significant. A rigorous analysis is very complex, but some factors are particularly important in designing active filters.

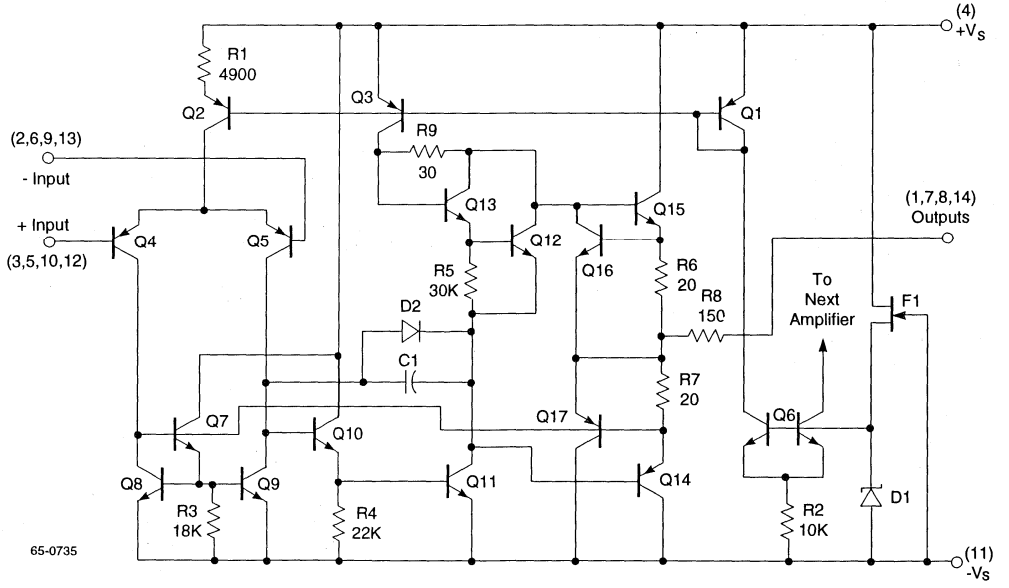
1. The passive component values should be chosen such that all op amps are operating within their linear region for the anticipated range of input signals. Slew rate, output current rating, and common-mode input range must be considered. For the integrators, the current through the feedback capacitor (I = C dV/dt) should be included in the output current computations.

2. From the equation for Q, it should seem that infinite Q could be obtained by making R7 zero. But as R7 is made small, the Q becomes limited by the op amp gain at the frequency of interest. The effective closed-loop gain is being increased directly as R7 is made smaller, and the ratio of open-loop gain to closed-loop gain is becoming less. The gain and phase error of the filter at high Q is very dependent on the op amp open-loop gain at w_0.

3. The attenuation at extremes of frequency is limited by the op amp gain and unity-gain bandwidth. For integrators, the finite open-loop op amp gain limits the accuracy at the low-end. The open-loop roll-off of gain limits the filter attenuation at high frequency.

The RC4156 quad operational amplifier has much better frequency response than a conventional 741 circuit and is ideal for active filter use. Natural frequencies of up to 10 kHz are readily achieved and up to 20 kHz is practical for some configurations. Q can range up to 50 with very good accuracy and up to 500 with reasonable response. The extra gain of the RC4156 at high frequencies gives the quad op amp an extra margin of performance in active-filter circuits.

Schematic Diagram (1/4 shown)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC4156N/RC4157N	0° to 70°C	Commercial	14 Pin Plastic DIP	RC4136N
RC4156M/RC4157M	0° to 70°C	Commercial	14 Pin Wide SOIC	RC4136M
RM4156D	-55°C to +125°C		14 Pin Ceramic DIP	
RM4156D/883B	-55°C to +125°C	Military	14 Pin Ceramic DIP	

THIS PAGE INTENTIONALLY LEFT BLANK

RC4207

Precision Dual Operational Amplifier

Features

- Low Noise – 0.35 μV_{p-p} (0.1 Hz to 10 Hz)
- Ultra-low V_{OS} – 75 μV
- Ultra-low V_{OS} drift – 1.3 $\mu V/°C$
- Long term V_{OS} stability – 0.2 $\mu V/Mo$
- Low input bias and offset currents – ±5 nA
- High gain – 400 V/mV
- Fits 4558 socket
- Industry standard pinout
- 8-lead mini-DIP

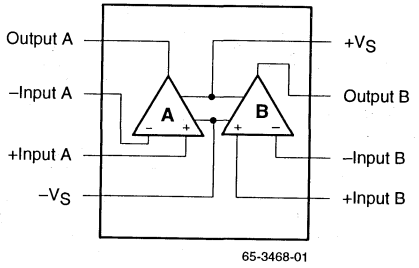
Description

Designed for low level signal conditioning and instrumentation applications, the 4207 is a precision dual amplifier combining excellent DC input specifications with low input noise characteristics. Ultra low input offset voltage, low drift, high CMRR, and low input bias currents serve to reduce input related errors to less than 0.01% in a typical high gain instrumentation amplifier system (A_V = 1000). The 4207 contains two separate amplifiers with a high degree of isolation between them; each is complete requiring no external compensation capacitors or offset nulling potentiometers.

The inherent V_{OS} is typically less than 150 μV, resulting in superior temperature drift, and this low initial offset is further reduced by "Zener-zap" nulling when the wafers are tested.

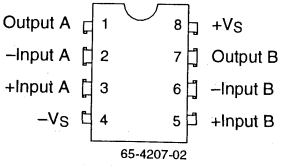
Advanced thin film and nitride dielectric processing allows the 4207 to achieve its high performance and small size (the 4207 is offered in 8-lead DIPs). The 4207 fits the industry standard 8-lead op amp pin-out.

Block Diagram



65-3468-01

Pin Assignments



65-4207-02

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±18	V
Input Voltage[2]				±18	V
Differential Input Voltage				30	V
Internal Power Dissipation[3]				500	mW
$P_D T_A < 50°C$				468	mW
Output Short Circuit Duration			Indefinite		
Junction Temperature				125	°C
Storage Temperature		-65		150	°C
Operating Temperature		0		70	°C
Lead Soldering Temperature (60 sec)				300	°C
For $T_A > 50°C$ Derate at			6.25		mW/°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
3. Observe package thermal characteristics.

Operating Conditions

Parameter		Min	Typ	Max	Units
θ_{JA}	Thermal resistance		160		°C/W

Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	4207F			4207G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			45	150		85	250	µV
Average Input Offset Voltage Drift[2]			0.3	1.3		0.7		µV/°C
Input Offset Current			±2.0	±10		±1.6	±15	nA
Average Input Offset Current Drift			8.0			12		pA/°C
Input Bias Current			±2.0	±10		±3.0	±15	nA
Average Input Bias Current Drift			13			18		pA/°C
Input Voltage Range		±10	±13.5		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	94	120		92	106		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	94	115		92	100		dB
Large Signal Voltage Gain	$R_L > 2.0k\Omega$, V_{OUT} = ±10V	200	450		75	400		V/mV
Maximum Output Voltage Swing	$R_L > 2.0k\Omega$	±11	±12.6		±11	±12.6		V
Power Consumption	$R_L = \infty$		150	240		150	240	mW

Electrical Characteristics

(V_S = ±15V, and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	4207F			4207G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			30	75		60	150	µV
Long Term V_{OS} Stability[1]			0.2			0.5		µV/Mo
Input Offset Current			±0.5	±5		±2	±10	nA
Input Bias Current			±0.5	±5		±2	±10	nA
Input Noise Voltage	0.1 Hz to 10 Hz		0.35			0.35		µVp-p
Input Noise Voltage Density	F_O = 10 Hz		10.3			10.3		$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10			10		
	F_O = 1000 Hz		9.6			9.6		
Input Noise Current	0.1 Hz to 10 Hz		14			14		pA_{p-p}
Input Noise Current Density	F_O = 10 Hz		0.32			0.32		$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14			0.14		
	F_O = 1000 Hz		0.12			0.12		
Input Resistance (Diff. Mode)			60			31		MΩ
Input Resistance (Com. Mode)			200			120		GΩ
Input Voltage Range[4]		±11	±14		±11	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	100	126		94	110		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	110		94	104		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	400	600		250	400		V/mV
	V_{OUT} = ±1.0V R_L = 1KΩ, V_S = ±4.0V	200	400		100	200		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±12	±12.8		
	$R_L \geq 1k\Omega$	±11	±12		±11	±12		
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		0.1	0.3		V/µs
Closed Loop Bandwidth	A_{VOL} = +1.0		1.5			1.5		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		150	200		160	240	mW
	V_S = ±4.0V, R_L = ∞		35	50		48	64	
Crosstalk	DC	126	155		126	155		dB

Notes:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Typical Performance Characteristics

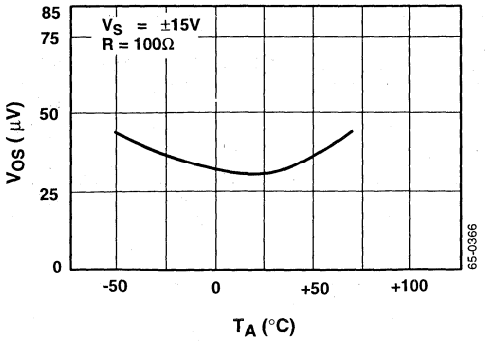


Figure 1. Input Offset Voltage vs. Temperature

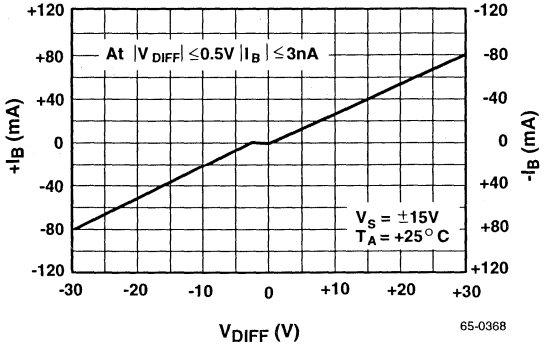


Figure 2. Input Bias Current vs. Differential Input Voltage

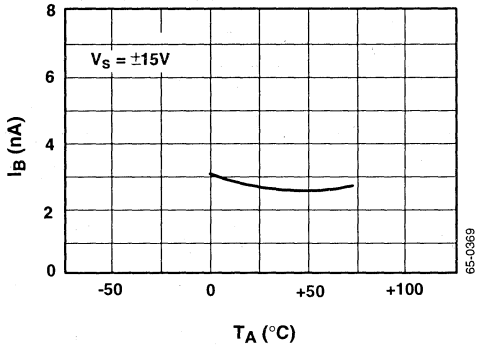


Figure 3. Input Bias Current vs. Temperature

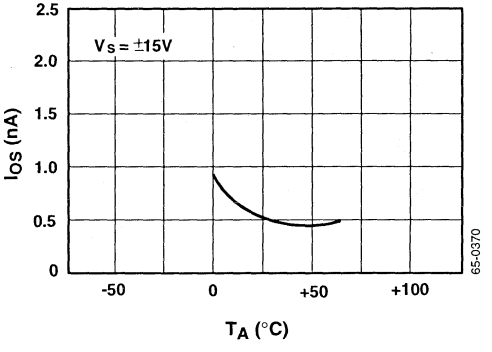


Figure 4. Input Offset Current vs. Temperature

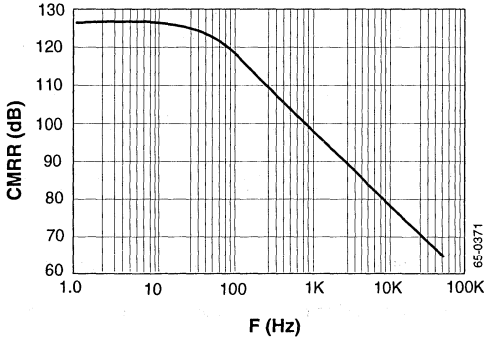


Figure 5. CMRR vs. Frequency

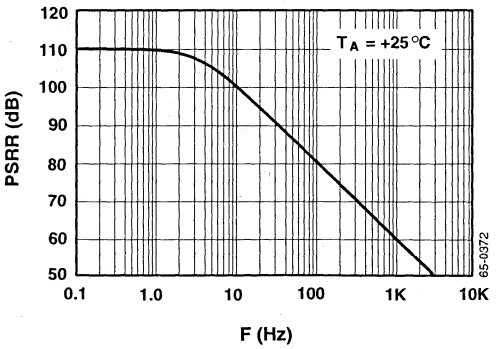


Figure 6. PSRR vs. Frequency

Typical Performance Characteristics (continued)

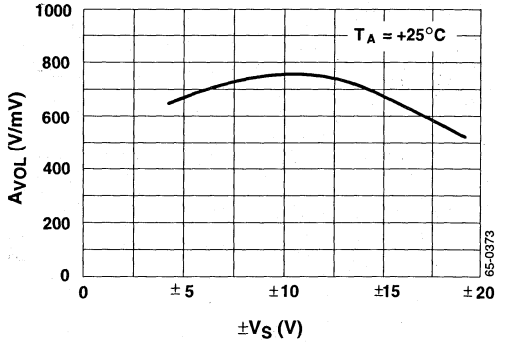


Figure 7. Open Loop Gain vs. Supply Voltage

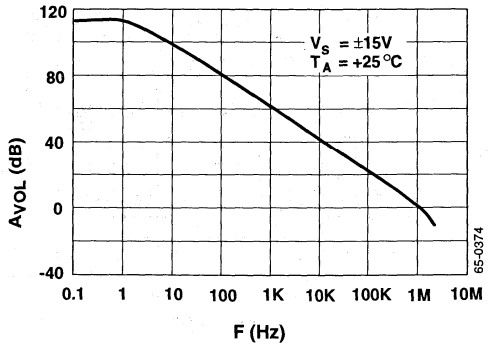


Figure 8. Open Loop Gain vs. Frequency

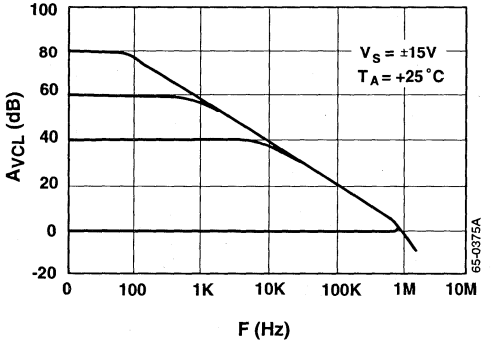


Figure 9. Closed Loop Response for Various Gain Configurations

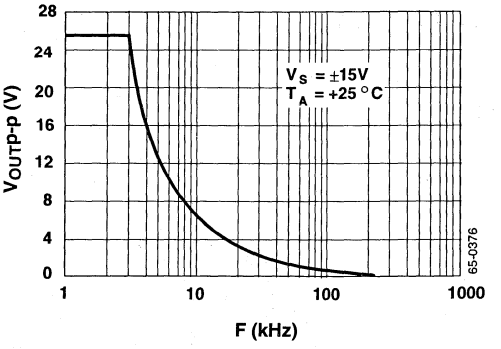


Figure 10. Maximum Undistorted Output vs. Frequency

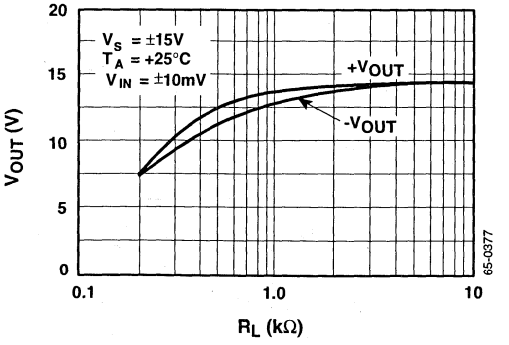


Figure 11. Output Voltage vs. Load Resistance to Ground

Typical Performance Characteristics (continued)

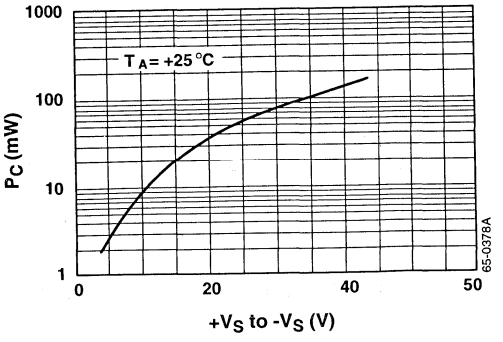


Figure 12. Power Consumption vs. Total Supply Voltage

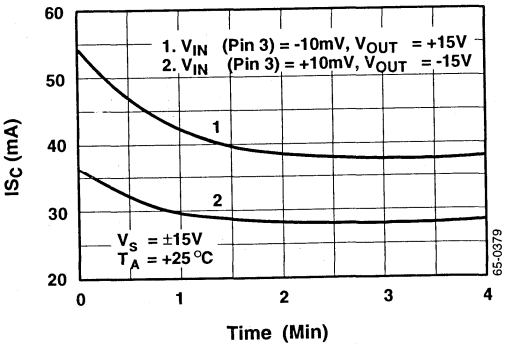


Figure 13. Output Short Circuit Current vs. Time

Typical Applications

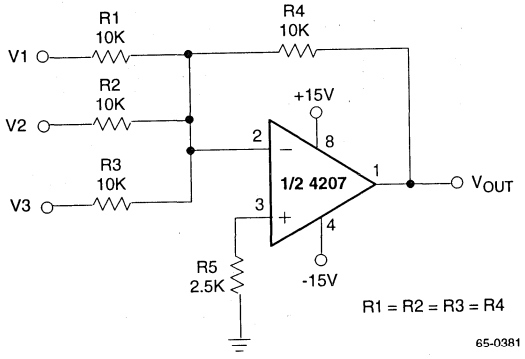


Figure 14. Adjustment-Free Precision Summing Amplifier

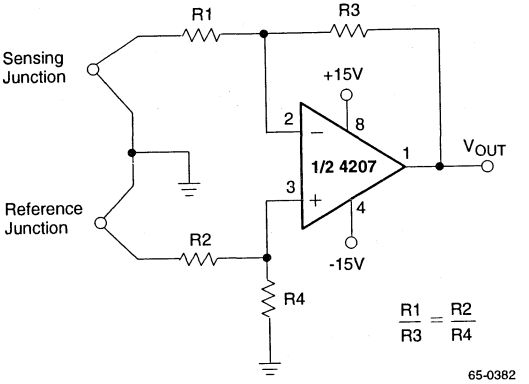


Figure 15. High Stability Thermocouple Amplifier

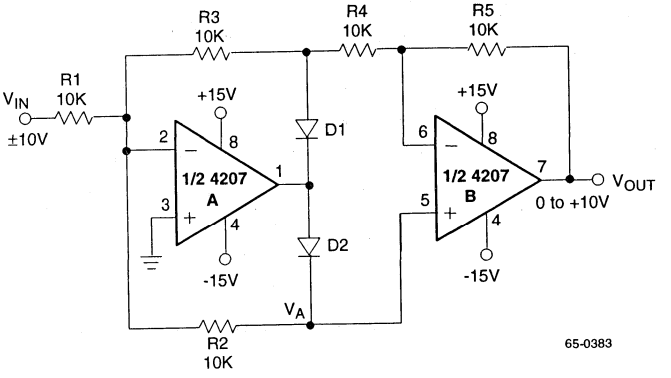
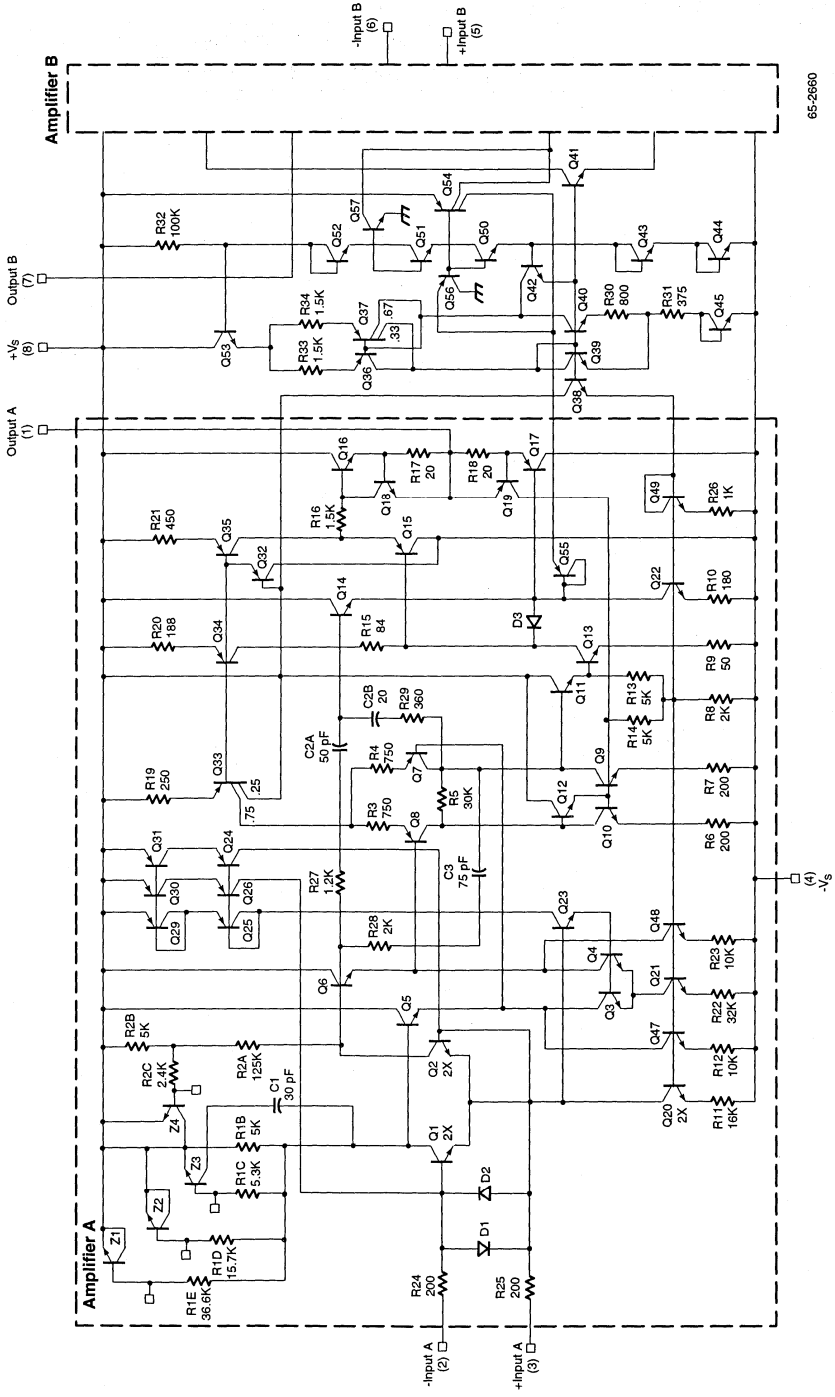


Figure 16. Precision Absolute Value Circuit

Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package
RC4207FN	0° to +70°C	Commercial	8 Pin Plastic DIP
RC4207GN	0° to +70°C	Commercial	8 Pin Plastic DIP

RC4227

Dual Precision Operational Amplifier

Features

- Very low noise
  Spectral noise density – 3.8 nV/√Hz
  1/F noise corner frequency – 2.7 Hz
- Very low VOS drift – 0.3 µV/Mo; 0.3 µV/°C
- High gain – 500 V/mV
- High output drive capability – ±10V into 1K load
- High slew rate – 2.7 V/µS
- Wide gain bandwidth product – 8 MHz
- High common mode rejection ratio – 104 dB
- Low input offset voltage – 75 µV
- Low frequency noise – 0.08 μV_{p-p} (0.1 Hz to 10 Hz)
- Low input offset current – 2.5 nA
- Industry standard pinout
- 8-Lead DIP

Description

The RC4227, a dual version of the OP-27, is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents. These features are all available in a device which is internally compensated for excellent phase margin (70°) in a unity gain configuration. Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 75 µV max. Input bias current cancellation techniques are used to obtain ±45 nA max. input bias currents.

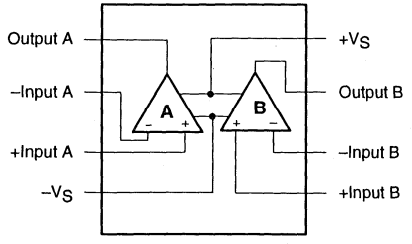
In addition to providing superior performance for audio frequency range applications, the RC4227 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 100 dB. A phase margin of 70° at unity gain guards against peaking (and ringing) in low gain feedback circuits. Stable operation can be obtained with capacitive loads up to 2000 pF[1]. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

The performance of the RC4227 is achieved using precision amplifier design techniques coupled with a process that combines nitride transistors and capacitors with precision thin-film resistors. The die size savings of nitride capacitors and thin film resistors allow the RC4227 to be offered in an 8-pin mini-dip package and fit the industry standard dual op amp pinout.

Note:

1. By decoupling the load capacitance with a series resistor of 50Ω or more, load capacitances larger than 2000 pF can be accommodated.

Block Diagram



65-3468-01

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±18	V
Input Voltage[2]				±18	V
Differential Input Voltage				0.7	V
Internal Power Dissipation[3]				658	mW
$P_D T_A$ < 50°C	PDIP			468	mW
	CerDIP			833	
Output Short Circuit Duration		Indefinite			
Junction Temperature	PDIP			125	°C
	CerDIP			175	
Storage Temperature		-65		150	°C
Operating Temperature	RM4227B	-55		125	°C
	RC4227F/G	0		70	
Lead Soldering Temperature (60 sec)				300	°C
For T_A > 50°C Derate at	PDIP		6.25		mW/°C
	CerDIP		8.33		

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
3. Observe package thermal characteristics.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		CerDIP		150		°C/W

Electrical Characteristics

(V_S = ±15V, and $T_A \leq +25°C$ unless otherwise noted)

Parameters	Test Conditions	4227B/F			4227G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			20	150		30	180	µV
Long Term V_{OS} Stability[1]			0.3			0.4		µV/Mo
Input Offset Current			±2.5	±10		±5	±15	nA
Input Bias Current			±5	±15		±7.5	±25	nA
Input Noise Voltage	0.1 Hz to 10 Hz		0.08			0.08		μV_{p-p}
Input Noise Voltage Density	F_O = 10 Hz		3.8			3.8		$\frac{nV}{\sqrt{Hz}}$
	F_O = 30 Hz		3.3			3.3		
	F_O = 1000 Hz		3.2			3.2		
Input Noise Current Density	F_O = 10 Hz		1.7			1.7		$\frac{pA}{\sqrt{Hz}}$
	F_O = 30 Hz		1.0			1.0		
	F_O = 1000 Hz		0.4			0.4		
Input Resistance (Diff. Mode)			5.0			4.0		MΩ
Input Resistance (Com. Mode)			2.5			2.0		GΩ
Input Voltage Range[2, 4]		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	104	123		100	120		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	104	120		100	118		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	500	1000		400	800		V/mV
	V_{OUT} = ±10V, R_L = 1KΩ	400	800		300	600		
	V_{OUT} = ±1.0V V_S = ±4.0V, $R_L \geq 1.0k\Omega$	250	500		200	400		
Output Voltage Swing	$R_L \geq 2.0k\Omega$	±12	±13.8		±12	±13.8		V
	$R_L \geq 1k\Omega$	±11	±12		±11	±12		
Slew Rate[2]	$R_L \geq 2.0k\Omega$	1.5	2.7		0.1	0.3		V/µs
Gain Bandwidth Product		5.0	8.0		5.0	8.0		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		70			70		Ω
Power Consumption	$R_L = \infty$		160	200		180	240	mW
Crosstalk		126	155		126	155		dB

Notes:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in VOS during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Electrical Characteristics

(V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	4227B			Units
		Min	Typ	Max	
Input Offset Voltage[1]			120	400	µV
Average Input Offset Voltage Drift[2]			0.3	3.5	µV/°C
Input Offset Current			±10	±35	nA
Input Bias Current			±15	±45	nA
Input Voltage Range		±10	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	100	119		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	114		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	350	650		V/mV
Output Voltage Swing	R_L ≥ 2.0 kΩ	±11	±13.2		V
Power Consumption	R_L = ∞		200	280	mW

Notes:

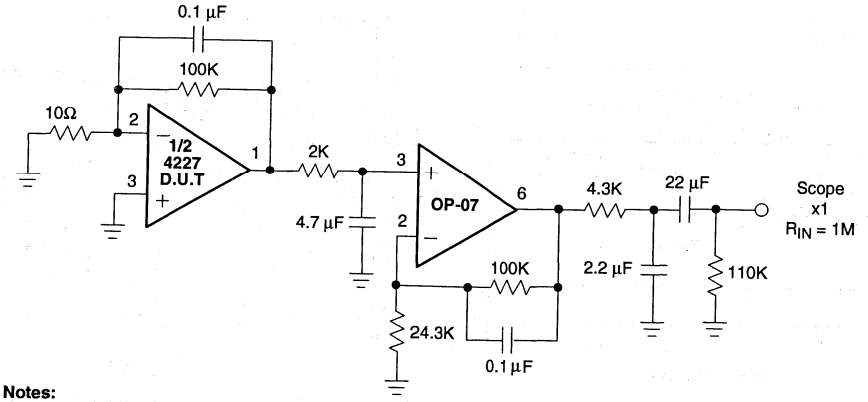
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.

Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	4227F			4227G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			45	150		85	250	µV
Average Input Offset Voltage Drift[2]			0.3	1.3		0.4		µV/°C
Input Offset Current			±8	±15		±10	±35	nA
Input Bias Current			±10	±30		±15	±45	nA
Input Voltage Range		±10	±11.8		±10	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	100	121		92	118		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	116		92	114		dB
Large Signal Voltage Gain	R_L > 2.0kΩ, V_{OUT} = ±10V	350	700		250	500		V/mV
Output Voltage Swing	R_L > 2.0kΩ	±11	±13.5		±11	±13.5		V
Power Consumption	R_L = ∞		180	240	200	280		mW

Typical Performance Characteristics



Notes:

1. Peak-to-peak noise measured in a 10-second interval.
2. The device under test should be warmed up for 3 minutes and shielded from air currents.
3. Voltage gain = 50,000.

65-3469-01

Figure 1. 0.1 Hz to 10 Hz Noise Test Circuit (1/2 Shown)

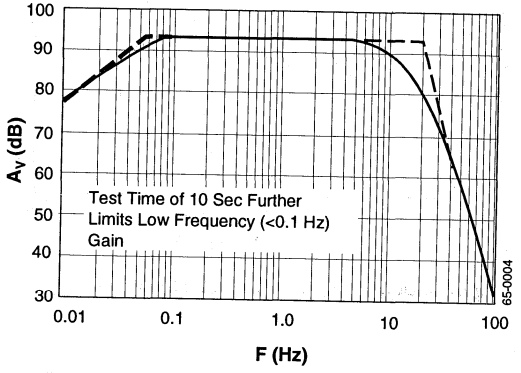


Figure 2. 0.1Hz to 10Hz Noise Gain vs. Frequency

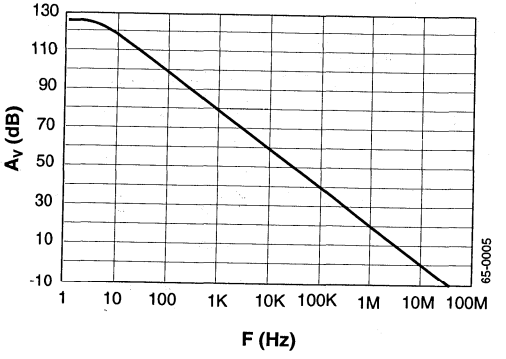


Figure 3. Open Loop Gain vs. Frequency

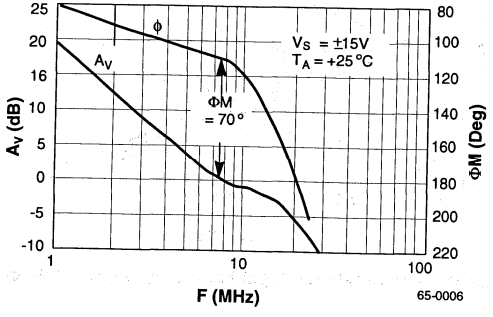


Figure 4. Gain, Phase Shift vs. Frequency

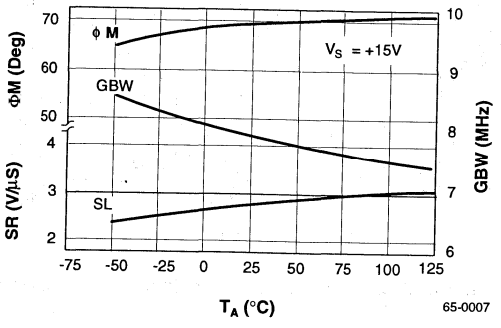


Figure 5. Slew Rate, Gain Bandwidth Product, Phase Margin vs. Temperature

Typical Performance Characteristics (continued)

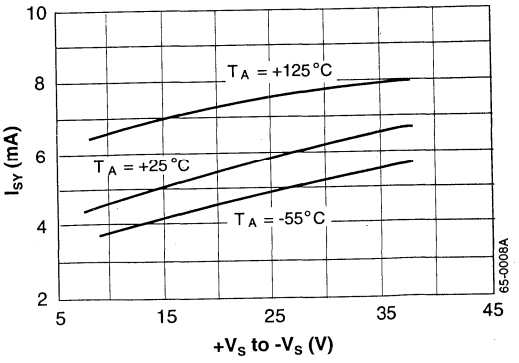


Figure 6. Supply Voltage vs. Total Supply Voltage

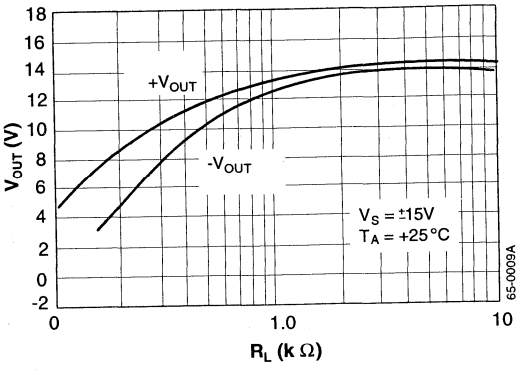


Figure 7. Maximum Output Swing vs. Load Resistance

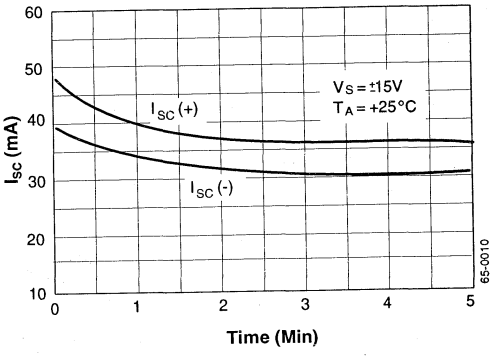


Figure 8. Short Circuit vs. Time

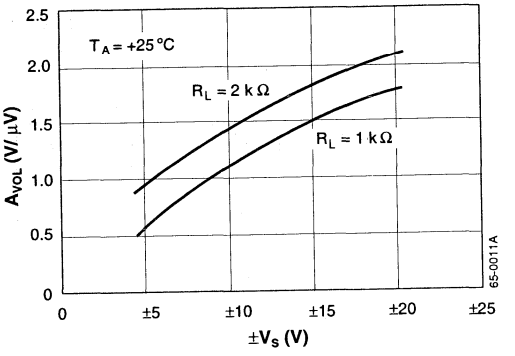


Figure 9. Open-Loop Gain vs. Total Supply Voltage

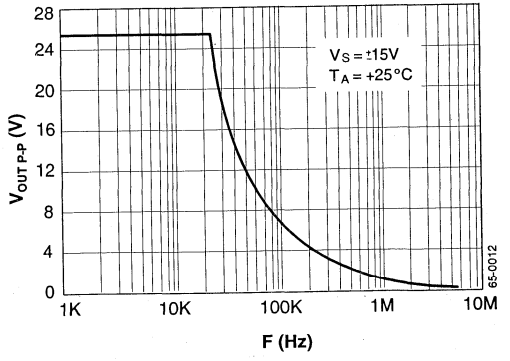


Figure 10. Maximum Undistorted Output vs. Frequency

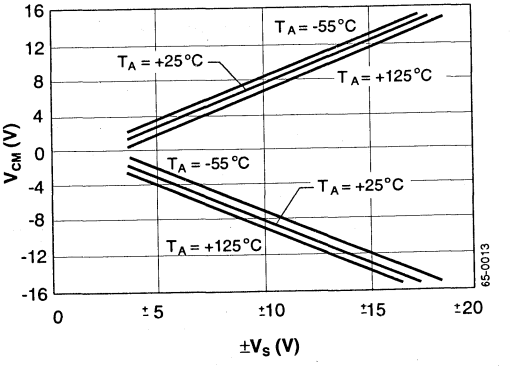


Figure 11. Common-Mode Input Range vs. Supply Voltage

Typical Performance Characteristics (continued)

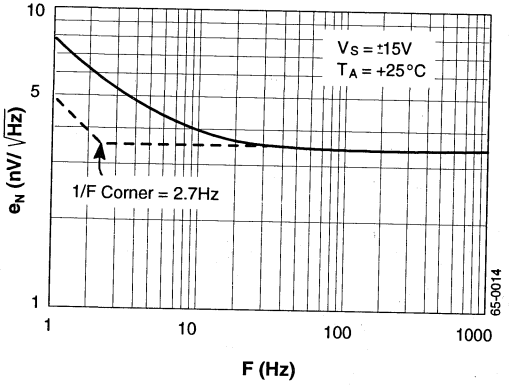


Figure 12. Input Noise Voltage Density vs. Frequency

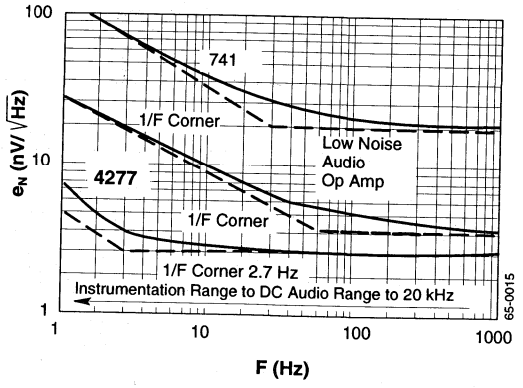


Figure 13. Op Amp Compensation Input Noise Voltage Density vs. Frequency

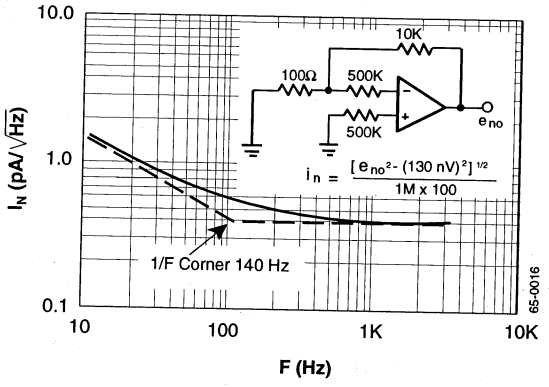
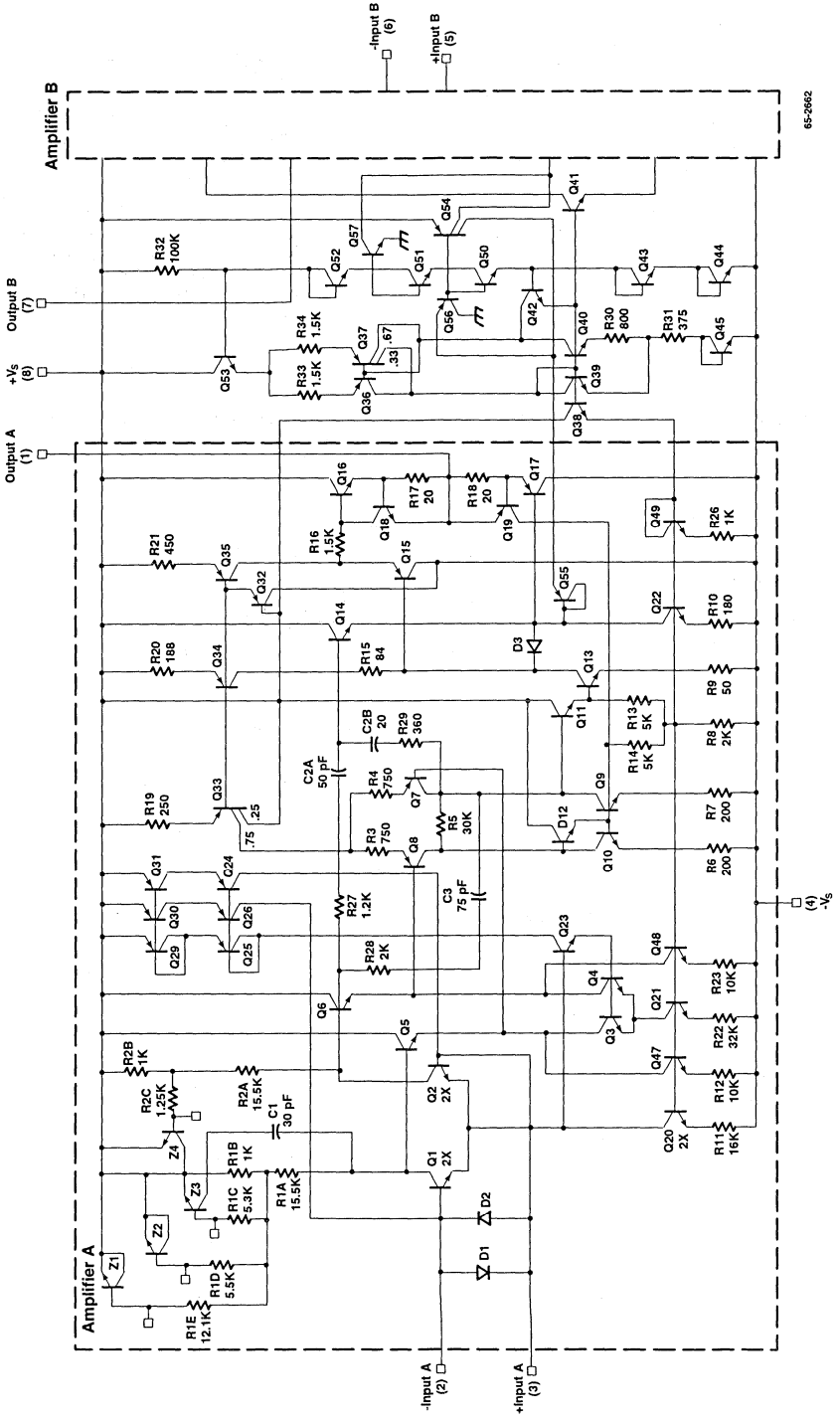


Figure 14. Input Noise Current Density vs Frequency

Simplified Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package
RC4227FN	0° to +70°C	Commercial	8 Pin Plastic DIP
RC4227GN	0° to +70°C	Commercial	8 Pin Plastic DIP
RM4227BD	-55°C to +125°C		8 Pin Ceramic DIP
RM4227BD/883[1]	-55°C to +125°C	Military	8 Pin Ceramic DIP

Note:

1. /883 suffix denotes MIl-STD-883, Par. 1.2.1 compliant device.

THIS PAGE INTENTIONALLY LEFT BLANK

RC4277

Dual Precision Operational Amplifier

Features

- High DC precision
- Very low VOS – 30 µV
- Very low VOS drift – 0.3 µV/°C
- High open-loop gain – 5000 V/mV
- High CMRR – 120 dB
- High PSRR – 120 db
- Low noise – 0.35 μV_{p-p} (0.1 Hz to 10 Hz)
- Low input bias current – 3.0 nA
- Low power consumption – 140 mW

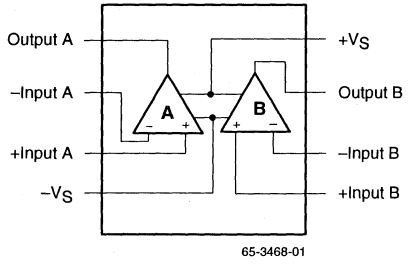
Description

The RC4277 provides the highest precision available in a dual bipolar operational amplifier. A monolithic dual version of the RC4077, the RC4277 is designed to replace OP-07 and OP-77 type amplifiers in applications requiring high PC board layout density. The RC4277 has a well-balanced, mutually supporting set of input specifications. Low V_{OS}, low I_B, high open-loop gain, and excellent matching characteristics combine to raise the performance level of many instrumentation, low-level signal conditioning, and data conversion applications. PSRR, CMRR, V_{OS} drift, and noise levels also support high precision operation.

The high performance of the RC4277 results from two innovative and unconventional manufacturing steps, plus careful circuit layout and design. The key steps are SiCr thin-film resistor deposition and post-package trimming of the input offset voltage characteristic. The low 75 µV max V_{OS} specification is maintained in high-volume production by way of the post-package trim procedure, where internal resistors are trimmed through the device input leads at the final test operation. Devices retain this low offset through the stability and accuracy of the trimmed thin-film resistors.

The RC4277 is available in 8-lead plastic and ceramic DIPs.

Block Diagram



Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±22	V
Input Voltage[2]				±22	V
Differential Input Voltage				30	V
Internal Power Dissipation[3]				500	mW
P_D T_A < 50°C	PDIP			468	mW
	CerDIP			833	
Output Short Circuit Duration		Indefinite			
Junction Temperature	PDIP			125	°C
	CerDIP			175	
Storage Temperature		-65		150	°C
Operating Temperature	RV4277	-25		85	°C
	RC4277	0		70	
Lead Soldering Temperature (60 sec)				300	°C
For T_A > 50°C Derate at	PDIP		6.25		mW/°C
	CerDIP		8.33		

Notes:

1. Functional operation under any of these conditions is NOT implied.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Observe package thermal characteristics.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		CerDIP		150		°C/W

Electrical Characteristics

(V_S = ±15V, and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage[3]			30	75	µV
Input Voltage Offset Match			25	150	µV
Long Term V_{OS} Stability[1]			0.3		µV/Mo
Input Offset Current			0.5	5.0	nA
Input Bias Current			±0.5	±5.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz		0.35		μV_{p-p}
Input Noise Voltage Density	F_O = 10 Hz		10.3		$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10		
	F_O = 1000 Hz		9.6		
Input Noise Current Density	F_O = 10 Hz		0.32		$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14		
	F_O = 1000 Hz		0.12		
Input Voltage Range[2, 4]		±11	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	110	132		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	110	132		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	1300	350		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		
	$R_L \geq 1k\Omega$	±11	±12		
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		V/µs
Closed Loop Bandwidth	A_{VCL} = +1.0		0.8		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		60	100	mW
Crosstalk		126	155		dB

Notes:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in VOS during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage	0°C ≤ T_A ≤ +70°C		50	120	µV
	-25°C ≤ T_A ≤ +85°C		50	135	
Average Input Offset Voltage Drift[2]			0.3	1.0	µV/°C
Input Offset Current			1.5	5.0	nA
Input Bias Current			±1.5	±5.0	nA
Input Voltage Range		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	110	124		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	110	124		dB
Large Signal Voltage Gain	R_L > 2kΩ, V_{OUT} = ±10V	1300	3000		V/mV
Output Voltage Swing	R_L > 2kΩ	±11	±12.6		V
Power Consumption	R_L = ∞		70	120	mW

Notes:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.

Typical Applications

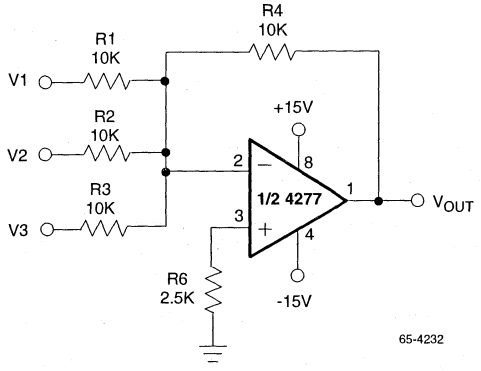


Figure 1. Adjustment-Free Precision Summing Amplifier

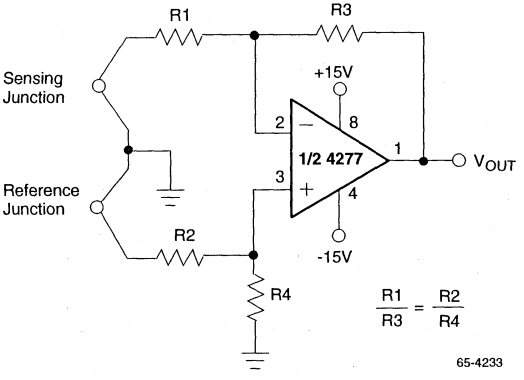


Figure 2. High Stability Thermocouple Amplifier

Typical Applications (continued)

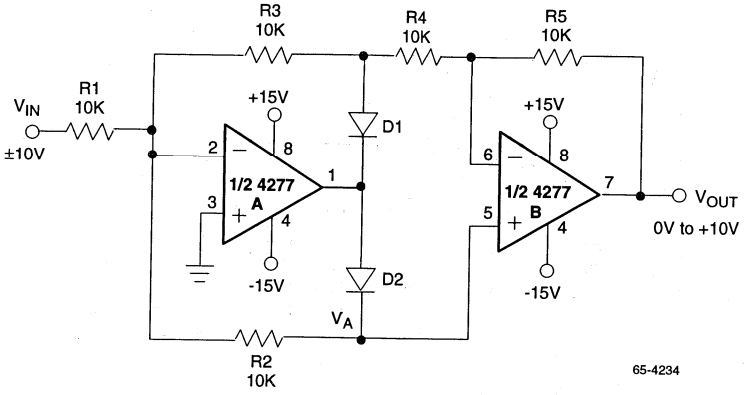
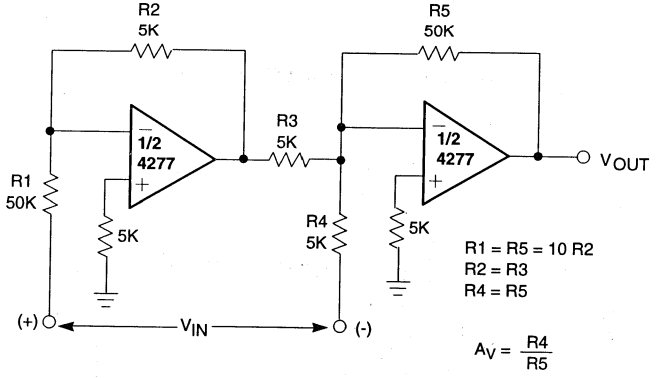


Figure 3. Precision Absolute Value Circuit



Note: This circuit can tolerate input voltages that exceed the 4277's supply voltage rating as long as the slew rate do not exceed the op amp's slew rate.

Figure 4. High Voltage Differential Amplifier

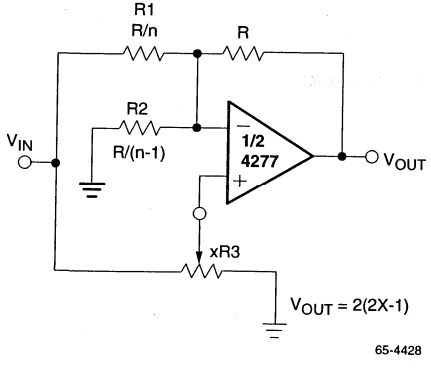


Figure 5. Polarity Changing Gain Controlled Amplifier

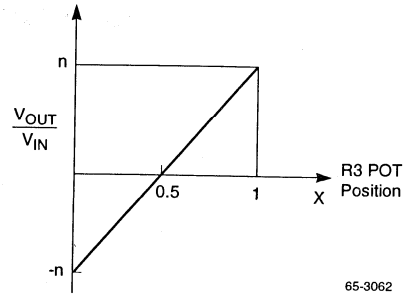


Figure 6. Gain Controlled Amplifier Transfer Function

Typical Applications (continued)

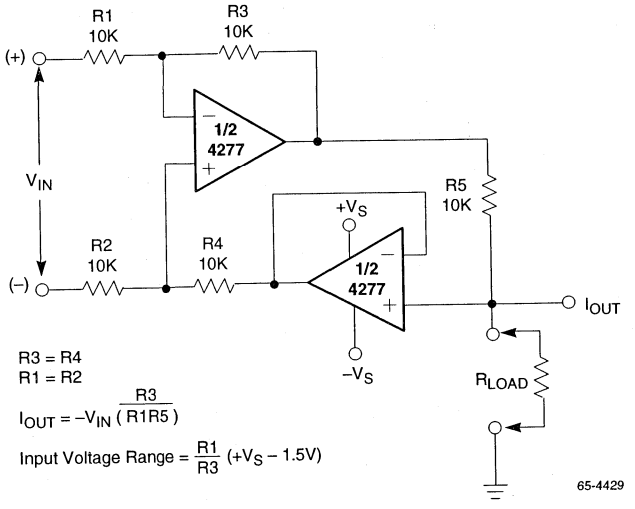


Figure 7. Differential Input Current Source

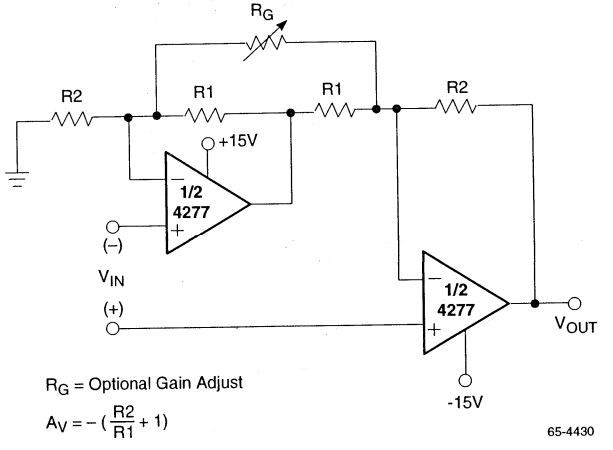


Figure 8. High Input Impedance Subtractor

Typical Applications (continued)

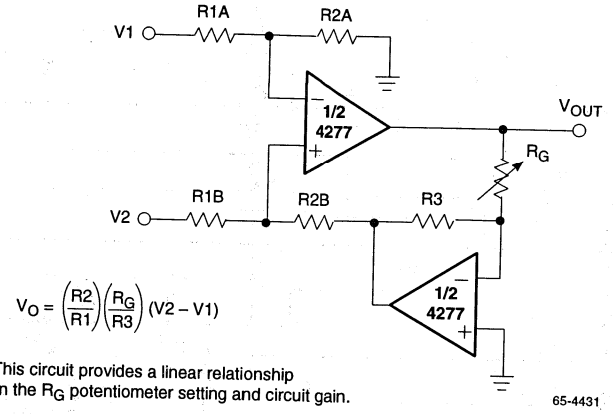


Figure 9. Difference Amplifier with Linear Gain Control

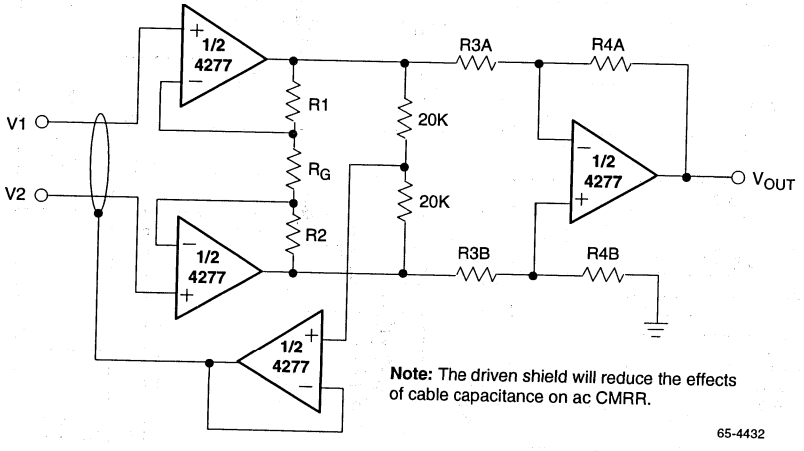
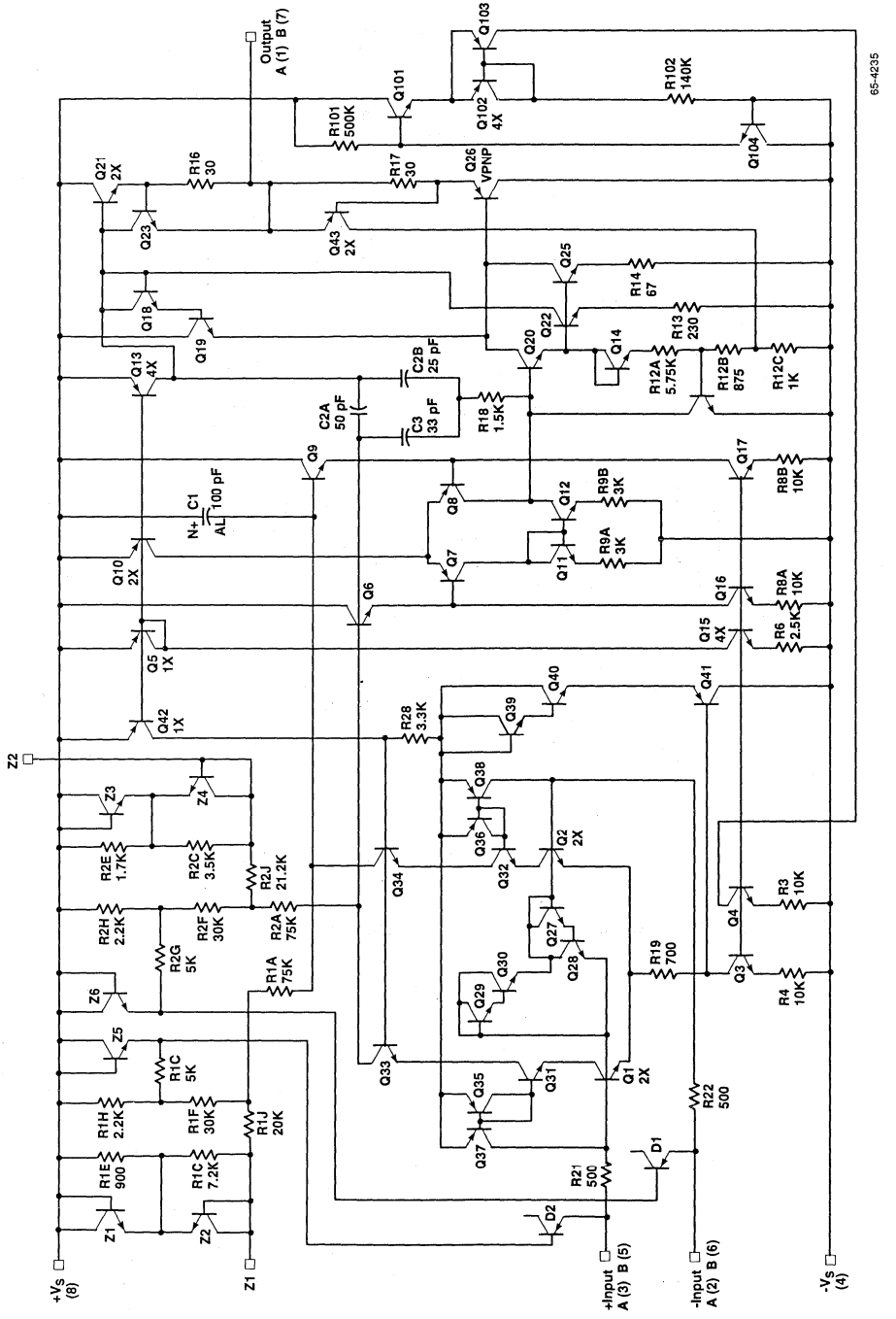


Figure 10. Three Op Amp Instrumentation Amplifier with Driven Shield

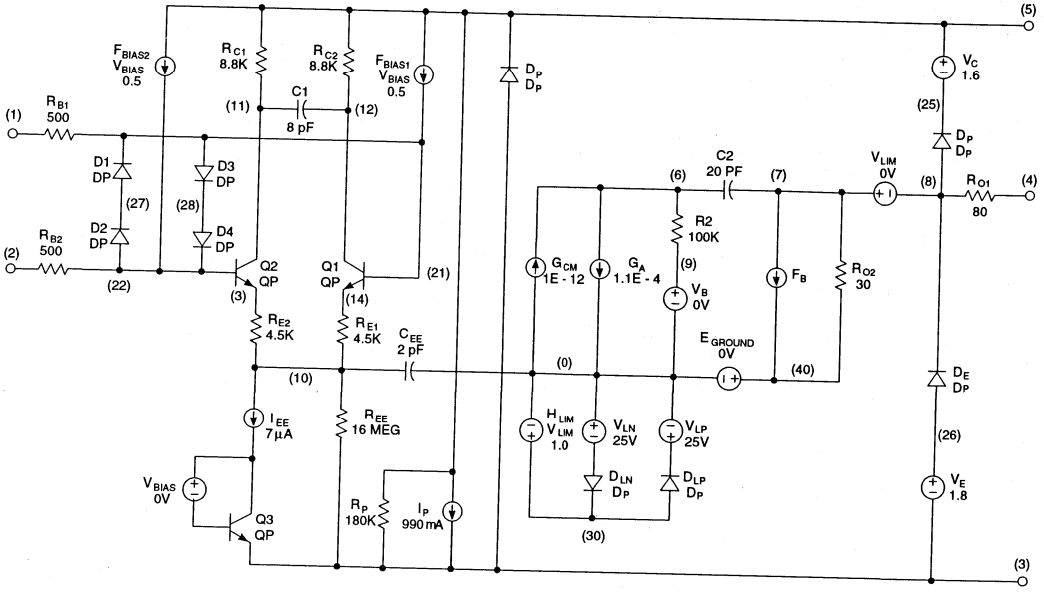
Schematic Diagram



One Section of Two

RM4277 SPICE Macro Model

This circuit models AC and DC characteristics including slew rate, bandwidth, V_{OS}, I_B, I_{OS}, CMRR, output voltage range, and gain. The circuit produces typical values for these parameters.



65-4447

Ordering Information

Product Number	Temperature Range	Screening	Package
RC4277FN	0°C to +70°C	Commercial	8 Pin Plastic DIP
RV4277FD	0°C to 70°C	Commercial	8 Pin Ceramic DIP

RC4558

Dual High-Gain Operational Amplifier

Features

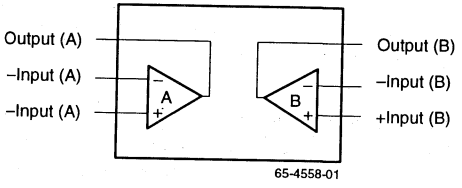
- 2.5 MHz unity gain bandwidth
- Supply voltage ±22V for RM4558 and ±18V for RC/RV4558
- Short-circuit protection
- No frequency compensation required
- No latch-up
- Large common-mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

Description

The RC4558 integrated circuit is a dual high-gain operational amplifier internally compensated and constructed on a single silicon IC using an advanced epitaxial process.

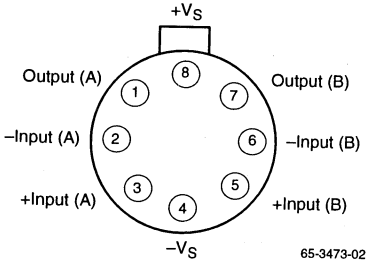
Combining the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of this dual device in dense single 741 operational amplifier applications. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

Block Diagram

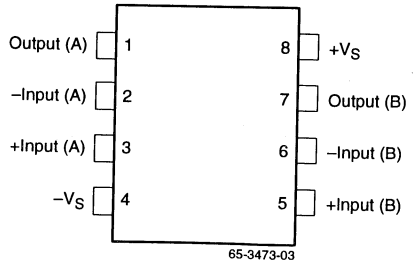


65-4558-01

Pin Assignments



65-3473-02



65-3473-03

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage	RM4558			±22	V
	RC4558			±18	
Input Voltage[2]				±15	V
Differential Input Voltage				30	V
$P_D T_A$ < 50°C	SOIC			300	mW
	PDIP			468	
	CerDIP			833	
	TO-99			658	
Junction Temperature	SOIC, PDIP			125	°C
	CerDIP, TO-99			175	
Operating Temperature	RM4558	-55		125	°C
	RC4558	0		70	
Lead Soldering Temperature	PDIP, CerDIP, TO-99 (60 sec)			300	°C
	SOIC (10 sec)			260	
Output Short Circuit Duration[3]		Indefinite			

Notes:

1. Functional operation under any of these conditions is NOT implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground on one op amp only. Rating applies to +75°C ambient temperature.

Matching Characteristics

(V_S = ±15V, T_A = +25°C unless otherwise specified)

Parameter	Test Conditions	Typ	Units
Voltage Gain	$R_L \geq 2$ kΩ	±1.0	dB
Input Bias Current	$R_L \geq 2$ kΩ	±15	nA
Input Offset Current	$R_L \geq 2$ kΩ	±7.5	nA

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise specified)

Parameters	Test Conditions	RM4558			RC4558			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	100		76	100		dB
Power Consumption	R_L = ∞		100	170		100	170	mW
Transient Response	V_{IN} = 20 mV							
Rise Time	$R_L = 2k\Omega$		0.3			0.3		µS
Overshoot	$C_L \leq 100pF$		35			35		%
Slew Rate	$R_L \geq 2k\Omega$		0.8			0.8		V/µS
Channel Separation	F = 10kHz, R_S = 1kΩ		90			90		dB
Unity Gain Bandwidth (Gain = 1)		2.5	3.0		2.0	3.0		MHz

The following specifications apply for RM = -55°C ≤ T_A ≤ +125°C, RC = 0° ≤ T_A ≤ +70°C

Parameters	Test Conditions	RM4558			RC4558			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current RC4558				500			300	nA
Input bias Current RC4558				1500			800	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Power Consumption	R_L = ∞		120	200		120	200	mW

Typical Performance Characteristics

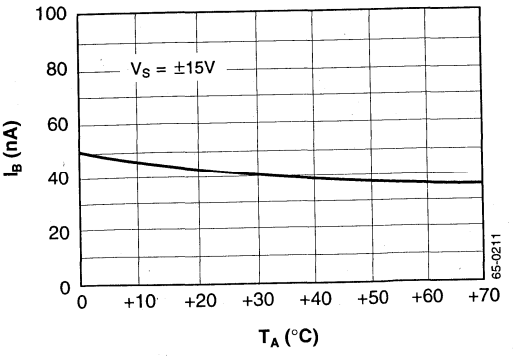


Figure 1. Input Bias Current vs. Temperature

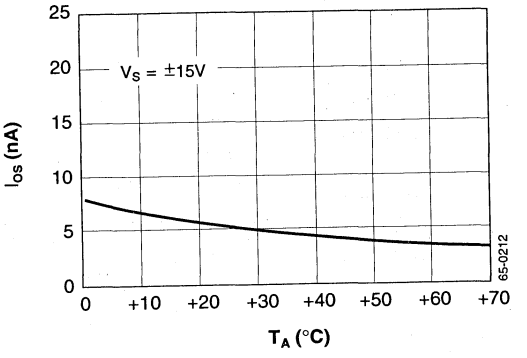


Figure 2. Input Offset Current vs. Temperature

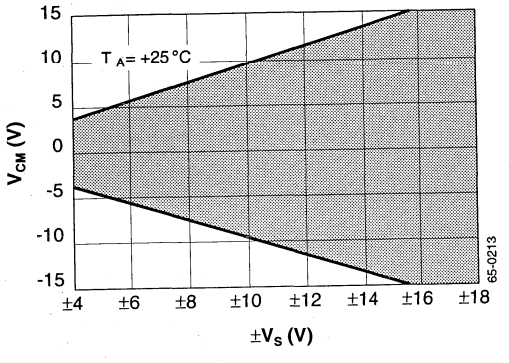


Figure 3. Input Common Mode Voltage Range vs. Supply Voltage

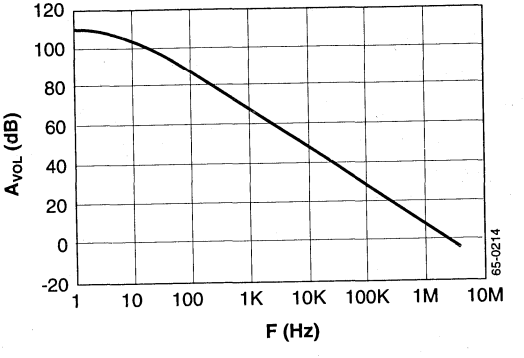


Figure 4. Open Loop Voltage Gain vs. Frequency

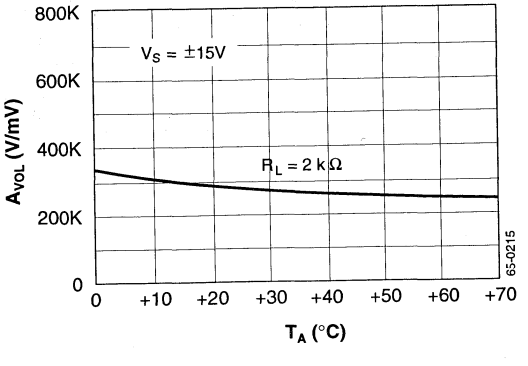


Figure 5. Open Loop Voltage Gain vs. Temperature

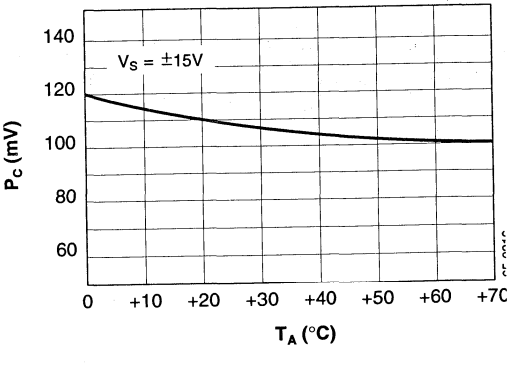


Figure 6. Power Consumption vs. Temperature

Typical Performance Characteristics (continued)

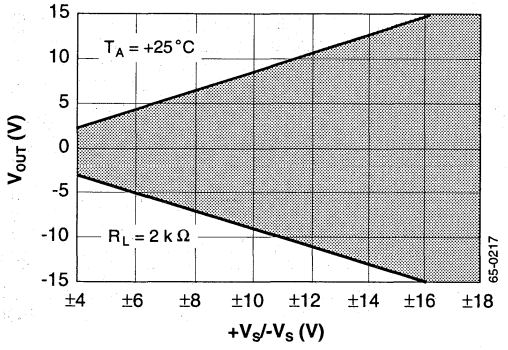


Figure 7. Output Voltage Swing vs. Supply Voltage

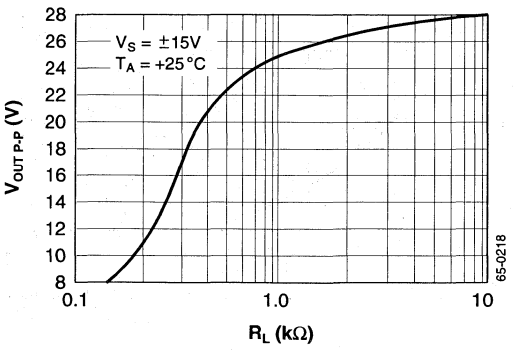


Figure 8. Output Voltage Swing vs. Load Resistance

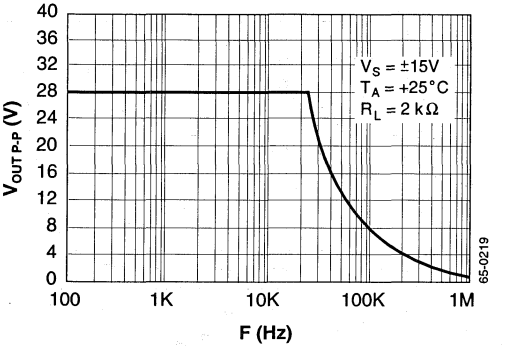


Figure 9. Output Voltage Swing vs. Freqeuncy

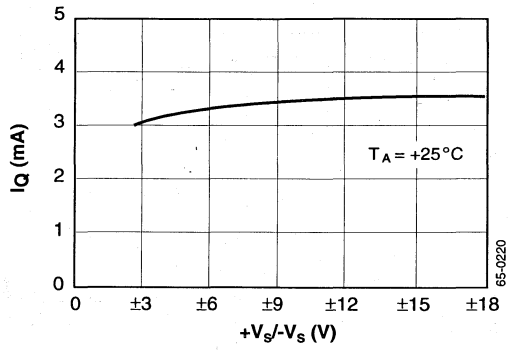


Figure 10. Quiescent Current vs. Supply Voltage

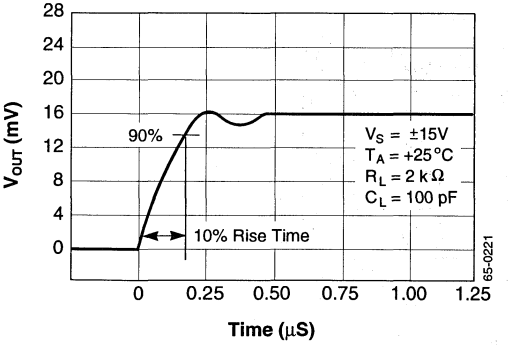


Figure 11. Transient Response Output Voltage vs. Time

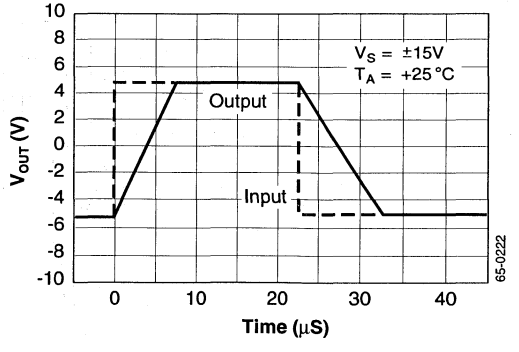


Figure 12. Follower Large Signal Pulse Response Output Voltage vs. Time

Typical Performance Characteristics (continued)

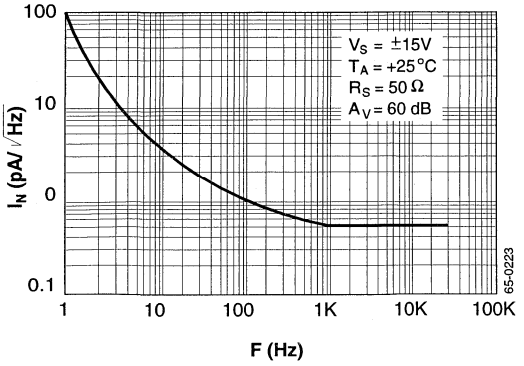


Figure 13. Input Noise Current Density vs. Frequency

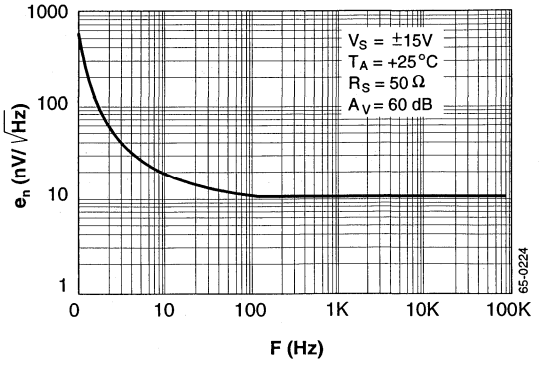


Figure 14. Input Noise Voltage Density vs. Frequency

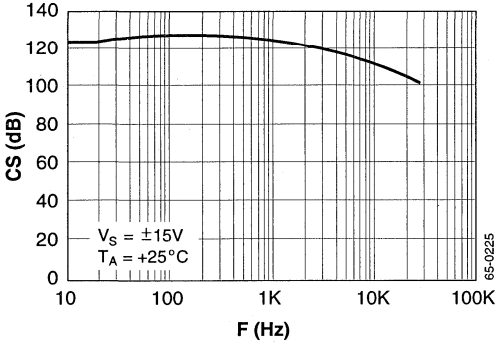


Figure 15. Channel Separation vs. Frequency

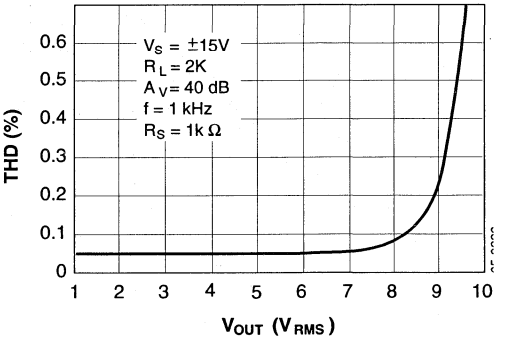


Figure 16. Total Harmonic Distortion vs Output Voltage

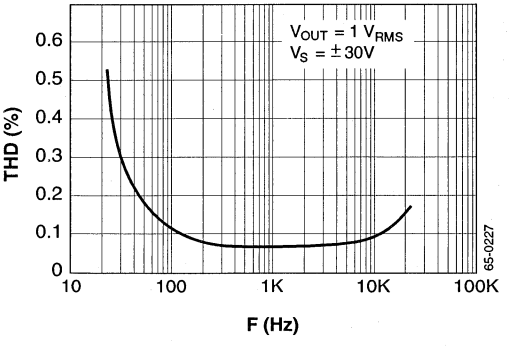


Figure 17. Distortion vs. Frequency

Typical Applications

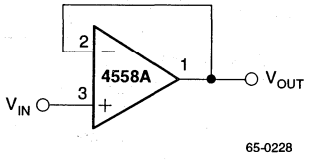


Figure 18. Voltage Follower

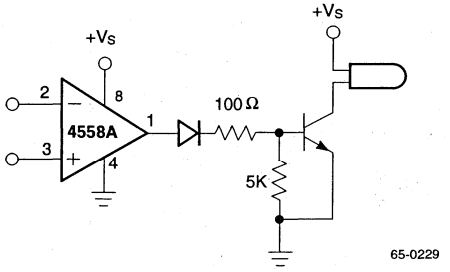


Figure 19. Lamp Driver

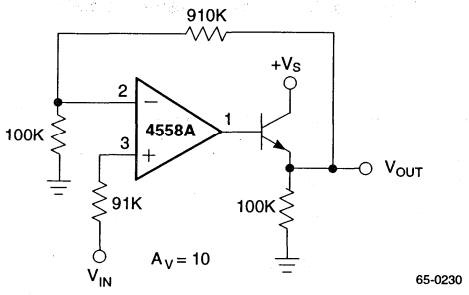


Figure 20. Power Amplifier

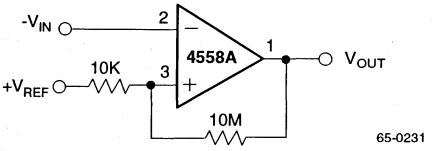


Figure 21. Comparator With Hysteresis

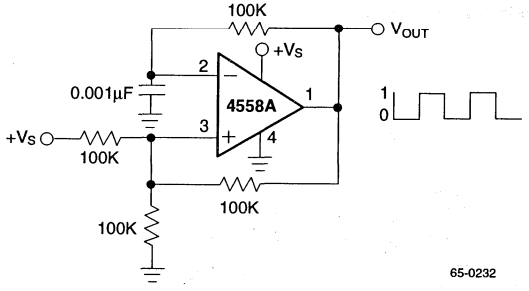


Figure 22. Squarewave Oscillator

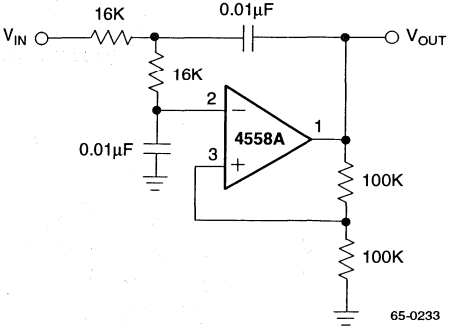


Figure 23. DC Coupled 1kHz Low-Pass Active Filter

Typical Applications (continued)

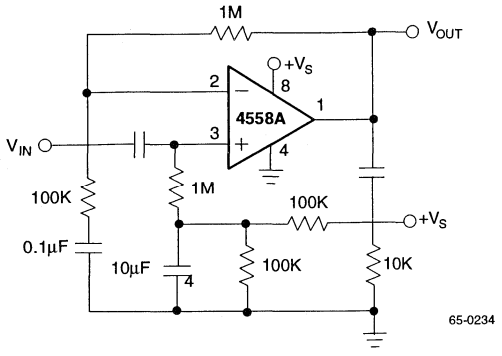


Figure 24. AC Coupled Non-Inverting Amplifier

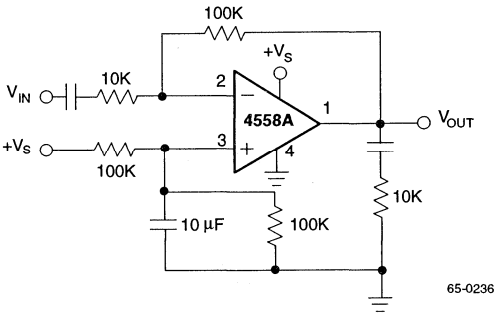


Figure 25. AC Coupled Inverting Amplifier

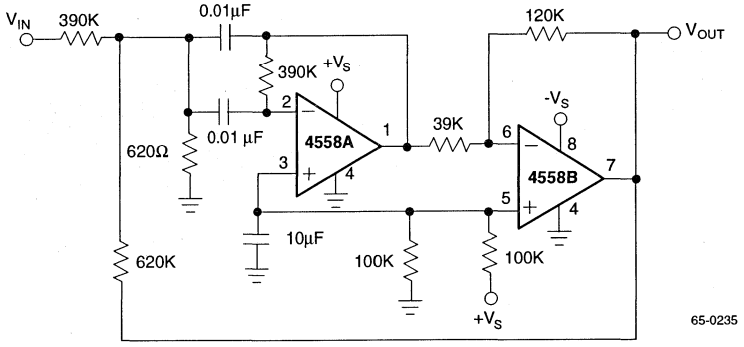


Figure 26. 1kHz Bandpass Active Filter

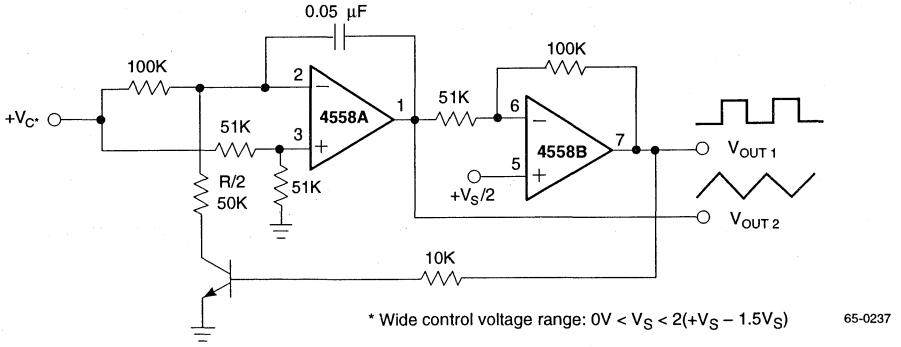
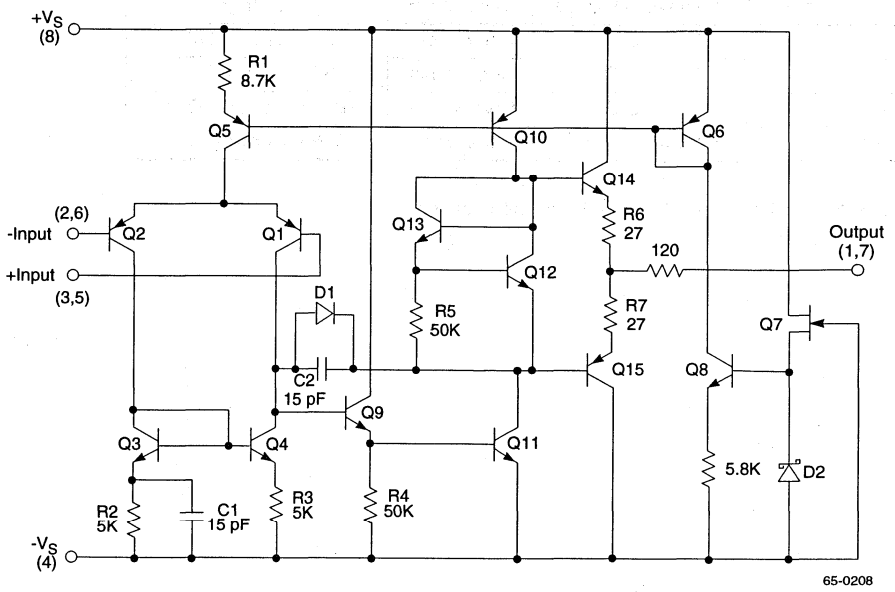


Figure 27. Voltage Controlled Oscillator (VCO)

Simplified Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package
RC4558M	0° to 70°C	Commercial	8 Pin Wide SOIC
RC4558N	0° to 70°C	Commercial	8 Pin Plastic DIP
RM4558D	0° to 70°C	Commercial	8 Pin Ceramic DIP
RM4558D/883B	-55°C to +125°C	Military	8 Pin Ceramic DIP

Note:

1. /883B suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

RC4559

Dual High-Gain Operational Amplifier

Features

- Unity gain bandwidth – 4.0 MHz
- Slew rate – 2.0 V/μS
- Low noise voltage – 1.4 μVRMS
- Supply voltage – ±22V for RM4559 and ±18V for RC4559
- No frequency compensation required
- No latch up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

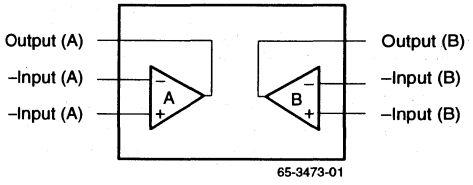
Description

The RC4559 integrated circuit is a high performance dual operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

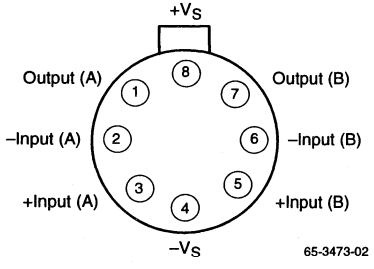
These amplifiers feature improved AC performance which far exceeds that of the 741-type amplifiers. The specially designed low-noise input transistors allow the RC4559 to be used in low-noise signal processing applications such as audio preamplifiers and signal conditioners.

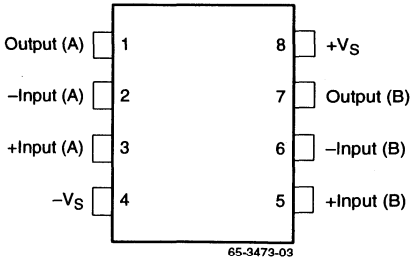
The RC4559 also has more output drive capability than 741-type amplifiers and can be used to drive a 600Ω load.

Block Diagram



Pin Assignments





Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage	RM4559			±22	V
	RC4559			±18	
Input Voltage[2]				±15	V
Differential Input Voltage				30	V
$P_D T_A$ < 50°C	SOIC			300	mW
	PDIP			468	
	CerDIP			833	
	TO-99			658	
Junction Temperature	SOIC, PDIP			125	°C
	CerDIP, TO-99			175	
Operating Temperature	RM4559	-55		125	°C
	RC4559	0		70	
Lead Soldering Temperature	PDIP, CerDIP, T0-99 (60 sec)			300	°C
	SOIC (10 sec)			260	
Output Short Circuit Duration[3]		Indefinite			

Notes:

1. Functional operation under any of these conditions is NOT implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground on one op amp only. Rating applies to +75°C ambient temperature.

Matching Characteristics

(V_S = ±15V, T_A = +25°C unless otherwise specified)

Parameter	Test Conditions	Typ	Units
Voltage Gain	$R_L \geq 2$ kΩ	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise specified)

Parameters	Test Conditions	RM4559			RC4559			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5.0	100		5.0	100	nA
Input Bias Current			40	250		40	250	nA
Input Resistance (Differential Mode)		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		
	$R_L \geq 600\Omega$	±9.5	±10		±9.5	±10		
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	100		80	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	82	100		82	100		dB
Supply Current	$R_L = \infty$		3.3	5.6		3.3	5.6	mA
Transient Response								
Rise Time	V_{IN} = 20 mV, $R_L = 2k\Omega$		80			80		µS
Overshoot	$C_L \leq 100pF$		35			35		%
Slew Rate		1.5	2.0		1.5	2.0		V/µS
Unity Gain Bandwidth		3.0	4.0		3.0	4.0		MHz
Power Bandwidth	$V_{OUT} = 20V_{p-p}$	24	32		24	32		kHz
Input Noise Voltage[1]	F=20Hz to 20kHz		1.4	5.0		1.4	5.0	μV_{RMS}
Input Noise Current	F=20Hz to 20kHz		25			25		pA_{RMS}
Channel Separation	Gain = 100, F = 10kHz, R_S = 1kΩ		90			90		dB
The following specifications apply for RM = -55°C ≤ T_A ≤ +125°C, RC = 0° ≤ T_A ≤ +70°C								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current				300			200	nA
Input Bias Current				500			300	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Supply Current	$R_L = \infty$		4.0	6.6		4.0	6.6	mA

Note:

1. Sample tested only.

Typical Performance Characteristics

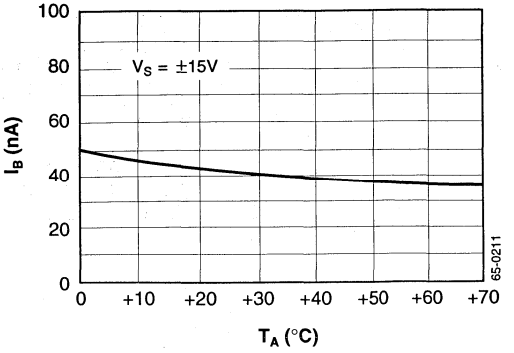


Figure 1. Input Bias Current vs. Temperature

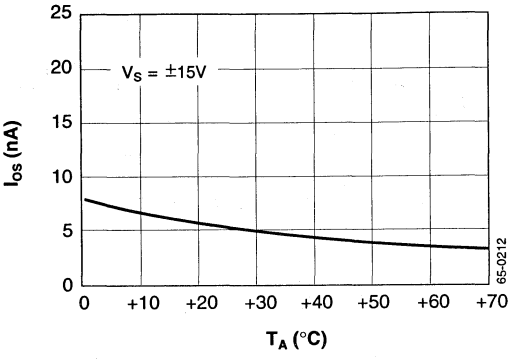


Figure 2. Input Offset Current vs. Temperature

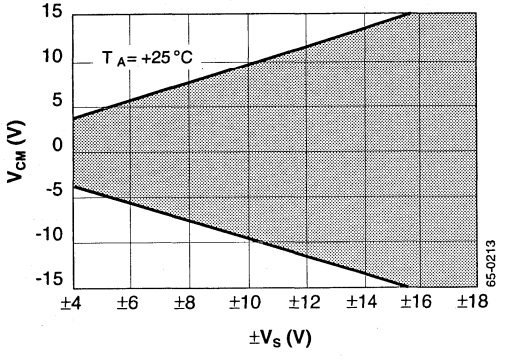


Figure 3. Input Common Mode Voltage Range vs. Supply Voltage

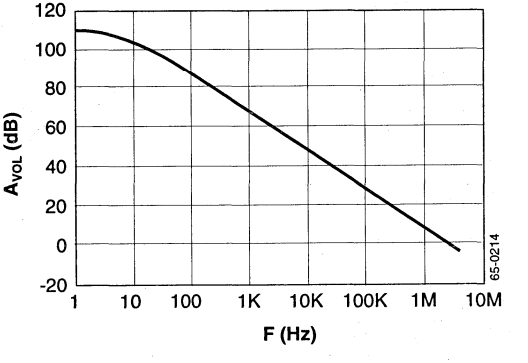


Figure 4. Open Loop Gain Voltage vs. Frequency

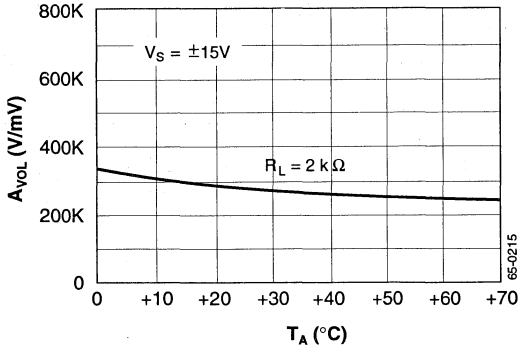


Figure 5. Open Loop Voltage Gain vs. Temperature

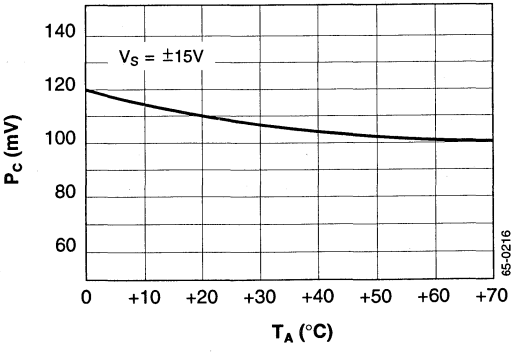


Figure 6. Power Consumption vs. Temperature

Typical Performance Characteristics (continued)

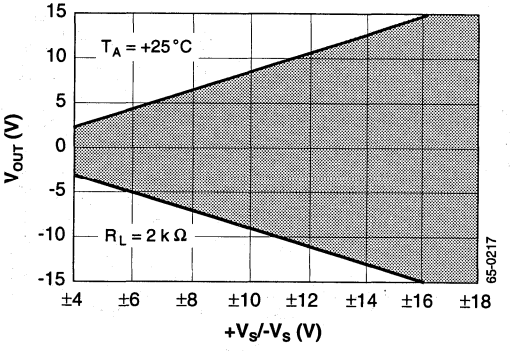


Figure 7. Output Voltage SWing vs. Supply Voltage

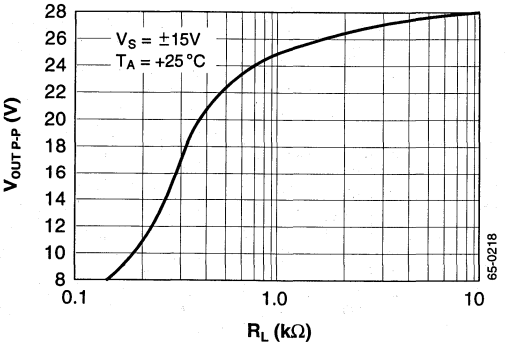


Figure 8. Output Voltage Swing vs. Load Resistance

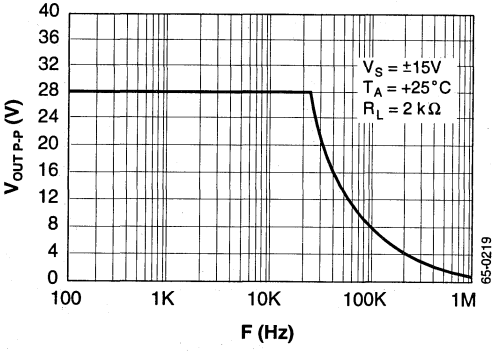


Figure 9. Output Voltage Swing vs. Frequency

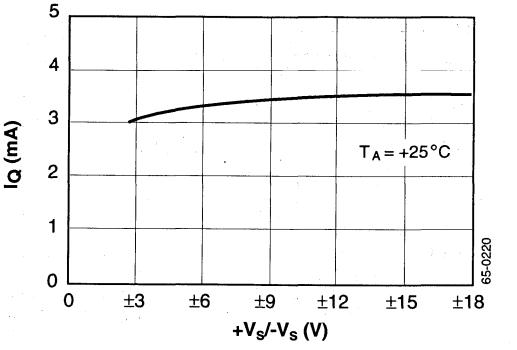


Figure 10. Quiescent Current vs. Supply Voltage

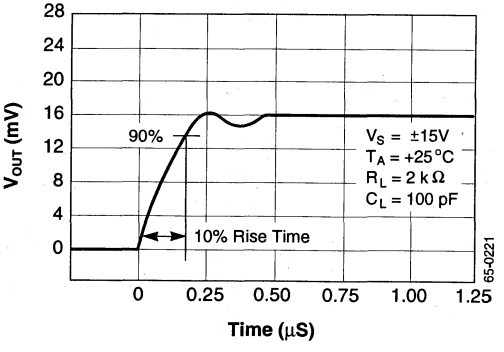


Figure 11. Transient Response Output Voltage vs. Time

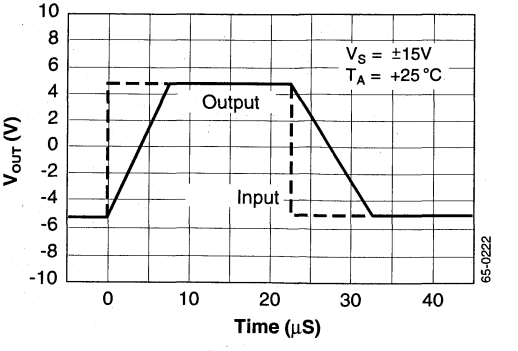


Figure 12. Follower Large Signal Pulse Response Output Voltage vs. Time

Typical Performance Characteristics (continued)

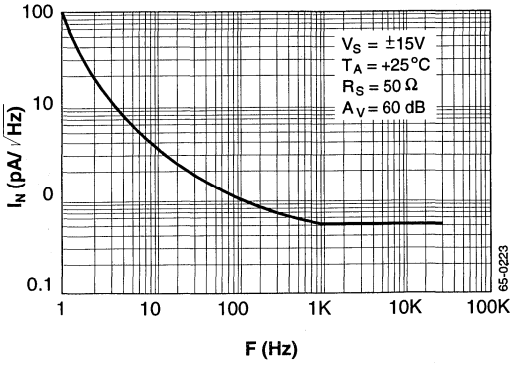


Figure 13. Input Noise Current Density vs. Frequency

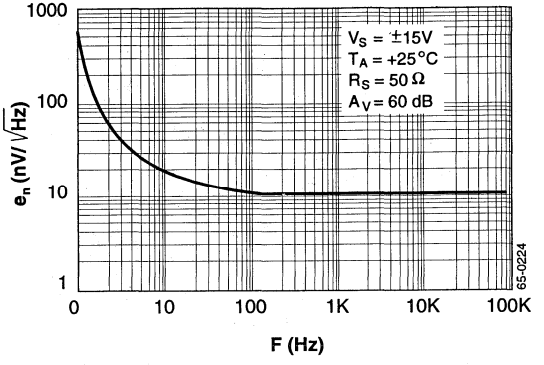


Figure 14. Input Noise Voltage Density vs. Frequency

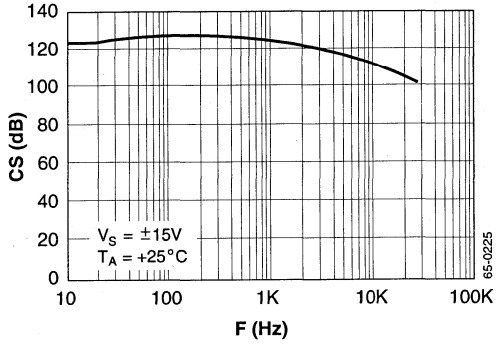


Figure 15. Channel Separation vs. Frequency

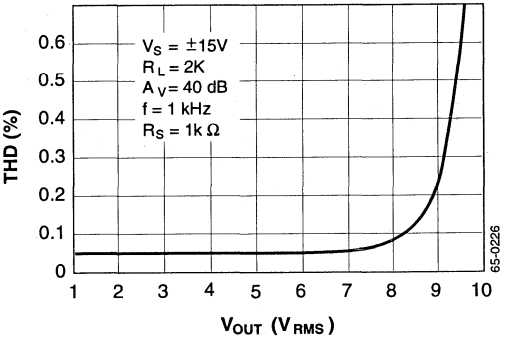


Figure 16. Total Harmonic Distortion vs. Output Voltage

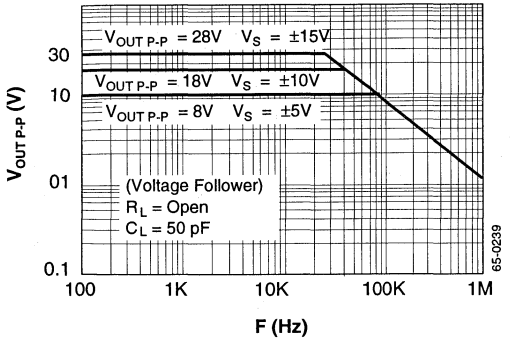


Figure 17. Output Voltage Swing vs. Frequency

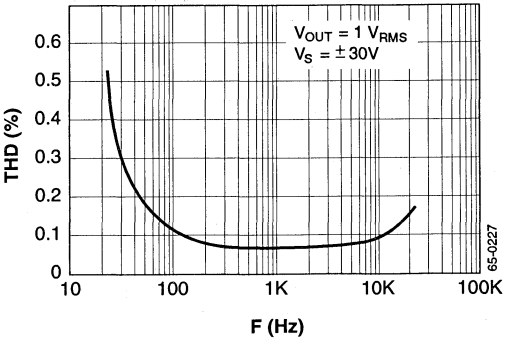


Figure 18. Distortion vs. Frequency

Typical Applications

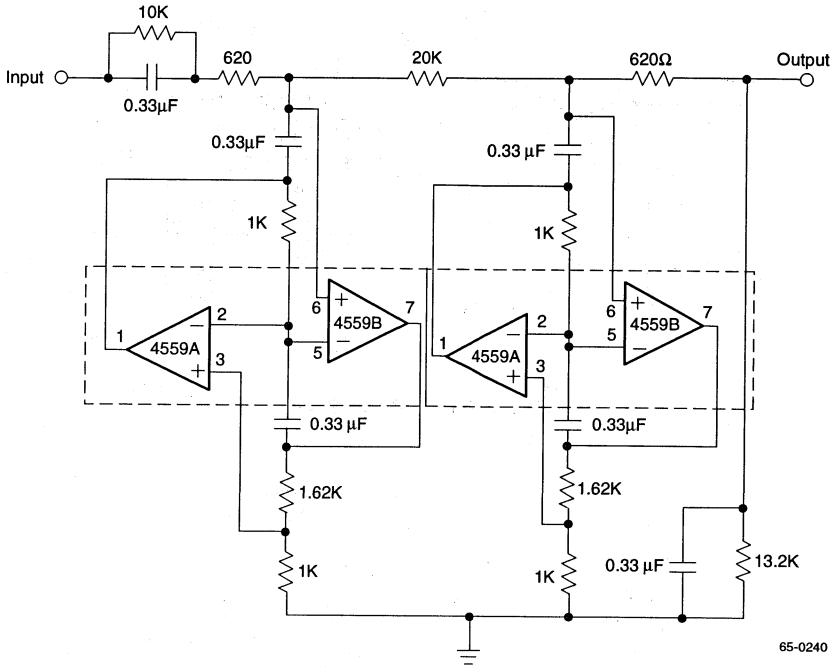


Figure 19. 400Hz Lowpass Butterworth Active Filter

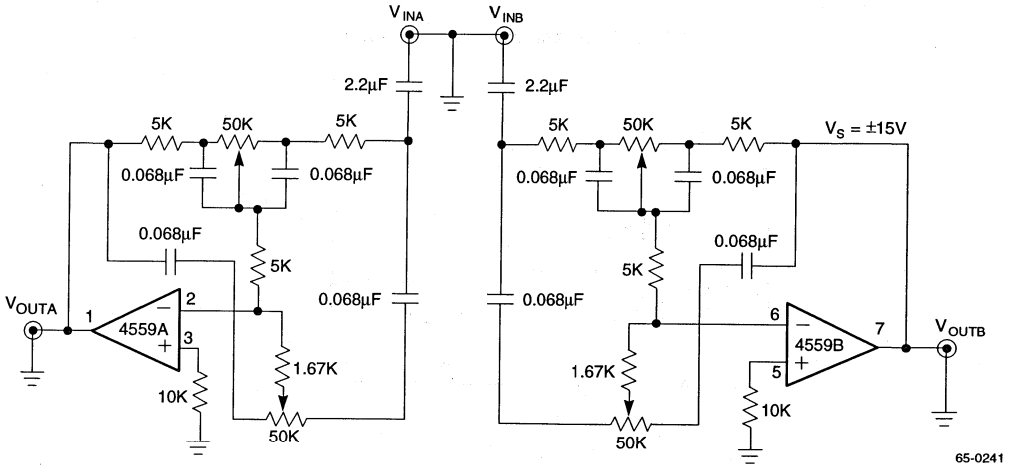


Figure 20. Stereo Tone Control

Typical Applications (continued)

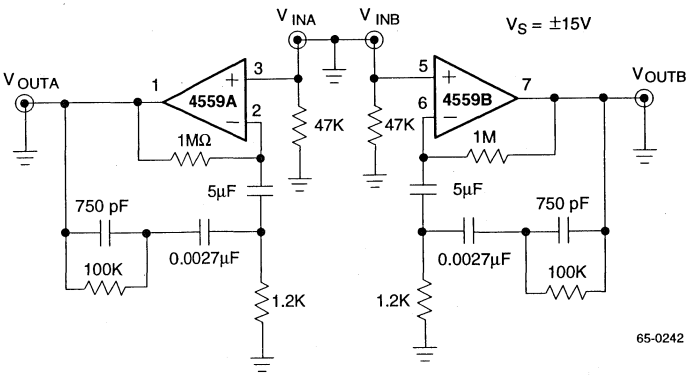


Figure 21. RIAA Preamplifier

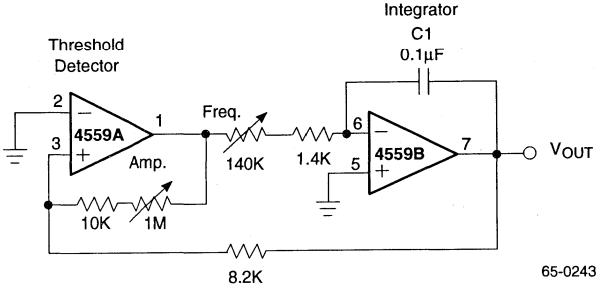


Figure 22. Triangular-Wave Generator

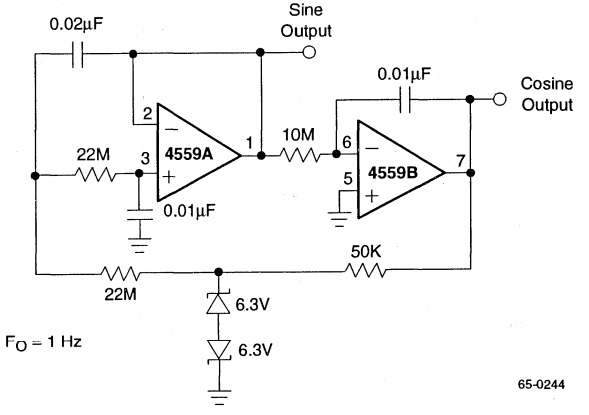
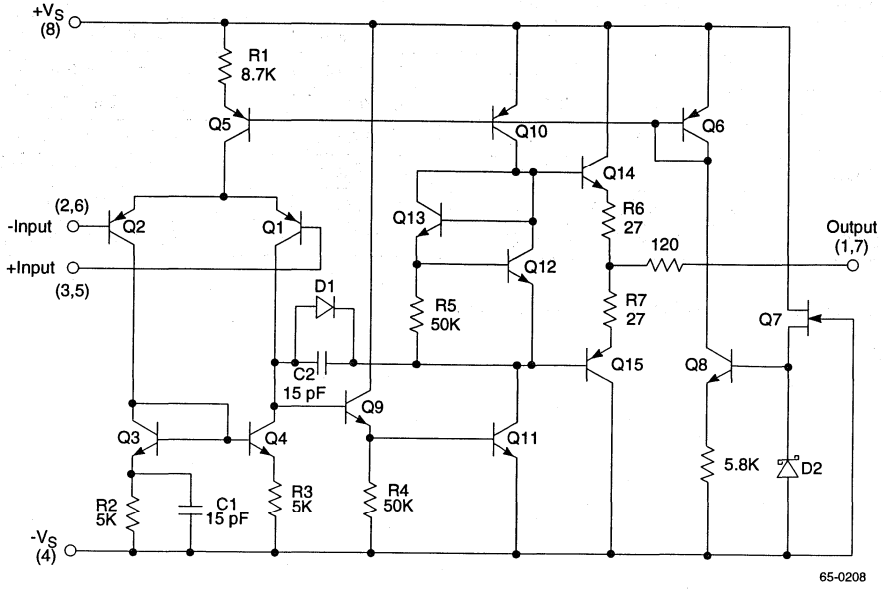


Figure 23. Low Frequency Sine Wave Generator with Quadrature Output

Simplified Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package
RC4559M	0° to 70°C	Commercial	8 Pin Wide SOIC
RC4559N	0° to 70°C	Commercial	8 Pin Plastic DIP
RC4559D	0° to 70°C	Commercial	8 Pin Ceramic DIP
RM4559D	-55°C to +125°C	Commercial	8 Pin Ceramic DIP
RM4559D/883B	-55°C to +125°C	Military	8 Pin Ceramic DIP
RM4559T	-55°C to +125°C	Commercial	8 Pin TO-99 Metal Can
RM4559T/883B	-55°C to +125°C	Military	8 Pin TO-99 Metal Can

Note:

1. /883B suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

RC5532/RC5532A

High Performance Dual Low Noise Operational Amplifier

Features

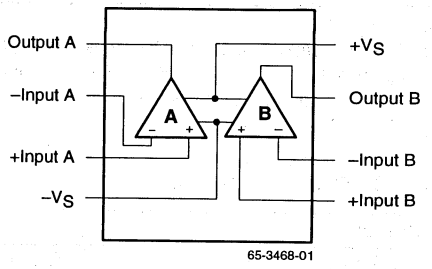
- Small signal bandwidth – 10 MHz
- Output drive capability – 600Ω, 10 VRMS
- Input noise voltage – 5 nV/√Hz
- DC voltage gain – 50,000
- AC voltage gain – 2200 at 10 kHz
- Power bandwidth – 140 kHz
- Slew rate – 8 V/μS
- Large supply voltage range – ±3V to ±20V

Description

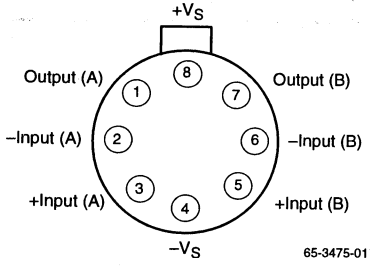
The RC5532 is a high performance, dual low noise operational amplifier. Compared to standard dual operational amplifiers, such as the RC747, it shows better noise performance, improved output drive capability, and considerably higher small-signal and power bandwidths.

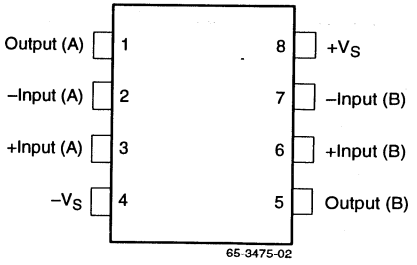
This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation, control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the RC5532A version be used which has guaranteed noise specifications.

Block Diagram



Pin Assignments





Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±22	V
Input Voltage				$\pm V_S$	V
Differential Input Voltage				0.5	V
$P_D T_A$ < 50°C	PDIP			468	mW
	CerDIP			833	
	SOIC			658	
Junction Temperature	PDIP			125	°C
	CerDIP, TO-99			175	
Storage Temperature		-65		150	°C
Operating Temperature	RM5532/A	-55		125	°C
	RC5532/A	0		70	
Lead Soldering Temperature (10 sec)				300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit to ground on one amplifier only.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
		TO-99		50		
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		CerDIP		150		
		TO-99		190		
For T_A > 50°C Derate at		PDIP		6.25		mW/°C
		CerDIP		8.33		
		TO-99		5.26		

DC Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RM5532/5532A			RC5532/5532A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			0.5	2.0		0.5	4.0	mV
	Over Temperature			3.0			5.0	mV
Input Offset Current				100		10	150	nA
	Over Temperature			200			200	nA
Input Bias Current			200	400		200	800	nA
	Over Temperature			700			1000	nA
Supply Current			6.0	11		6.0	16	mA
	Over Temperature			13			22	mA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio		80	100		70	100		dB
Power Supply Rejection Ratio		86	100		80	100		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	50			25	100		V/mV
	Over Temperature	25			15	50		
	$R_L \geq 600\Omega$, V_{OUT} = ±10V	40			15	50		
	Over Temperature	20			10			
Output Voltage Swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
	R_L = 600Ω, V_S = ±18V	±15	±16		±15	±16		
	$R_L \geq 2k\Omega$	±12	±13					
Input Resistance (Diff. Mode)			300			300		kΩ
Short Circuit Current			38			38		mA

Notes:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum input current should be limited to±10mA.
2. Over Temperature: RM = 55 °C ≤ T_A ≤ 125°C; RC = 0°C ≤ T_A ≤70°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C)

Parameters	Test Conditions	RC/RM5532			RC/RM5532A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Noise Voltage Density	F_O = 30 Hz		8.0			8.0	12	nV/√Hz
	F_O = 1 kHz		5.0			5.0	6.0	
Input Noise Current Density	F_O = 30 Hz		2.7			2.7		pA/√Hz
	F_O = 1 kHz		0.7			0.7		
Channel Separation	F = 1 kHz, R_S = 5 kΩ		110			110		dB

AC Electrical Characteristics

(V_S = ±15V and T_A = +25°C)

Parameters	Test Conditions	Min	Typ	Max	Units
Output Resistance	A_V = 30 dB Closed Loop, F = 10 kHz, R_L = 600Ω		0.3		Ω
Overshoot	Unity Gain, V_{IN} = 100 mV_{p-p} C_L = 100 pF, R_L = 600Ω		10		%
Gain	F = 10 kHz		2.2		V/mV
Gain Bandwidth Product	C_L = 100 pF, R_L = 600Ω		10		MHz
Slew Rate			8.0		V/µS
Power Bandwidth	V_{OUT} = ±10V		140		kHz
	V_{OUT} = ±14V, R_L = 600Ω, V_S = ±18V		100		kHz

Test Circuits

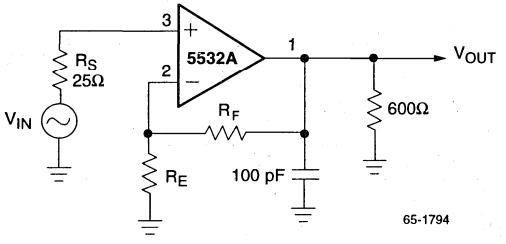


Figure 1. Closed Loop Frequency Response

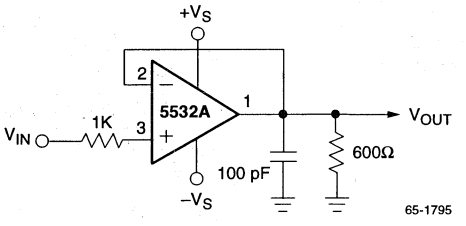


Figure 2. Follower, Transient Response

Typical Performance Characteristics

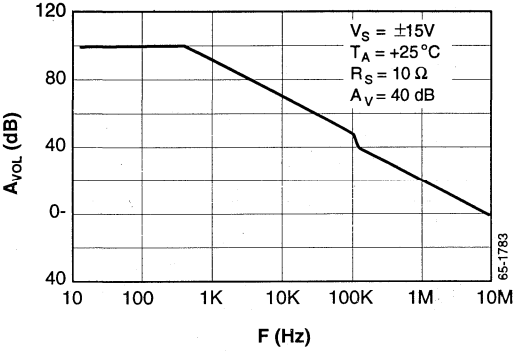


Figure 3. Open Loop Gain vs. Frequency

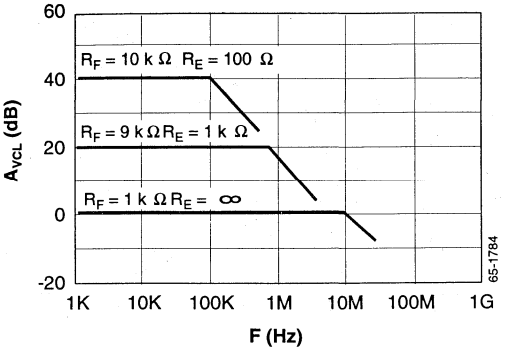


Figure 4. Closed Loop Gain vs. Frequency

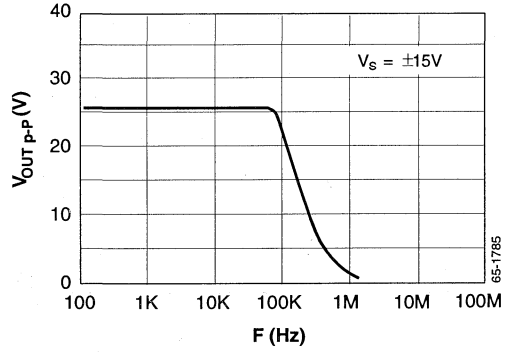


Figure 5. Output Voltage Swing vs. Frequency

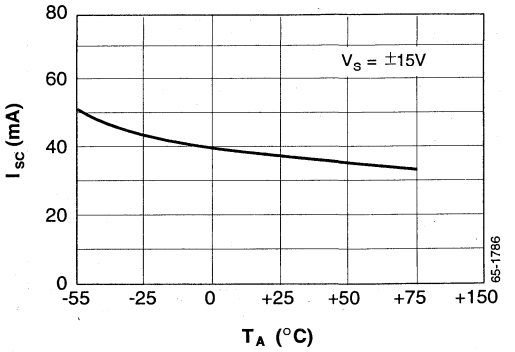


Figure 6. Short Circuit Current vs. Temperature

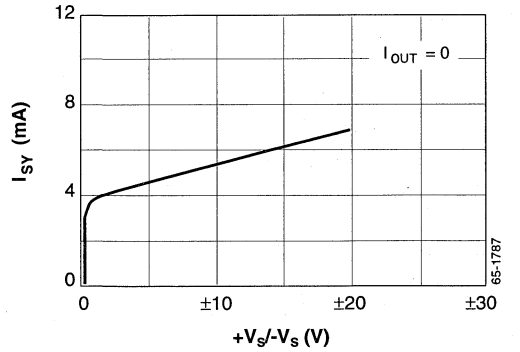


Figure 7. Supply Current vs. Supply Voltage

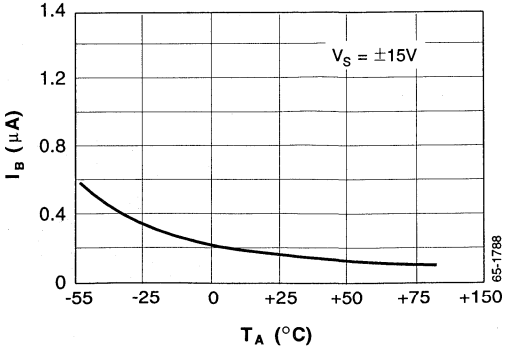


Figure 8. Input Bias Current vs. Temperature

Typical Performance Characteristics (continued)

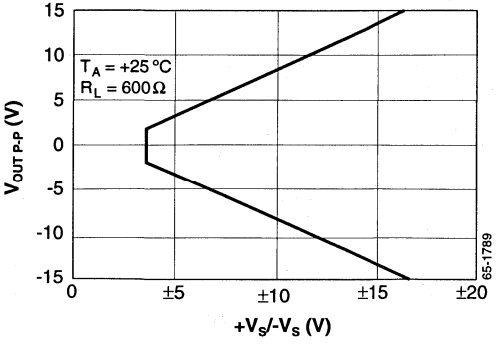


Figure 9. Output Voltage Swing vs. Supply Voltage

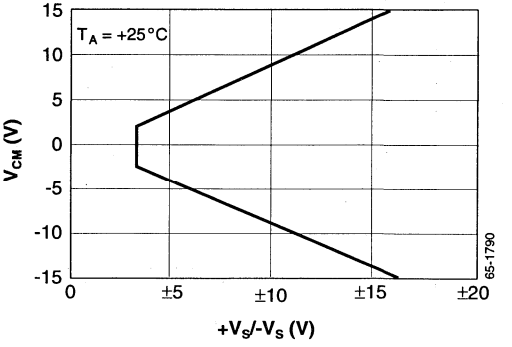


Figure 10. Common Mode Input Range vs. Supply Voltage

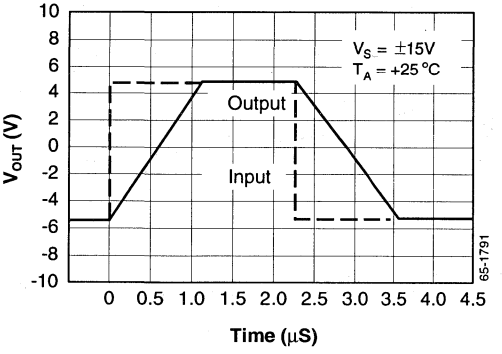


Figure 11. Follower Large Signal Pulse Response

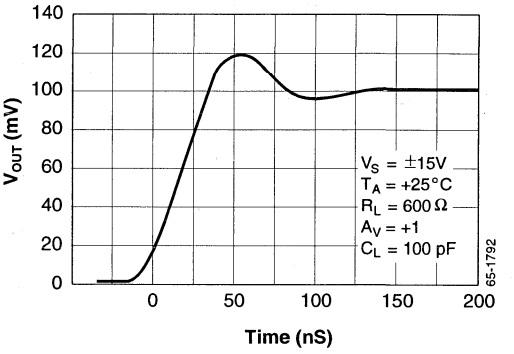


Figure 12. Transient Response Output Voltage vs. Time

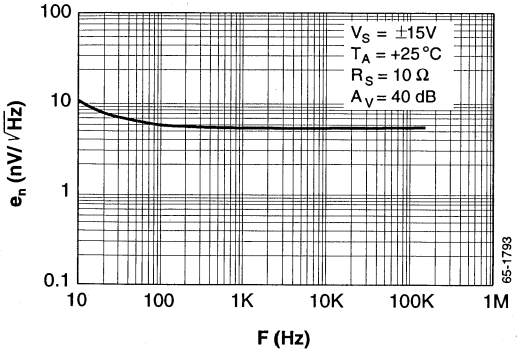
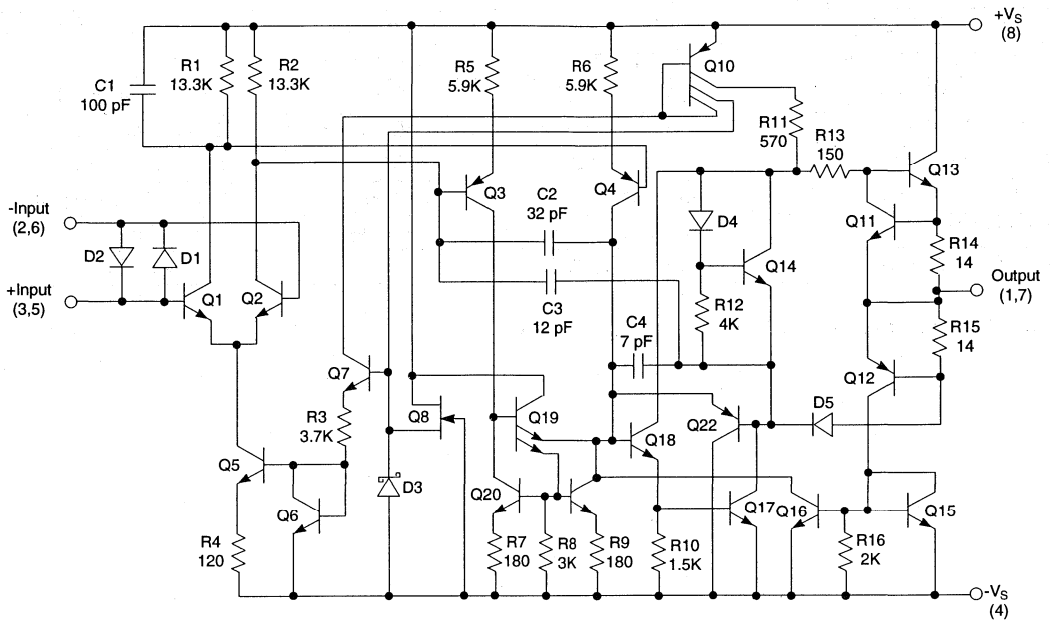


Figure 13. Input Noise Density vs. Frequency

Simplified Schematic Diagram (1/2 shown for 5532)



Ordering Information

Product Number	Temperature Range	Screening	Package
RC5532D/RC5532AD	0°C to +70°C	Commercial	8 Pin Ceramic DIP
RC5532N/RC5532AN	0°C to +70°C	Commercial	8 Pin Plastic DIP
RM5532D/RM5532AD	-55°C to +125°C	Commercial	8 Pin Ceramic DIP
RM5532D/883B	-55°C to +125°C	Military	8 Pin Ceramic DIP
RM5532AD/883B	-55°C to +125°C	Military	8 Pin Ceramic DIP
RM5532T/RM5532AT	-55°C to +125°C	Commercial	8 Pin TO-99 Metal Can
RM5532T/883B	-55°C to +125°C	Military	8 Pin TO-99 Metal Can
RM5532AT/883B	-55°C to +125°C	Military	8 Pin TO-99 Metal Can

Note:

1. /883B suffix denotes Mil-Std-883, Par. 1.2.1 compliant device.

RC5534/RC5534A

High Performance Low Noise Operational Amplifier

Features

- Small signal bandwidth – 10 MHz
- Output drive capability – 600Ω, 10 V_{RMS} at V_S = ±18V
- Input noise voltage – 4 nV/√Hz
- DC voltage gain – 100,000
- AC voltage gain – 6000 at 10 kHz
- Power bandwidth – 200 kHz
- Slew rate – 13 V/µS
- Large supply voltage range – ±3V to ±20V

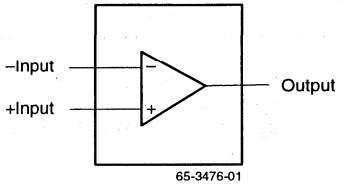
Description

The RC5534 is a high performance, low noise operational amplifier. This amplifier features popular pin-out, superior noise performance, and high output drive capability.

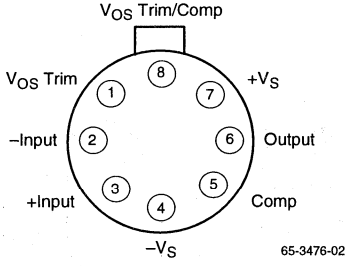
This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product, power bandwidth, and slew rate which far exceeds that of the 741 type amplifiers. The RC5534 is internally compensated for a gain of three or higher and may be externally compensated for optimizing specific performance requirements of various applications such as unity-gain voltage followers, drivers for capacitive loads or fast settling.

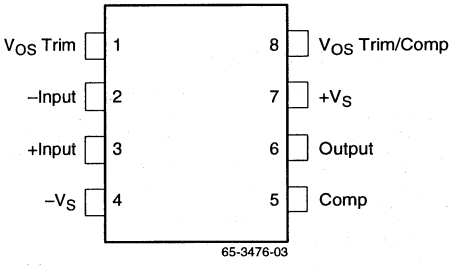
The specially designed low noise input transistors allow the RC5534 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifiers.

Block Diagram



Pin Assignments





Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±22	V
Input Voltage				±V_S	V
Differential Input Voltage				0.5	V
$P_D T_A$ < 50°C	PDIP			468	mW
	CerDIP			833	
	SOIC			658	
Junction Temperature	PDIP			125	°C
	CerDIP, TO-99			175	
Storage Temperature		-65		150	°C
Operating Temperature	RM5534/A	-55		125	°C
	RC5534/A	0		70	
Lead Soldering Temperature (60 sec)				300	°C
Output Short Circuit Duration[2]		Indefinite			

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Short circuit may be to ground only. Rating applies to +125°C case temperature or +175°C junction temperature.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
		TO-99		50		
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		CerDIP		150		
		TO-99		190		
For T_A > 50°C Derate at		PDIP		6.25		mW/°C
		CerDIP		8.33		
		TO-99		5.26		

Operating Conditions

(RM = -55°C ≤ T_A ≤ +125°C; RC = 0°C ≤ T_A ≤ + 70°C, V_S = ±15V)

Parameter	Test Conditions	RM5534/A			RC5534/A			Units
Input Offset Voltage	R_S ≤ 1 kΩ			3.0			5.0	mV
Input Offset Current				500			400	nA
Input Bias Current				1500			2000	nA
Large Signal Voltage Gain	R_L ≥ 600Ω, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	R_L ≥ 600Ω	±10			±10			V
Supply Current	V_S = ±15V, R_L = ∞			9.0			14	mA

DC Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RM5534/A			RC5534/A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 1k\Omega$		0.5	2.0		0.5	4.0	mV
Input Offset Current			10	200		20	300	nA
Input Bias Current			400	800		500	1500	nA
Input Resistance (Diff. Mode)			100			100		kΩ
Large Signal Voltage Gain	$R_L \geq 600\Omega$, V_{OUT} = ±10V	50	100		25	100		V/mV
Output Voltage Swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 1k\Omega$	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 1k\Omega$	86	100		86	100		dB
Supply Current	$R_L = \infty$		4.0	6.5		4.0	8.0	mA
Transient Response Rise Time	V_{IN} = 50 mV, R_L = 600Ω, C_L = 100 pF, C_C = 22 pF		35			35		nS
Overshoot			17			17		%
Slew Rate	C_C = 0		13			13		V/μS
Gain Bandwidth Product	C_C = 22 pF, C_L = 100 pF		10			10		MHz
Power Bandwidth	$V_{OUT} = 20V_{p-p}$, C_C = 0		200			200		kHz
Input Noise Voltage	F = 20 Hz to 20 kHz		1.0			1.0		μV_{RMS}
Input Noise Current	F = 20 Hz to 20 kHz		25			25		pA_{RMS}
Channel Separation	F = 1 kHz, R_S = 5 kΩ		110			110		dB

AC Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RC/RM5534A			RC/RM5534			Units
Input Noise Voltage Density	F_O = 30 Hz		5.5	7.0		7.0		$nV/\sqrt{Hz}$
	F_O = 1 kHz		3.5	4.5		4.0		
Input Noise Current Density	F_O = 30 Hz		1.5			2.5		$pA/\sqrt{Hz}$
	F_O = 1 kHz		0.4			0.6		
Broadband Noise Figure	F = 10 Hz - 20 kHz, RS = 5 kΩ		0.9					dB

Typical Performance Characteristics

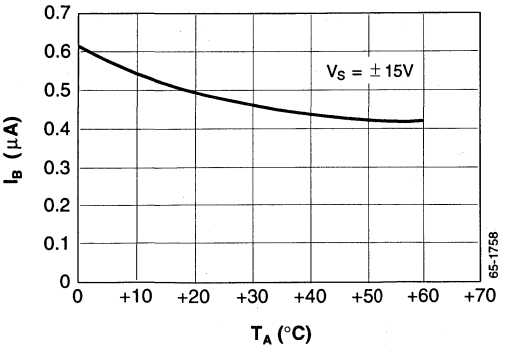


Figure 1. Input Bias Current vs. Temperature

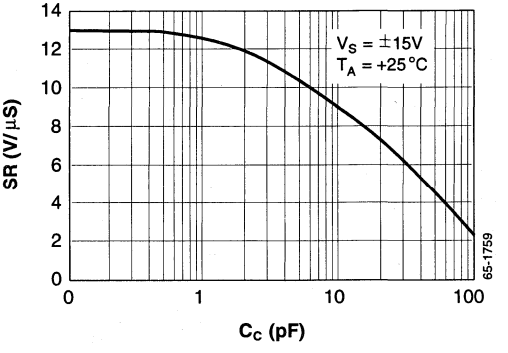


Figure 2. Slew Rate vs. Compensation Capacitor

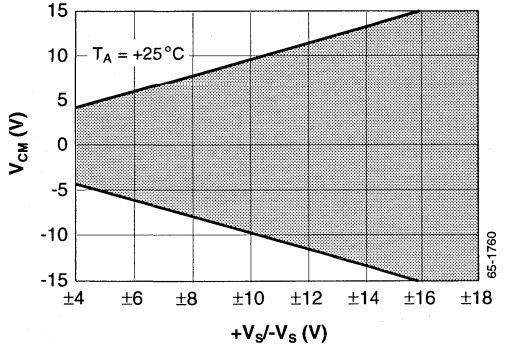


Figure 3. Common Mode Input Range vs. Supply Voltage

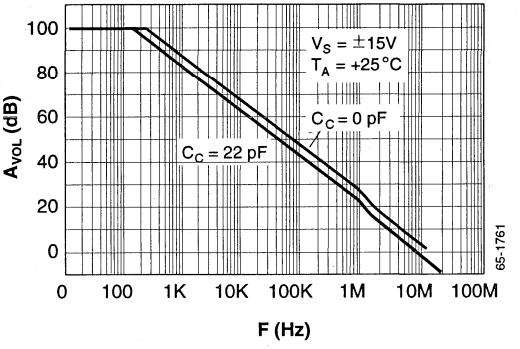


Figure 4. Open Loop Gain vs. Frequency

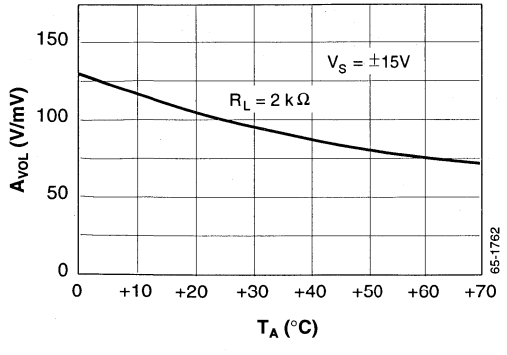


Figure 5. Open Loop Gain vs. Temperature

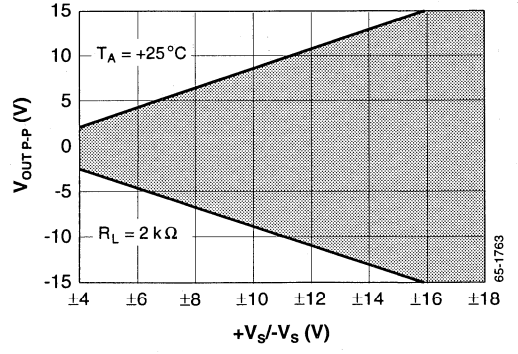


Figure 6. Output Voltage Swing vs. Supply Voltage

Typical Performance Characteristics (continued)

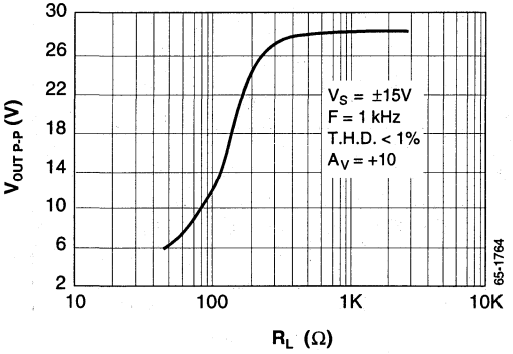


Figure 7. Output Voltage Swing vs. Load Resistance

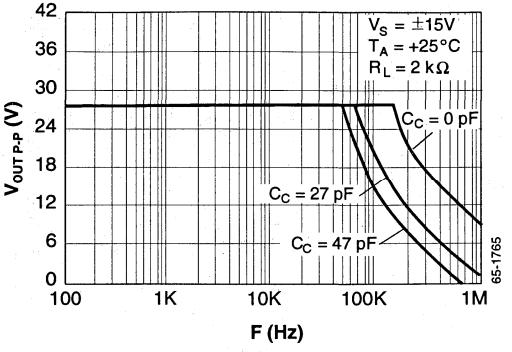


Figure 8. Output Voltage Swing vs. Frequency

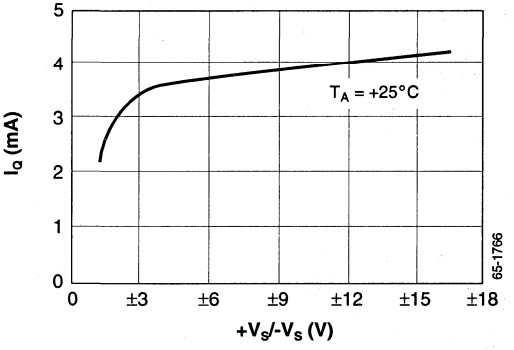


Figure 9. Quiescent Current vs. Supply Voltage

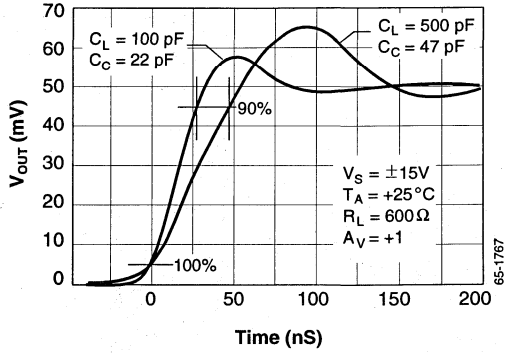


Figure 10. Transient Response Output Voltage vs. Time

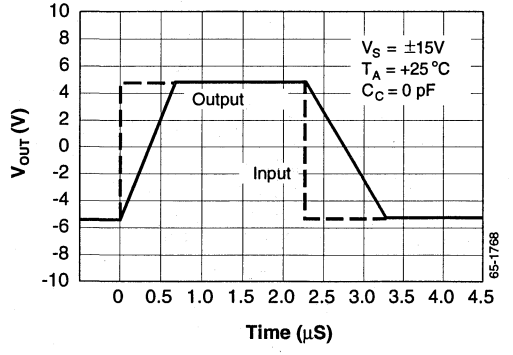


Figure 11. Follower Large Signal Pulse Response Output Voltage vs. Time

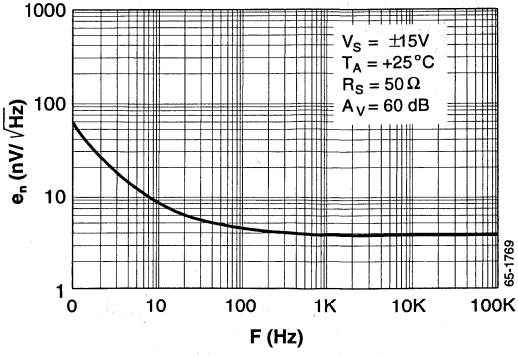


Figure 12. Input Noise Density vs. Frequency

Typical Performance Characteristics (continued)

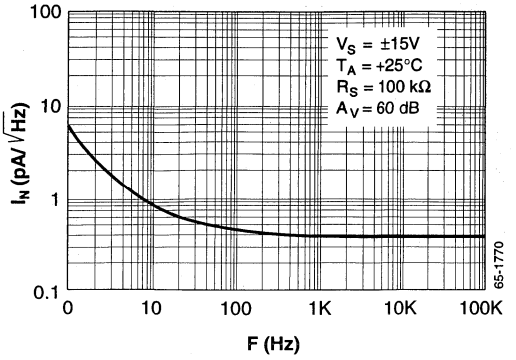


Figure 13. Input Noise Current Density vs. Frequency

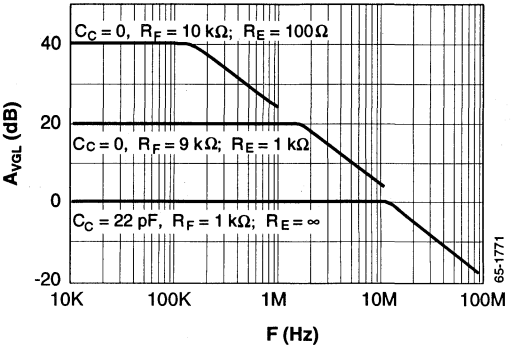


Figure 14. Closed Loop Gain vs. Frequency

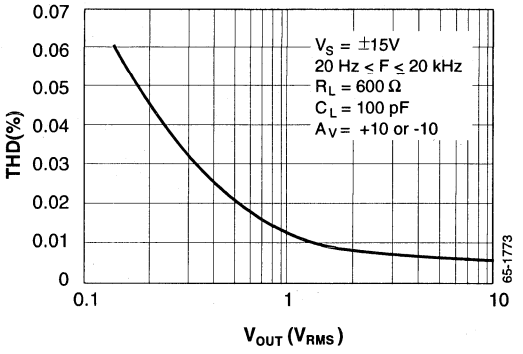


Figure 15. Total Harmonic Distortion vs. Output Voltage

Typical Test Circuits

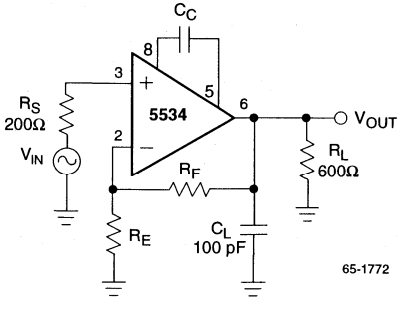


Figure 16. Closed Loop Frequency Response Test Circuit

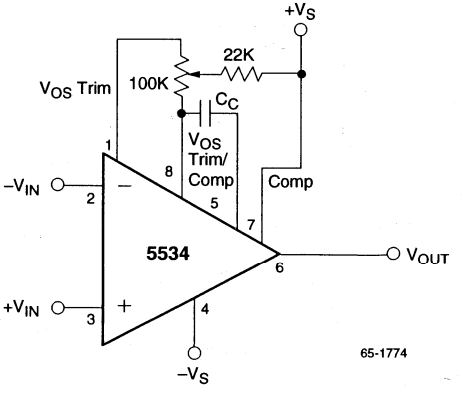
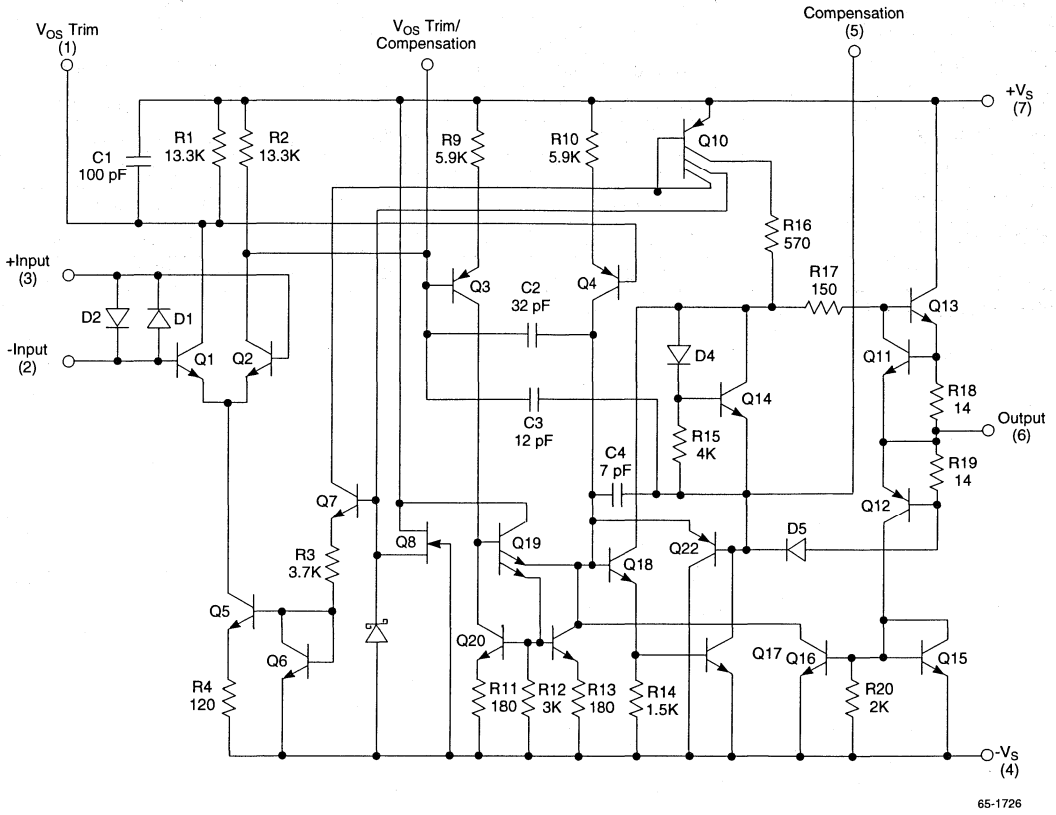


Figure 17. Offset Voltage Trim Circuit

Simplified Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package
RC5534D/RC5534AD	0°C to +70°C	Commercial	8 Pin Ceramic DIP
RC5534N/RC5534AN	0°C to +70°C	Commercial	8 Pin Plastic DIP
RM5534D/RM5534AD	-55°C to +125°C	Commercial	8 Pin Ceramic DIP
RM5534D/883	-55°C to +125°C	Military	8 Pin Plastic DIP
RM5534AD/883	-55°C to +125°C	Military	8 Pin Plastic DIP
RM5534T/RM5534AT	-55°C to +125°C	Commercial	8 Pin TO-99 Metal Can
RM5534T/883	-55°C to +125°C	Military	8 Pin TO-99 Metal Can
RM5534AT/883	-55°C to +125°C	Military	8 Pin TO-99 Metal Can

Note: /883 denotes MIL-STD-883, Par. 1.2.1 compliant device.

RC6100
Horizontal Line Genlock

Features

- High speed tracking sync separator easily follows hum or average picture level (APL) fluctuations
- Glitch remover for operation in high impulse noise environment
- Low-jitter phase-locked loop
- Locks and follows VCR sync
- Compatible with NTSC and PAL systems
- Choice of eight output frequencies
- Field ID output
- Internal VCO

Applications

- Digital video signal processing
- Digital television receivers and VCRs
- Video conferencing equipment
- Multimedia computers

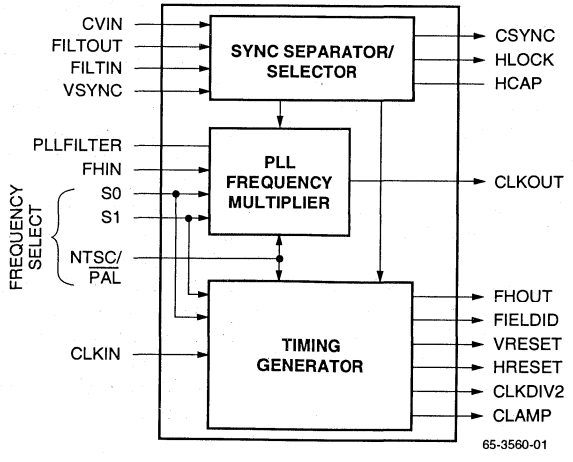
Description

The RC6100 contains a phase-locked loop (PLL) in a frequency multiplier configuration to generate a high-frequency clock as required for video A/D converter and digital video signal processing.

The device accepts composite video, composite sync or component sync signals as input. The output signals generated are: clamp gate, composite sync, horizontal sync, vertical sync, field ID, locked (loop), the oscillator output (Clock), and Clock/2.

The NTSC output frequency choices are: 27.0, 25.175, 14.318, 13.5, 12.588, 12.273, 7.159, and 6.137 MHz. The PAL frequencies generated are: 27.0, 17.734, 15.0, 14.75, 13.5, 8.867, 7.5, and 7.375 MHz.

Logic Symbol



Block Diagram

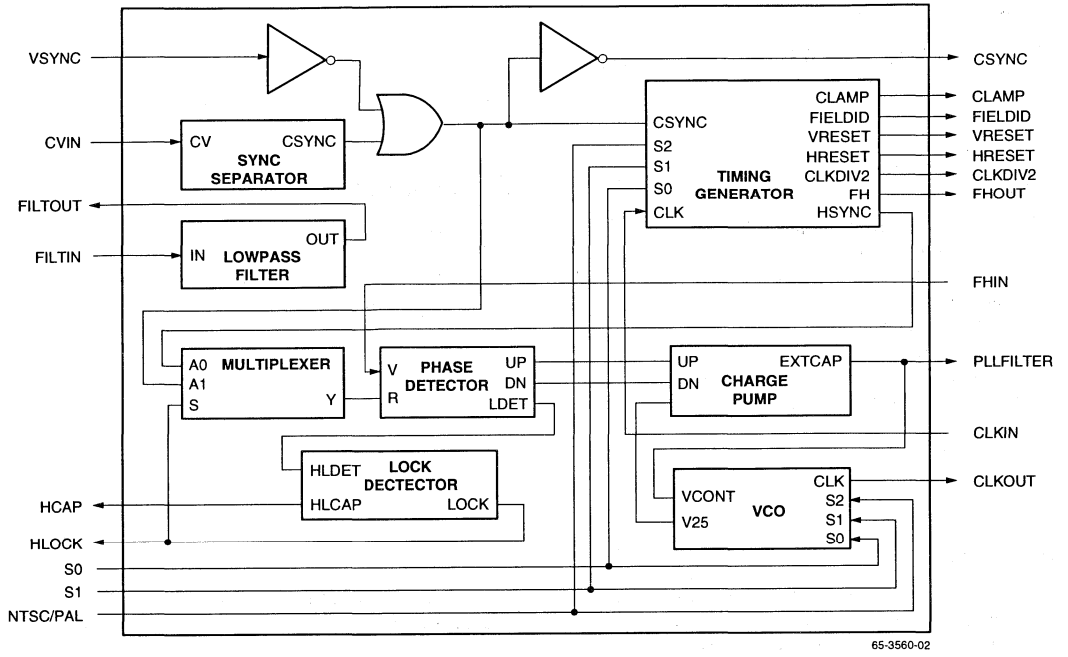


Figure 1.

Functional Description

The RC6100 block diagram is shown in Figure 1. Baseband composite video may be applied to either the FILTIN or CVIN input, depending upon whether the lowpass filter circuit function is desired. Use of the lowpass filter is desirable whenever the input video signal contains impulse noise or glitches that can cause jitter on the sync and clock output signals. Signals that require lowpass filtering should be input at FILTIN and the lowpass filter output (FILTOUT) should be connected to the CVIN input. However, video signals that do not require noise filtering should be input directly at CVIN to optimize performance. The FILTIN and CVIN inputs can also receive composite sync or horizontal sync signals at CMOS or TTL levels.

The input VSYNC is intended for those applications in which the horizontal and vertical sync signals have already been separated. In this mode, horizontal sync should be applied to CVIN and vertical sync applied to VSYNC. These two signals will be combined to form CSYNC and used by the timing generator to form HRESET, VRESET, and the other timing control signals. The VSYNC input is active low and is held at logic high via an internal bias network. If VSYNC is left open, there is no effect on signal processing.

The sync separator extracts a composite sync signal from the composite video, or creates composite sync from separate horizontal and vertical sync inputs. This signal is available at the CSYNC output. Composite sync is also used to control the timing generator, which is the workhorse function of the RC6100.

The timing generator contains programmable dividers for generating and controlling the pixel clock. The selection of pixel clock frequencies is controlled via logic inputs NTSC/PAL, S0, and S1. Table 1 shows the states of these inputs and the corresponding clock frequencies. The timing generator also provides the following output signals: CLAMP, VRESET, FIELDID, HRESET, FHOUT, and CLKDIV2. The CLAMP output is an active-low rectangular pulse of about 4 µs duration, the origination of which is timed by the rising-edge of CSYNC; the pulse is active during the horizontal back-porch interval, as shown in Figure 2. The CLAMP output is also active during the vertical blanking interval. The VRESET output is a short vertical sync signal that is logic low for the duration of the scan line that follows the first serration pulse of the vertical interval, as shown in Figure 3. HRESET is a horizontal sync signal that is set to logic low for one period of the pixel clock (CLKOUT); it is also phase coherent with the pixel clock. FHOUT is a clock signal at the horizontal frequency. It is normally connected to FHIN and used as the VCO (feedback) input to the loop phase comparator. The timing of HRESET relative to FHOUT is shown in Figure 4. (Note: the drawing exaggerates delays t1 and t2.) The FIELDID output goes to logic low immediately after the

VRESET pulse for RS170 Field 1 (the odd field) and toggles to logic high at the same time in the next field (see Figure 3). CLOCKDIV2 is the half-frequency pixel clock output; it is a 50-percent duty-cycle waveform. The Selection Codes of Table 1 (NTSC/PAL, S0, and S1) are input to the RC6100 to select the desired clock frequency to be output. The divisors shown in Table 1 indicate on-half the number of pixel clocks in each horizontal line. The pixel clock generator circuit (Figure 5) is formed by the Phase Detector, Charge Pump, external Loop Filter, and the VCO. The loop filter requires only a simple RC lag-lead network. When the PLL is locked, the VCO provides a pixel clock that is equal to 2NfH, or 2N times the horizontal scan frequency (where N is the frequency divisor value). CLKOUT is normally connected to CLKIN, the clock input of the timing generator function. Note that a half-frequency pixel clock (CLKDIV2) is also generated. Both pixel clock outputs are 50-percent duty-cycle waveforms.

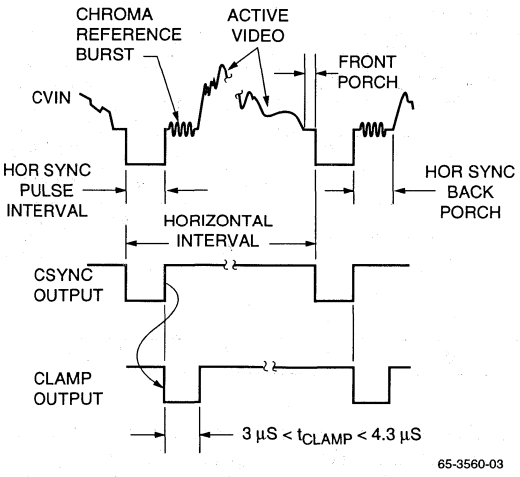
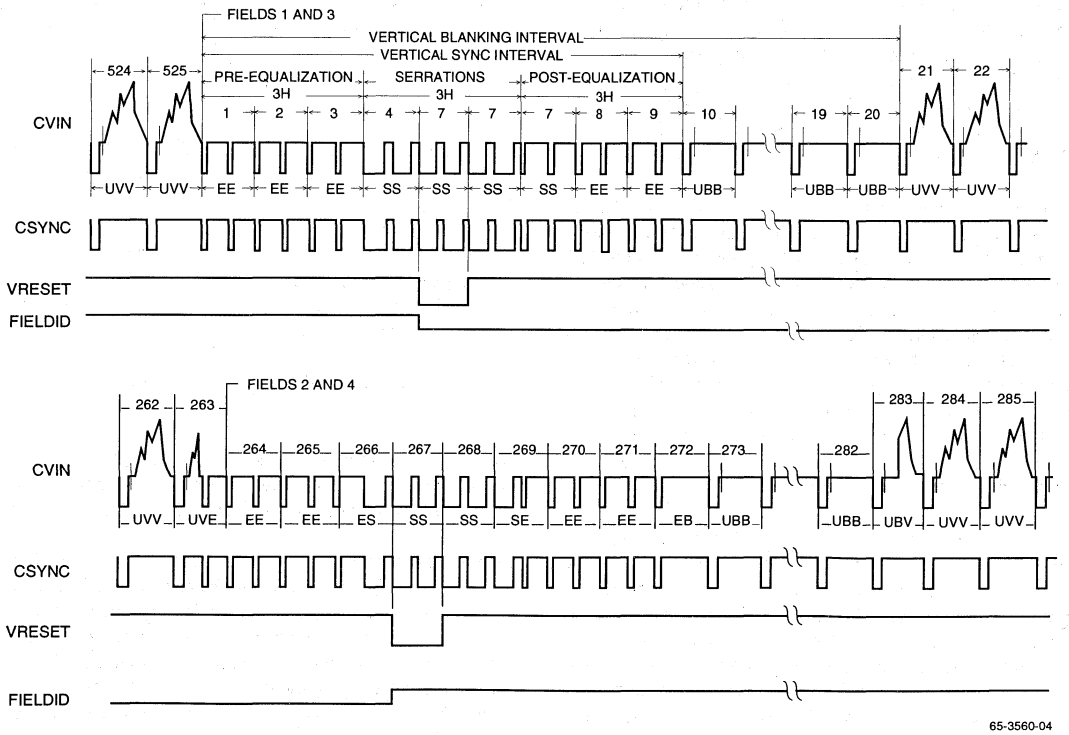


Figure 2. CLAMP Output Timing



Definitions:

UVV: active video
UVE: half-line video, half-line equalization pulse
EE: equalization pulse
EB: equalization broad pulse
SS: vertical sync pulse with serrations
ES: half-line equalization pulse, half-line vertical sync pulse
SE: half-line vertical sync pulse, half-line equalization pulse
UBV: half-line black, half-line video
UBB: black burst

Figure 3. VRESET Output TIming

Table 1. Clock Frequency Selection

Selection Codes			Frequencies (MHz) and Divisors (N)			
NTSC/ PAL	S1	S0	System	Clock Out	Clock/2 Out	Divide by N
1	0	0	NTSC (CCIR601)	27.0	13.5	858
1	0	1	NTSC (VGA)	25.175	12.588	800
1	1	0	NTSC (4fSC/Studio)	14.318	7.159	455
1	1	1	NTSC (Sq. Pixel)	12.273	6.137	390
0	0	0	PAL (CCIR601)	27.0	13.5	864
0	0	1	PAL ((4fSC/Studio)	17.734	8.867	567.5
0	1	0	PAL	15.0	7.5	480
0	1	1	PAL (Sq. Pixel)	14.75	7.375	472

The timing performance of the phase lock is controlled by an external RC filter, the CSYNC signal, and internally-generated horizontal sync signals. When the PLL is not locked, CSYNC is selected as the reference input to the phase detector. CSYNC is derived directly from the composite video input, which contains the required horizontal edge information, and is not dependent upon the loop being locked. When the loop is locked, an internally generated horizontal sync signal from the timing generator is used for this reference input. CSYNC is only used as the loop reference input in the unlocked condition, because it contains serration pulses that would contribute undesirable jitter to the VCO output.

The lock-detect output signal (HLOCK) indicates when the phase reference and VCO inputs of the phase detector are locked. The response time of the lock detector is controlled by an external timing network (R2 and C3) and, when lock is established, the HLOCK output goes low and the MUX makes the appropriate reference signal choice. The values of R2 and C3 were chosen to provide a lock-indication response time that is approximately 15 horizontal lines in duration, and an unlock-indication response time of approximately three horizontal lines in duration. Increasing the value of either R2 or C3 would result in increasing both the lock and unlock response times.

The PLL consists of the phase detector, charge pump, loop filter, VCO, and divide-by-N counter. The phase detector is essentially a control loop summing junction. The charge pump, loop filter, and VCO are in the forward path, and the divide-by-N counter forms the feedback path. Stabilizing this control system consists of choosing the proper component values for the loop filter, such that sufficient phase margin exists at the unity-gain crossover frequency. The filter is a lag-lead network formed by the charge pump, C1 (0.01 µF), R1 (5 KΩ), and C2 (1.0 µF). Increasing the value of C1 moves the pole of the lag network (low pass) closer to the origin (lower frequency). This will reduce the loop bandwidth, which generally tends to reduce VCO jitter, but at a cost of settling (response) time and (in the extreme) stability. Table 2 shows valves for R1. C1, and C2 for all input setings.

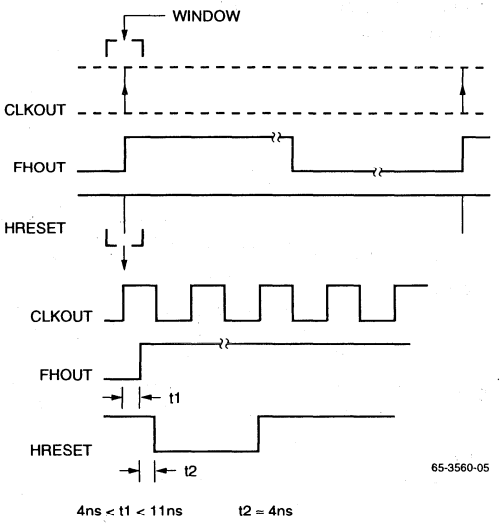


Figure 4. HRESET Output Timing

Increasing the value of either R1 or C2 moves the zero of the lead network (high pass) lower in frequency, which tends to increase loop gain at higher frequencies and can also result in poorer noise performance. The location of the zero is generally determined empirically to adjust the loop transfer function for adequate phase margin for a given desired bandwidth. The values given for C1, R1, and C2 provide excellent loop performance across the entire operating frequency range of the RC6100; loop settling time is approximately 400 µs, and lock detection requires about one millisecond.

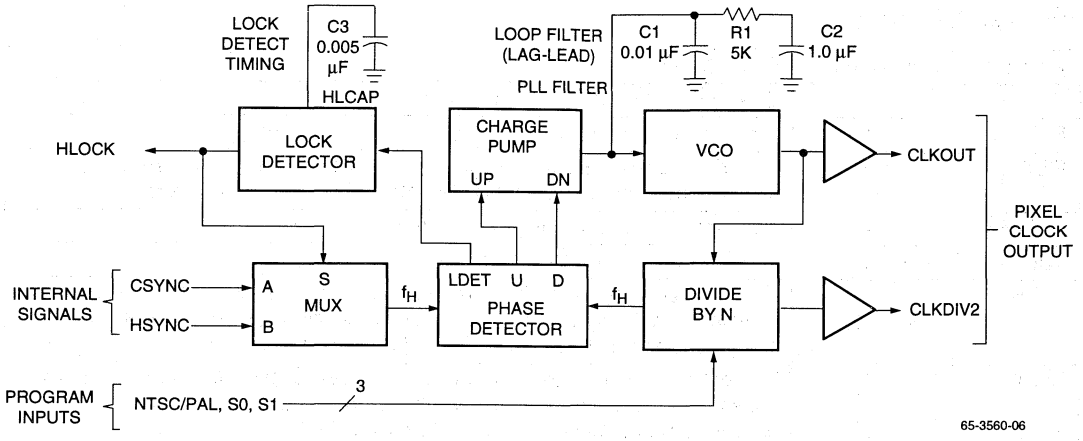


Figure 5. Pixel Clock Generator

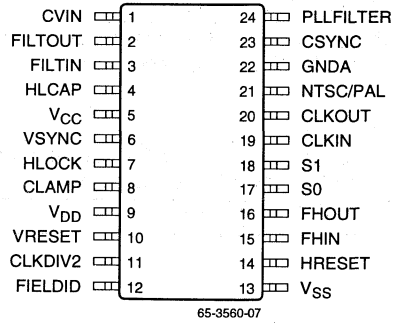
Table 2. PLL Filter Components

code	fin	fosc	Dividers N	Dividers M	KVC0	KCP	R1	C2(K/20)	C1
100	15734	27.00E+06	1.00	858	2.66E+07	3.82E–05	4.17E+03	9.69E–07	9.69E–09
101	15734	25.18E+06	1.00	800	2.66E+07	3.82E–05	3.89E+03	1.04E–06	1.04E–08
110	15734	14.32E+06	2.00	455	2.51E+07	3.82E–05	4.68E+03	8.64E–07	8.64E–09
111	15734	12.27E+06	2.00	390	2.51E+07	3.82E–05	4.01E+03	1.01E–06	1.01E–08
000	15625	27.00E+06	1.00	864	2.66E+07	3.82E–05	4.17E+03	9.76E–07	9.76E–09
001	15625	17.73E+06	2.00	567.5	3.48E+07	3.82E–05	4.19E+03	9.72E–07	9.72E–09
010	15625	15.00E+06	2.00	480	2.48E+07	3.82E–05	4.97E+03	8.19E–07	8.19E–09
011	15625	14.75E	2.00	472	2.48E+07	3.82E–05	4.89E+03	8.33E–07	8.33E–09

Note:

1. Table values are ideal; actual values may vary by ±20% due to process variations.
2. Code: <NTSC/$\overline{\text{PAL}}$> <S1> <S0>

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Description
CVIN	1	This input accepts composite video.
FILTOUT	2	Output of low pass video input filter.
FILTIN	3	This input accepts either composite video, composite sync or horizontal sync signals. The input can be analog (1 Vpp) or TTL/CMOS logic levels.
HLCAP	4	Horizontal lock-detect timing capacitor.
V_{CC}	5	+5V power supply for analog circuits.
VSYNC	6	This input accepts vertical sync pulses for use when video input signals do not contain vertical sync components. This input is active low but remains high in normal operation. The input is TTL or CMOS compatible.
HLOCK	7	The locked-loop output indicates that the oscillator is phase-locked to the incoming horizontal sync. Sensitivity and delay time constant are set by an external capacitor. This output is CMOS or TTL compatible.
CLAMP	8	Clamp gate pulse output. This signal is approximately 4 µs in duration and is timed from the trailing edge of composite sync signal. The clamp gate is used by the video ADC and other video processing circuitry for DC restoration. This output is CMOS or TTL compatible.
V_{DD}	9	+5V power supply for digital circuits.
VRESET	10	Vertical sync signal output. This output is low during the line following the first serration pulse in the vertical sync interval. VRESET is CMOS or TTL compatible.
CLKDIV2	11	CLKOUT divided-by-two output frequency.
FIELDID	12	The field ID output signal is low following the VRESET pulse of RS170 field 1. This output is CMOS or TTL compatible.
V_{SS}	13	Digital ground.
HRESET	14	Horizontal reset signal is decoded from a programmable counter. This signal is coherent with the clock output and is one clock cycle in duration. This output is CMOS or TTL compatible.
FHIN	15	Horizontal frequency signal input; normally driven by FHOUT.
FHOUT	16	Horizontal frequency signal output.
S0, S1	17, 18	Frequency select inputs. They select one of four possible clock frequencies by providing the appropriate divide-by-N for the frequency-multiplying PLL. Table 1 shows the binary, frequency select codes. These inputs are TTL or CMOS compatible.
CLKIN	19	Clock input for internal timing functions; normally driven by CLKOUT.
CLKOUT	20	Buffered VCO output signal.
NTSC/PAL	21	This pin is used to select between NTSC or PAL frequencies of operation. A logic one selects the NTSC frequencies. See Table 1. These inputs are TTL or CMOS compatible.
GNDA	22	Analog ground.
CSYNC	23	Composite sync signal output. This signal is the sync separated from the video input, and is CMOS or TTL compatible.
PLLFILTER	24	PLL loop-compensation filter input.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Power Supply Voltage (V_{CC})			7	V
Input Voltage	V_{CC} + 0.3V ≥ V_{IN} ≥ GND – 0.3V			
Operating Temperature	0		70	°C
Storage Temperature	-40		125	°C
Junction Temperature			150	°C
Lead Soldering Temperature (10 sec)			300	°C

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
θ_{JA}	SO-24 thermal resistance		75		°C/W
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{CC}	Supply current		30	40	mA

DC Electrical Characteristics

V_{CC} = 5V, T_A = 0 to 70°C, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
Logic Interface					
V_{IH}	Logic input high voltage	4			V
V_{IL}	Logic input low voltage			0.8	V
V_{OH}	Logic output high voltage	4			V
V_{OL}	Logic output low voltage			0.4	V
I_{IN}	Logic input current (V_{CC} ≥ VIN ≥ GND)			±30	µA
Analog Interface					
V_{IN}	Composite video signal (AC coupled)			1.0	V_{p-p}
I_{IN}	Input current (V_{IN} = V_{CC}–1V)			±700	µA
HLOCK	Lo @ 10mA		0.5	1.5	V
HLOCK	HI	3.5			V

AC Electrical Characteristics

V_{CC} = 5V, T_A = 0 to 70°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CS}	Composite sync amplitude	Maintains lock with horizontal rate jitter T_{HJ} of <10 ns	150		600	mV_{p-p}
V_{IN}	Impulse noise immunity	CVIN = 1 V_{p-p} + glitch; Glitch < 50 ns, Neg polarity, Voltage relative to blanking; Test for proper CSYNC output	0.3			V
fCLOCK	Clock range		12.273		27.0	MHz
ΔHFOUT/ ΔVCC	VCO power supply rejection rate HFOUT = 27 MHz	4.5V < V_{CCA} < 5.5V			3.5	%/V
HFPULL	PLL Lock/Hold in Range	CVIN horizontal frequency	±500			Hz
	code 100	= 15734 Hz nominal		750		Hz
tPD (VCS)	Video in to CSYNC delay			750		ns
tPD (VHS)	Video in to HRESET delay			750		ns
tPD (HCG)	H sync to CLAMPgate delay			4.4		ns
tDHS	Duration of HRESET reset	fclk = 27 MHz	69	74	89	ns
tDCG	Duration of CLAMPgate		3.0		4.5	µs
fclk jitter	DC=2.5v@pll filter	2.5@VCOin code 100		1	1	ns
	closed loop	CVin=15.734KHz, Code 100, fclk=27MHz		6	20	ns
	Capture Range	fin=15.734+500Hz to 15.625-500Hz	200			Hz
PLLFilter	Sink/source current		±150		±350	µA
CLDIV	VOL @ 4mA				0.8	V
	VOH		3.5			V

Typical Application

Figure 6 shows the RC6100 Horizontal Line Genlock used in a video signal-processing system. The part provides the clock that is required to synchronize the various elements of the system. Note that the clamp gate output of the RC6100 is applied to the clamp gate input of the TMC1175 ADC.

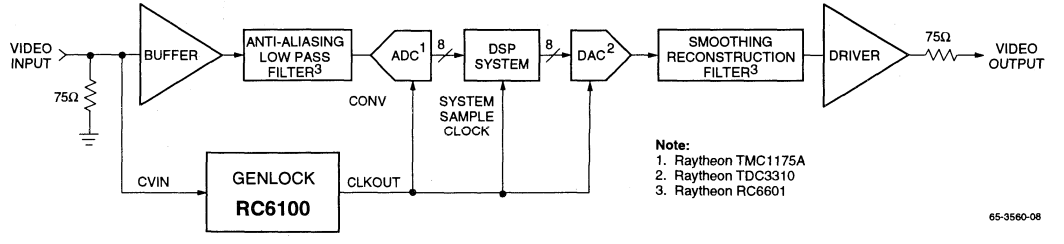


Figure 6. Application of RC6100 with TMC1175 and TDC3310 in Video Processing System

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6100M	0°C to +70°C	Commercial	24 Pin Wide SOIC	RC6100M

THIS PAGE INTENTIONALLY LEFT BLANK

RC6302
Dual Video Amplifier

Features

- Unity gain stable
- 70 MHz -3 dB Bandwidth
- 20 MHz ±0.1 dB gain flatness
- 0.06% differential gain (R_L = 150Ω)
- 0.06° differential phase (R_L = 150Ω)
- High CMRR (100dB), High PSRR (80 dB)
- Dual ±5V power supply
- Low offset 1.0 mV
- 8-pin narrow SO package
- 160 V/µs slew rate
- Fast settling time: 0.1% in 35 ns

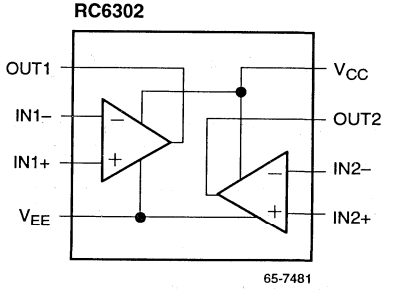
Applications

- Video amplifier
- Video instrumentation amplifier
- Active filter

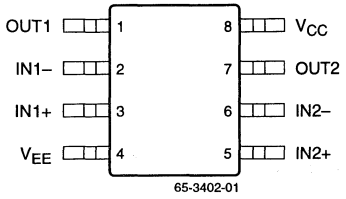
Description

The RC6302 consists of two low power, wide band voltage feedback operational amplifiers. Each channel is capable of delivering a load current of at least 35mA. The amplifiers are optimized for video applications where low differential gain and low phase distortion are significant requirements.

Block Diagram



Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
IN1–	2	Amplifier 1 inverting input
IN1+	3	Amplifier 1 non-inverting input
IN2–	6	Amplifier 2 inverting input
IN2+	5	Amplifier 2 non-inverting input
OUT1	1	Amplifier 1 output
OUT2	7	Amplifier 2 output
V_{EE}	4	Negative supply voltage
V_{CC}	8	Positive supply voltage

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Positive power supply, V_{CC}			7	V
Negative power supply, V_{EE}			-7	V
Differential input voltage			0	V
Operating Temperature	0		+70	°C
Storage Temperature	-40		+125	°C
Junction Temperature			150	°C
Lead Soldering Temperature (10 seconds)			300	°C
Operating Temperature	0		+70	°C
Short circuit tolerance: No more than one output can be shorted to ground.				

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-4.75	-5.0	-5.25	V
θ_{JA}	SO8 Thermal Resistance		140		°C/W

DC Electrical Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, T_A = 0°C to 70°C, R_{LOAD} = 150Ω, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	No load		1.0	±5	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift[1]			6.0	±50	µV/°C
I_B	Input Bias Current			±1.0	±5	µA
$\Delta I_B/\Delta T$	Input Bias Current Drift[1]			±8.0	±50	nA/°C
R_{IN}	Input Resistance[1]		1			MΩ
C_{IN}	Input Capacitance[1]			0.5	2	pF
CMIR	Common Mode Input Range		±2.5			V
CMRR	Common Mode Rejection Ratio	No Load	70	100		dB
PSRR	Power Supply Rejection Ratio	No Load	60	80		dB
Is	Quiescent Supply Current	No Load, Whole IC		15	25	mA
R_{OUT}	Output Impedance[1]	At DC		0.2		Ω
I_{OUT}	Output Current			35		mA
V_{OUT}	Output Voltage Swing	No Load	±2.5	±3.0		V
		RL=150Ω	±2.5	±3.0		V
A_{VOL}	Open-loop Gain		58	68		dB

Note:

1. Guaranteed by design.

AC Electrical Characteristics

V_{CC} = 5V, V_{EE} = -5V, R_{LOAD} = 150Ω, R_G = R_F = 250Ω, A_V = 2, T_A = 0 to 70°C, C_L = 10 pF, C_F = 3 pF unless otherwise specified. Closed Loop. See Typical Test Circuit.

Parameter		Conditions	Min	Typ	Max	Units
Frequency Response						
BW	-3 dB Bandwidth (A_V = 2)[1]	V_{OUT} = 0.4 Vpp		70		MHz
		V_{OUT} = 0.8 Vpp		55		MHz
Flat	±0.1 dB Bandwidth[1]		15	20		MHz
Peak	Maximum Small Signal AC Peaking			0.3		DB
X_{TALK}	Crosstalk Isolation[1]	@ 5 MHz		60		dB
Time Domain Response						
t_{r1}, t_{f1}	Rise and Fall Time 10% to 90%[1]	2V Output Step		6	8	ns
t_s	Settling Time to 0.1 %[1]	2V Output Step		35		ns
OS	Overshoot[1]	2V Output Step		13		%
US	Undershoot[1]	2V Output Step		4		%
SR	Slew Rate[1]	V_{OUT} = ±2.0V		160		V/µs
Distortion						
HD_2	2nd Harmonic Dist. @ 20 MHz[1]	V_{OUT} = 0.8 Vpp		-50		dB
HD_3	3nd Harmonic Dist. @ 20 MHz[1]	V_{OUT} = 0.8 Vpp		-50		dB
Equivalent Input Noise						
NF	Noise Floor > 100 KHz[1]			-140		dBm
SND	Spectral Noise Density[1]	100 kHz to 200 MHz		10		nV/√Hz
Video Performance						
DG	Diff. Gain (p-p), NTSC & PAL[1]	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		%
DP	Diff. Phase (p-p), NTSC & PAL[1]	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		Deg.

Note:

1. Guaranteed by design.

Applications Discussion

Capacitive Load

The RC6302 can drive a capacitive load from 10 to over 100 pF. In back terminated video applications, bandwidth will only be limited by the RC time constants of the external output components. A minimum 10 pF capacitive load is required. When driving a 75Ω cable, place the 75Ω source termination resistor as close to the amplifier output as possible.

DC Accuracy

Since the RC6302 is a voltage-feedback amplifier, the inverting and non-inverting inputs have similar impedances and bias currents. To minimize offset voltage, match the source resistances seen by inverting and non-inverting inputs.

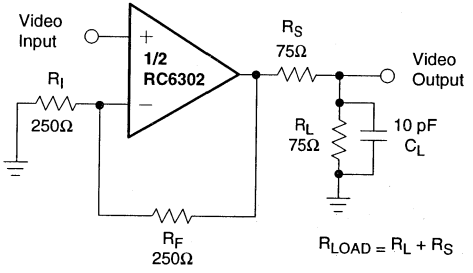
Feedback Components

Because the RC6302 is a voltage-feedback amplifier, it facilitates using reactive (capacitive and inductive) feedback components for implementing filters, integrators, sample/hold circuits, etc. The feedback network and the parasitic capacitance at the inverting (summing junction) input create a pole and affect the transfer function of the circuit. For stable operation, minimize the parasitic capacitance and equivalent resistance of the components used in the feedback circuit.

Circuit Board

High-frequency applications require good grounding, power supply decoupling, low parasitic capacitance and inductance, and good isolation between the three inputs to minimize their crosstalk. Minimal coupling from output to input should exist to prevent positive feedback.

Typical Test Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6302M8	0° to 70°C	Commercial	8 Pin Narrow SOIC	RC6302M8

RC6303

Triple Video Amplifier

with Separate Enable Inputs

Features

- Triple video amplifier
- Independently enabled amplifiers
- 90 MHz -3 dB Bandwidth (A_V = 2)
- 20 MHz ±0.1 dB gain flatness
- Stable at $A_V \geq 2$
- 0.06% differential gain (A_V = 2, R_L = 150Ω)
- 0.06° differential phase (A_V = 2, R_L = 150Ω)
- High CMRR (100dB), High PSRR (80 dB)
- Dual ±5V power supply
- Low offset 1.0 mV
- 16-pin narrow SO package
- 300 V/µs slew rate
- Fast settling time: 0.1% in 35 ns
- TTL or CMOS compatible enable inputs

Applications

- RGB amplifier
- 3:1 crosspoint switch
- RGB switch
- Video instrumentation amplifier
- Selectable gain amplifier
- Active filter

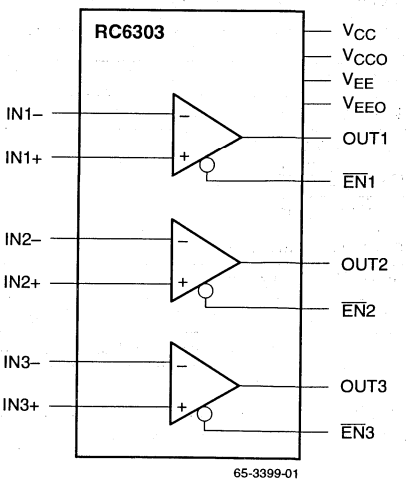
Description

The RC6303 consists of three low power, wide band voltage feedback operational amplifiers. Each channel is capable of delivering a load current of at least 35mA. Each amplifier can be independently enabled or disabled with a TTL or CMOS signal. When disabled, the amplifier is in a high impedance output state, presenting a very high input to output isolation.

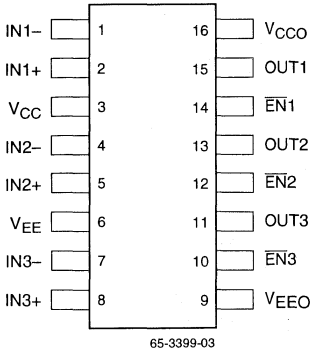
The amplifiers are optimized for video applications with gain ≥ 2 where low differential gain and low phase distortion are significant requirements.

The layout is optimized for minimal crosstalk between amplifiers.

Block Diagram



Pin Assignments



65-3399-03

Pin Definitions

Pin Name	Pin Number	Pin Function Description
$\overline{EN1}$	14	Enables amplifier 1 when low
$\overline{EN2}$	12	Enables amplifier 2 when low
$\overline{EN3}$	10	Enables amplifier 3 when low
IN1–	1	Amplifier 1 inverting input
IN1+	2	Amplifier 1 non-inverting input
IN2–	4	Amplifier 2 inverting input
IN2+	5	Amplifier 2 non-inverting input
IN3–	7	Amplifier 3 inverting input
IN3+	8	Amplifier 3 non-inverting input
OUT1	15	Amplifier 1 output
OUT2	13	Amplifier 2 output
OUT3	11	Amplifier 3 output
V_{CC}	3	Analog positive supply
V_{CCO}	16	Positive supply for output stages
V_{EE}	6	Analog negative supply
V_{EEO}	9	Negative supply for output stages

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Positive power supply, V_{CC}			7	V
Negative power supply, V_{EE}			-7	V
Differential input voltage			0	V
Operating Temperature	0		+70	°C
Storage Temperature	-40		+125	°C
Junction Temperature			150	°C
Lead Soldering Temperature (10 seconds)			300	°C
Short circuit tolerance: No more than one output can be shorted to ground.				

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-4.75	-5.0	-5.25	V
θ_{JA}	SO16 thermal resistance		105		°C/W

DC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, R_{LOAD} = 150Ω, T_A = 0°C to 70°C, unless otherwise specified. Open Loop.

Parameter		Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	No Load		1.0	±5	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift[1]			6.0	±50	µV/°C
I_B	Input Bias Current			±1.0	±5	µA
$\Delta I_B/\Delta T$	Input Bias Current Drift[1]			±8.0	±50	nA/°C
Rin	Input Resistance[1]		1			MΩ
Cin	Input Capacitance[1]			0.5	2	pF
CMIR	Common Mode Input Range		±2.5			V
CMRR	Common Mode Rejection Ratio	No Load	70	100		dB
PSRR	Power Supply Rejection Ratio	No Load	60	80		dB
Is	Quiescent Supply Current	No Load, Whole IC		25	33	mA
Isd	Supply Current Disabled			3	4	mA
R_{OUT}	Output Impedance (Closed Loop) [1]	Enabled, At DC		0.2		Ω
		Disabled, V_O = ±2V	10	200		kΩ
C_{OUT}	Output Capacitance[1]	Disabled		0.5	2	pF
I_{OUT}	Output Current		35			mA
V_{OUT}	Output Voltage Swing	No Load	±2.5	±3.0		V
		R_L = 150Ω	±2.5	±3.0		V
A_{VOL}	Open-loop Gain		58	68		dB
Venh	Enable High Voltage		2.4			V
Venl	Enable Low Voltage				0.8	V
Ien	Enable Input Current			3	10	µA
t_{off}	Disable Time [1]			200		ns
t_{on}	Enable Time [1]	Settling to 1%		160		ns
Iso	Off Isolation (Input to Output)[1]	@ 5 MHz		60		dB

Note:

1. Guaranteed by design.

AC Characteristics

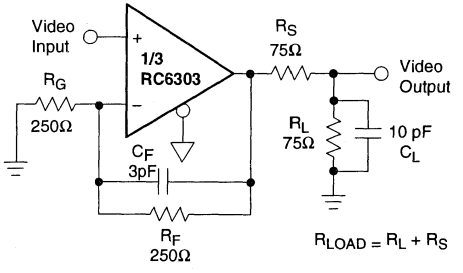
V_{CC} = 5V, V_{EE} = -5V, A_V = 2, T_A = 0 to 70°C, R_{LOAD} = 150Ω, R_G = R_F = 250Ω, C_L = 10 pF, C_F = 3 pF unless otherwise specified. Closed Loop. See Typical Test Circuit.

Parameter		Conditions	Min	Typ	Max	Units
Frequency Response						
BW	-3 dB Bandwidth (A_V = 2)[1]	V_{OUT} = 0.4 Vpp		90		MHz
		V_{OUT} = 0.8 Vpp	70	85		MHz
Flat	±0.1 dB Bandwidth[1]		15	20		MHz
Peak	Maximum Small Signal AC Peaking[1]			0.3		dB
X_{TALK}	Crosstalk Isolation[1]	@ 5 MHz		60		dB
Time Domain Response						
t_{r1}, t_{f1}	Rise and Fall Time 10% to 90%[1]	2V Output Step		6	8	ns
ts	Settling Time to 0.1 %[1]	2V Output Step		35		ns
OS	Overshoot[1]	2V Output Step		13		%
US	Undershoot[1]	2V Output Step		4		%
SR	Slew Rate[1]	V_{OUT} = ±2.0V	200	300		V/µs
Distortion						
HD_2	2nd Harmonic Dist. @ 20 MHz[1]	V_{OUT} = 0.8 Vpp		-50		dB
HD_3	3nd Harmonic Dist. @ 20 MHz[1]	V_{OUT} = 0.8 Vpp		-50		dB
Equivalent Input Noise						
NF	Noise Floor > 100 KHz[1]			-140		dBm
SND	Spectral Noise Density[1]	100 kHz to 200 MHz		10		$nV/\sqrt{Hz}$
Video Performance						
DG	Diff. Gain (p-p), NTSC & PAL[1]	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		%
DP	Diff. Phase (p-p), NTSC & PAL[1]	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		Deg.

Note:

1. Guaranteed by design.

Test Circuit



Applications Discussion

Each of the three sections of the RC6303 is provided with an Enable input, thus the part is useful for selecting and multiplexing. A three-channel video multiplexer can be built with just one RC6303 and a decoder, as shown in Figure 1.

Note that RC6303 enable time is shorter than its disable time, hence a make-before-break action is provided, minimizing switching transients on the signal output.

An RGB switch is shown in Figure 2.

Capacitive Load

The RC6303 can drive a capacitive load from 10 to over 100 pF. In back terminated video applications, bandwidth will only be limited by the RC time constants of the external output components. A minimum 10 pF capacitive load is required. When driving a 75Ω cable, place the 75Ω source termination resistor as close to the amplifier output as possible.

Enable/Disable

The enable pins (10, 12, 14), when pulled to a TTL or CMOS logic low or when tied to ground, activate each amplifier individually. When pulled to a TTL or CMOS logic high, the amplifier is tri-stated and presents a high impedance at its output. When disabled the amplifier's power consumption drops, and the non-inverting input signal is isolated from its respective output.

DC Accuracy

Since the RC6303 is a voltage-feedback amplifier, the inverting and non-inverting inputs have similar impedances and bias currents. To minimize offset voltage, match the source resistances seen by inverting and non-inverting inputs.

Feedback Components

Because the RC6303 is a voltage-feedback amplifier, it facilitates using reactive (capacitive and inductive) feedback components for implementing filters, integrators, sample/hold circuits, etc. The feedback network and the parasitic capacitance at the inverting (summing junction) input create a pole and affect the transfer function of the circuit. For stable operation, minimize the parasitic capacitance and equivalent resistance of the components used in the feedback circuit.

Circuit Board

High-frequency applications require good grounding, power supply decoupling, low parasitic capacitance and inductance, and good isolation between the inputs to minimize their crosstalk. Avoid coupling from output to input to prevent positive feedback.

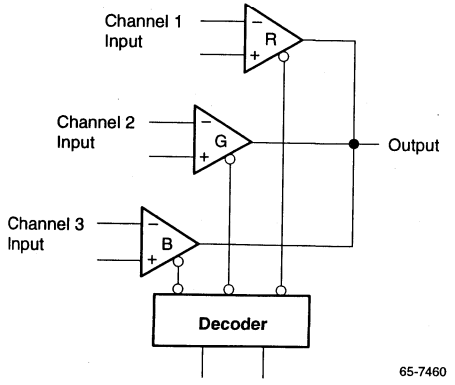


Figure 1.

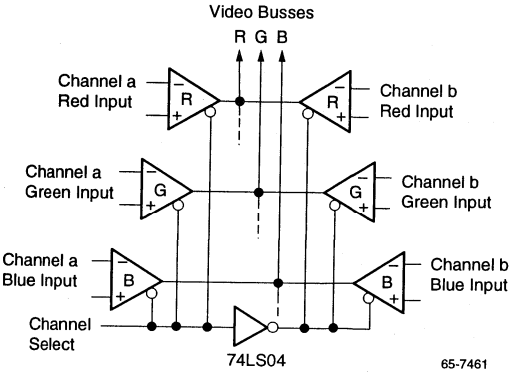


Figure 2.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6303M	0° to 70°C	Commercial	16 Pin Narrow SOIC	RC6303M

RC6333

Triple Video Amplifier

Features

- Triple video amplifier
- 175 MHz -3 dB Bandwidth (A_V = 2)
- 50 MHz ±0.1 dB gain flatness
- Unity gain stable
- 0.06% differential gain (A_V = 1, R_L = 150Ω)
- 0.06° differential phase (A_V = 1, R_L = 150Ω)
- High CMRR (95dB), High PSRR (80 dB)
- Dual ±5V power supply
- Low offset 3.0 mV typical
- 14-pin narrow SO package
- 250V/µs slew rate
- Fast settling time: 0.1% in 15 ns
- TTL or CMOS compatible

Applications

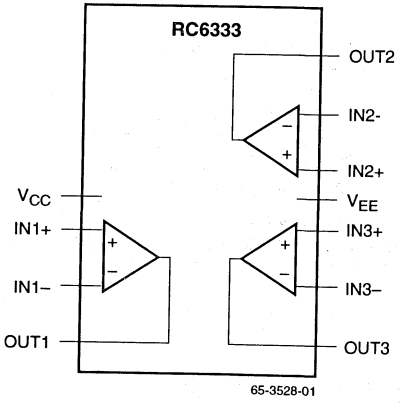
- RGB amplifiers
- Video instrumentation amplifier
- Selectable gain amplifier
- Active filters
- Set-top Buffers/Drivers

Description

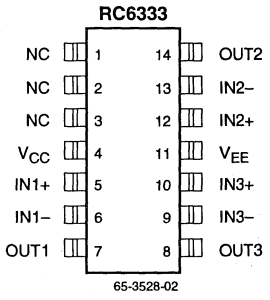
The RC6333 consists of three low power, wide band voltage feedback operational amplifiers. Each channel is capable of delivering a load current of at least 35mA.

The amplifiers are optimized for video applications where low differential gain and low phase distortion are significant requirements.

Block Diagram



Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
IN1–	6	Amplifier 1 inverting input
IN1+	5	Amplifier 1 non-inverting input
IN2–	13	Amplifier 2 inverting input
IN2+	12	Amplifier 2 non-inverting input
IN3–	9	Amplifier 3 inverting input
IN3+	10	Amplifier 3 non-inverting input
NC	1–3	Not Connected.
OUT1	7	Amplifier 1 output
OUT2	14	Amplifier 2 output
OUT3	8	Amplifier 3 output
VCC	4	Analog positive supply
VEE	11	Analog negative supply

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
VCC	Positive power supply			7	V
VEE	Negative power supply			-7	V
	Differential input voltage			0	V
	Operating Temperature	0		+70	°C
	Storage Temperature	-40		±125	°C
	Junction Temperature			150	°C
	Lead Soldering (10 seconds)			240	°C
Short circuit tolerance: No more than one output can be shorted to ground.					

Notes:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter		Min	Typ	Max	Units
VCC	Power Supply Voltage	4.75	5.0	5.25	V
VEE	Negative Supply Voltage	-4.75	-5.0	-5.25	V
θJA	SO14 Thermal Resistance		105		°C/W

DC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, R_{LOAD} = 150Ω, T_A = 0°C to 70°C, unless otherwise specified. Open Loop.

Parameter		Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	No Load		3	±10	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift[1]			±6	±30	µV/°C
I_B	Input Bias Current			±1	±5	µA
$\Delta I_B/\Delta T$	Input Bias Current Drift[1]			±8	±40	nA/°C
Rin	Input Resistance[1]		1			MΩ
Cin	Input Capacitance[1]			0.5	2	pF
CMIR	Common Mode Input Range		±2.5			V
CMRR	Common Mode Rejection Ratio	No Load	70	100		dB
PSRR	Power Supply Rejection Ratio	No Load	65	80		dB
Is	Quiescent Supply Current	No Load		26	40	mA
R_{OUT}	Output Impedance (Closed Loop)[1]	Enabled, At DC		0.2		Ω
I_{OUT}	Output Current	Per Amplifier	35			mA
V_{OUT}	Output Voltage Swing	No Load	±2.5	±3.0		V
		R_L = 150Ω	±2.5	±3.0		V
A_{VOL}	Open-loop Gain		60	75		dB

Note:

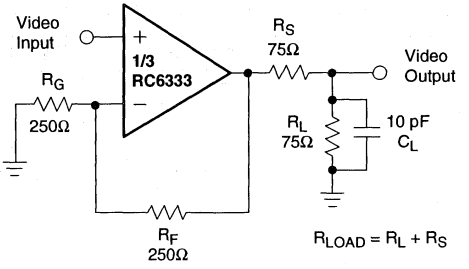
1. Guaranteed by design.

AC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, T_A = 0 to 70°C, R_{LOAD} = 150Ω, R_G = R_F = 250Ω, C_L = 10 pF, unless otherwise specified. Closed Loop. Guaranteed by Design. See Typical Test Circuit.

Parameter		Conditions	Min	Typ	Max	Units
Frequency Response						
BW	-3 dB Bandwidth (A_V = 2)	V_{OUT} = 0.4 Vpp		+175		MHz
		V_{OUT} = 0.8 Vpp	75	90		MHz
Flat	±0.1 dB Bandwidth	V_{OUT} = 0.4 Vpp	50	75		MHz
Peak	Maximum Small Signal AC Peaking	V_{OUT} = 0.8 Vpp		0.01		dB
X_{TALK}	Crosstalk Isolation	@ 5 MHz		50		dB
Time Domain Response						
t_{r1}, t_{f1}	Rise and Fall Time 10% to 90%	2V Output Step		10	15	ns
ts	Settling Time to 0.1%	2V Output Step		15		ns
OS	Overshoot	2V Output Step		5		%
US	Undershoot	2V Output Step		2		%
SR	Slew Rate	V_{OUT} = ±2.0V	200	250		V/µs
Distortion						
HD_2	2nd Harmonic Dist. @ 20 MHz	V_{OUT} = 0.8 Vpp		-48		dB
HD_3	3nd Harmonic Dist. @ 20 MHz	V_{OUT} = 0.8 Vpp		-56		dB
Video Performance						
DG	Diff. Gain (p-p), NTSC & PAL	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		%
DP	Diff. Phase (p-p), NTSC & PAL	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		Deg.
NF	Noise Floor	>100kHz		-130		dB rms

Test Circuit



Applications Discussion

Capacitive Load

The RC6333 can drive a capacitive load from 10 to over 50 pF. In back terminated video applications, bandwidth will only be limited by the RC time constants of the external output components. When driving a 75Ω cable, place the 75Ω source termination resistor as close to the amplifier output as possible.

DC Accuracy

Since the RC6333 is a voltage-feedback amplifier, the inverting and non-inverting inputs have similar impedances and bias currents. To minimize offset voltage, match the source resistances seen by inverting and non-inverting inputs.

Feedback Components

Because the RC6333 is a voltage-feedback amplifier, it facilitates using reactive (capacitive and inductive) feedback components for implementing filters, integrators, sample/hold circuits, etc. The feedback network and the parasitic capacitance at the inverting (summing junction) input create a pole and affect the transfer function of the circuit. For stable operation, minimize the parasitic capacitance and equivalent resistance of the components used in the feedback circuit.

Circuit Board

High-frequency applications require good grounding, power supply decoupling, low parasitic capacitance and inductance, and good isolation between the inputs to minimize their crosstalk. Avoid coupling from output to input to prevent positive feedback.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6333M	0° to 70°C	Commercial	14 Pin Narrow SOIC	RC6333M

RC6334
Quad Video Amplifier

Features

- Quad video amplifier
- 175 MHz -3 dB Bandwidth (A_V = 2)
- 50 MHz ±0.1 dB gain flatness
- Unity gain stable
- 0.06% differential gain (A_V = 1, R_L = 150Ω)
- 0.06° differential phase (A_V = 1, R_L = 150Ω)
- High CMRR (95dB), High PSRR (80 dB)
- Dual ±5V power supply
- Low offset 3.0 mV typical
- 14-pin narrow SO package
- 250V/µs slew rate
- Fast settling time: 0.1% in 15 ns
- TTL or CMOS compatible

Applications

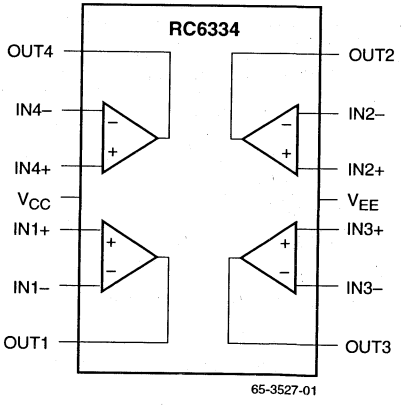
- RGB amplifiers
- Video instrumentation amplifier
- Selectable gain amplifier
- Active filters
- Set-top box Buffers/Drivers

Description

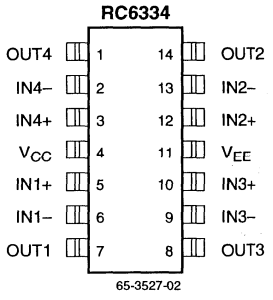
The RC6334 consists of four low power, wide band voltage feedback operational amplifiers. Each channel is capable of delivering a load current of at least 35mA.

The amplifiers are optimized for video applications where low differential gain and low phase distortion are significant requirements.

Block Diagram



Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
IN1–	6	Amplifier 1 inverting input
IN1+	5	Amplifier 1 non-inverting input
IN2–	13	Amplifier 2 inverting input
IN2+	12	Amplifier 2 non-inverting input
IN3–	9	Amplifier 3 inverting input
IN3+	10	Amplifier 3 non-inverting input
IN4–	2	Amplifier 4 inverting input
IN4+	3	Amplifier 4 non-inverting input
OUT1	7	Amplifier 1 output
OUT2	14	Amplifier 2 output
OUT3	8	Amplifier 3 output
OUT4	1	Amplifier 4 output
V_{CC}	4	Analog positive supply
V_{EE}	11	Analog negative supply

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
V_{CC}	Positive power supply			7	V
V_{EE}	Negative power supply			-7	V
	Differential input voltage			0	V
	Operating Temperature	0		+70	°C
	Storage Temperature	-40		±125	°C
	Junction Temperature			150	°C
	Lead Soldering (10 seconds)			240	°C
Short circuit tolerance: No more than one output can be shorted to ground.					

Notes:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-4.75	-5.0	-5.25	V
θ_{JA}	SO14 Thermal Resistance		105		°C/W

DC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, R_{LOAD} = 150Ω, T_A = 0°C to 70°C, unless otherwise specified. Open Loop.

Parameter		Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	No Load		3	±10	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift[1]			±6	±30	µV/°C
I_B	Input Bias Current			±1	±5	µA
$\Delta I_B/\Delta T$	Input Bias Current Drift[1]			±8	±40	nA/°C
Rin	Input Resistance[1]		1			MΩ
Cin	Input Capacitance[1]			0.5	2	pF
CMIR	Common Mode Input Range		±2.5			V
CMRR	Common Mode Rejection Ratio	No Load	70	100		dB
PSRR	Power Supply Rejection Ratio	No Load	65	80		dB
Is	Quiescent Supply Current	No Load		33	48	mA
R_{OUT}	Output Impedance (Closed Loop)[1]	Enabled, At DC		0.2		Ω
I_{OUT}	Output Current	Per Amplifier	35			mA
V_{OUT}	Output Voltage Swing	No Load	±2.5	±3.0		V
		R_L = 150Ω	±2.5	±3.0		V
A_{VOL}	Open-loop Gain		60	75		dB

Note:

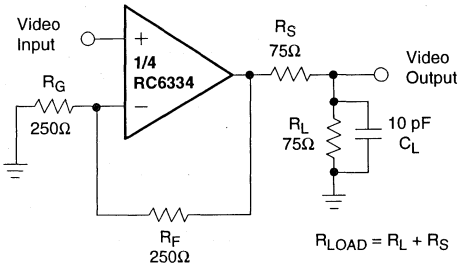
1. Guaranteed by design.

AC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, T_A = 0 to 70°C, R_{LOAD} = 150Ω, R_G = R_F = 250Ω, C_L = 10 pF, unless otherwise specified. Closed Loop. Guaranteed by Design. See Typical Test Circuit.

Parameter		Conditions	Min	Typ	Max	Units
Frequency Response						
BW	-3 dB Bandwidth (A_V = 2)	V_{OUT} = 0.4 Vpp		+175		MHz
		V_{OUT} = 0.8 Vpp	75	90		MHz
Flat	±0.1 dB Bandwidth	V_{OUT} = 0.4 Vpp	50	60		MHz
Peak	Maximum Small Signal AC Peaking	V_{OUT} = 0.8 Vpp		0.01		dB
X_{TALK}	Crosstalk Isolation	@ 5 MHz		50		dB
Time Domain Response						
t_{r1}, t_{f1}	Rise and Fall Time 10% to 90%	2V Output Step		10	15	ns
ts	Settling Time to 0.1%	2V Output Step		15		ns
OS	Overshoot	2V Output Step		5		%
US	Undershoot	2V Output Step		2		%
SR	Slew Rate	V_{OUT} = ±2.0V	200	250		V/µs
Distortion						
HD_2	2nd Harmonic Dist. @ 20 MHz	V_{OUT} = 0.8 Vpp		-48		dB
HD_3	3nd Harmonic Dist. @ 20 MHz	V_{OUT} = 0.8 Vpp		-56		dB
Video Performance						
DG	Diff. Gain (p-p), NTSC & PAL	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		%
DP	Diff. Phase (p-p), NTSC & PAL	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		Deg.
NF	Noise Floor	>100kHz		-130		dB rms

Test Circuit



65-3527-04

Applications Discussion

Capacitive Load

The RC6334 can drive a capacitive load from 10 to over 50 pF. In back terminated video applications, bandwidth will only be limited by the RC time constants of the external output components. When driving a 75Ω cable, place the 75Ω source termination resistor as close to the amplifier output as possible.

DC Accuracy

Since the RC6334 is a voltage-feedback amplifier, the inverting and non-inverting inputs have similar impedances and bias currents. To minimize offset voltage, match the source resistances seen by inverting and non-inverting inputs.

Feedback Components

Because the RC6334 is a voltage-feedback amplifier, it facilitates using reactive (capacitive and inductive) feedback components for implementing filters, integrators, sample/hold circuits, etc. The feedback network and the parasitic capacitance at the inverting (summing junction) input create a pole and affect the transfer function of the circuit. For stable operation, minimize the parasitic capacitance and equivalent resistance of the components used in the feedback circuit.

Circuit Board

High-frequency applications require good grounding, power supply decoupling, low parasitic capacitance and inductance, and good isolation between the inputs to minimize their crosstalk. Avoid coupling from output to input to prevent positive feedback.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6334M	0° to 70°C	Commercial	14 Pin Narrow SOIC	RC6334M

RC6601

Programmable Video Filter

Features

- 1 MHz to 10 MHz minimum programmable range
- Approximates CCIR601 digital video standard
- Phase corrected for minimum group delay variation
- External voltage or current control of cutoff frequency
- 0.25 % differential gain, R_L = 150Ω
- 0.20° differential phase, R_L = 150Ω
- No precision external components required
- Single ended input/output
- ±5V power supply
- 16-pin SOIC package

Applications

- Video filtering
- Communication filters
- ADC anti-aliasing filter
- HDTV
- Set top boxes
- Satellite modems

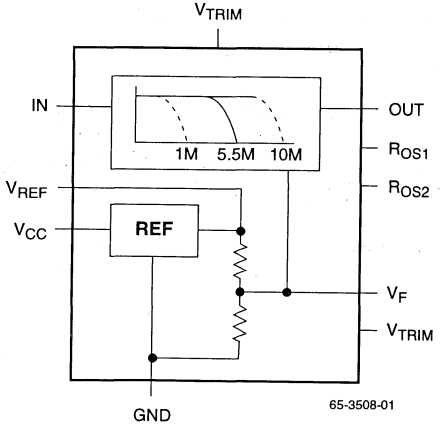
Description

The RC6601 is a fully integrated, continuous time filter, programmable for various video filtering applications. The RC6601 approximates the requirements of the CCIR601 standard for digitizing NTSC and PAL video signals. It provides a pass band ripple of ±0.25 dB typical up to 5.5 MHz with a -40 dB stop band, beginning at 8 MHz.

The structure of the filter assures wide dynamic range operation with low noise and low distortion. The cutoff frequency is factory set at 5.5 MHz (±5% typical). It can be varied over a range of 1–10 MHz by a user supplied voltage V_F. The voltage V_F can be readily derived from the on-chip precision reference voltage V_{REF} as shown in the typical application circuit.

The RC6601 is packaged in a wide body, 16-pin SOIC package. The package dimensions are included in this data sheet.

Block Diagram



Functional Description

Digitizing video signals requires high-order anti-aliasing filters that can handle large signal swings with low distortion. CCIR601 standards recommend equi-ripple gain and group delay characteristics for filtering NTSC and PAL signals. RC6601 is a single-chip solution that matches the requirements with less than ±0.25dB gain ripple, ±20ns group delay variation in the passband, and more than 40dB attenuation in the stop band. The block diagram in Figure 1a shows the direct synthesis of the filter transfer function as a fifth order elliptic with third order phase equalization. The cut-off frequency, nominally set at 5.5MHz, is continuously programmable over a decade. Using current mode techniques, the IC can drive 2Vpp signals into 75Ω load drawing only 35mA quiescent current.

The architecture of the complete filter as illustrated by Figure 1a is a 5th-order elliptic transfer function in tandem with a 3rd-order all-pass phase equalizer. The Cauer-elliptic response function has an equi-ripple passband with a sharp roll-off into stop-band in the magnitude transfer function but causes excessive group delay peaking. The equalizer maintains this magnitude response while compensating for the group delay peaking. These two filters are represented in Figure 1a by a series of 2nd-order expressions that can be realized as biquads using transimpedance-based integrators.

Elliptic poles and zeros give a flat magnitude response in passband and a 40dB roll-off from 5.5MHz to 8MHz. The equalizer transfer function corrects group delay to ±15ns to 90% of the cut-off frequency. These pole-zero values determine biquad coefficients as shown in Figure 1b. A supply-independent band-gap cell generates and distributes bias currents for all the transimpedance integrators as in Figure 1b. The cut-off frequency is programmed by globally scaling the currents, using a single external setting.

The entire filter, including the programmable bias generators, is integrated on a single chip using complementary bipolar technology. The npn and pnp transistors have a cut-off frequency of 4GHz and of 1.5GHz respectively. Gate-oxide-based capacitors and thin film resistors with 0.5% match set filter time constants. At 5.5MHz cut-off, the filter averages 2.5mA/pole. Nearly 15mA of the supply current is used for the output driver. The cut-off frequency is actually programmable beyond the 1–10 MHz, with an external voltage control. Measured differential gain of 0.25% and a differential phase of 0.2° make it well suited for video applications.

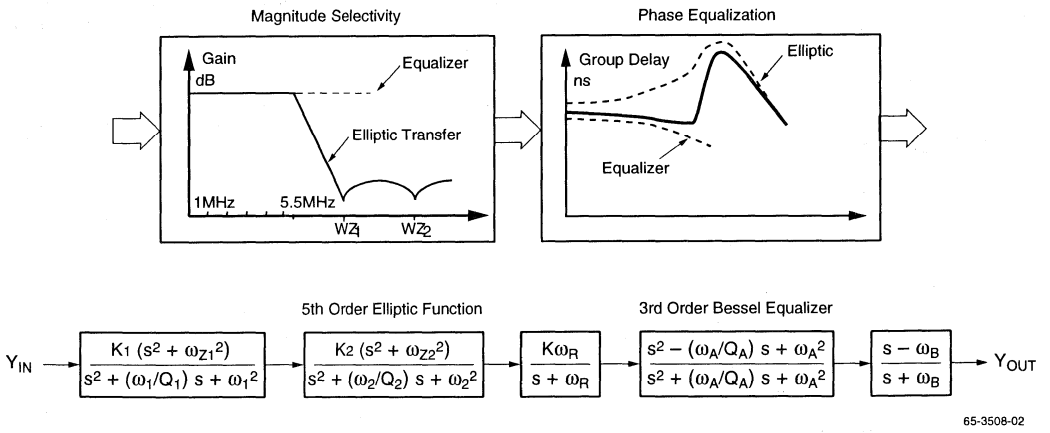
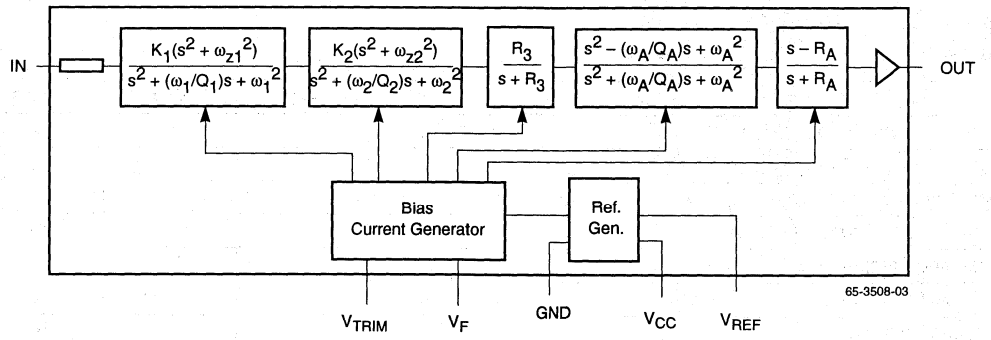


Figure 1a. Composite Video Filter

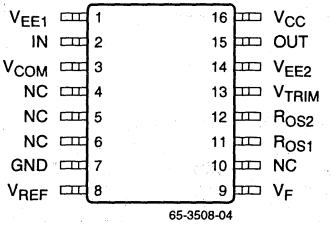


$K_1, K_2 = 0.09293$ $\omega_{Z1} = 1.415\omega_C$ $\omega_1 = 1.046\omega_C$
$Q_1 = 5.67$ $\omega_{Z2} = 2.0733\omega_C$ $\omega_2 = 0.855\omega_C$
$Q_2 = 1.1776$ $R_3 = 0.59678\omega_C$ $\omega_A = 1.44868\omega_C$
$Q_A = 0.691$ $R_A = 1.323\omega_C$

where ω_C = cut off frequency (in radians)
e.g. for default filter: $\omega_C = 2\pi \bullet (5.5)10^6 = 34.5575 \times 10^6$
Scaling bias currents directly scales the frequency ω_C

Figure 1b. Internal Programming Architecture

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Description
GND	7	Supply Ground
IN	2	Signal Input
NC	4–6, 10	No Connect
OUT	15	Signal Output
ROS1	11	Offset Adjust 1
ROS2	12	Offset Adjust 2
VCC	16	Positive Supply Voltage
VCOM	3	Common Mode Voltage
VEE1	1	Negative Supply
VEE2	14	Negative Supply Voltage (Output)
VF	9	Filter Control Voltage for Cut-off Frequency
VREF	8	Precision Reference Voltage
VTRIM	13	Pass Band Peaking Voltage

Preliminary Information

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Positive Power Supply (V_{CC})			6	V
Negative Power Supply (V_{EE1}, V_{EE2})			-6	V
Input Voltage (V_{EE1}, V_{EE2})	-0.3 V to V_{CC} to +0.3V			V
Input Current (Power On or Off)			±10	mA
Operating Temperature	0		70	°C
Storage Temperature	-40		125	°C
Junction Temperature		150		°C
Lead Soldering (10 seconds)			300	°C
Short Circuit Tolerance	No more than one output may be shorted to ground.			

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-5.25	-5.0	-4.75	V
I_S	Quiescent Supply Current		40	50	mA
θ_{JA}	SO16 thermal resistance		105		°C/W

DC Electrical Characteristics

V_{CC} = 5V, $V_{EE1,2}$ = -5V, C_L = 15pF, R_L = 150Ω, T_A = 0°C to 70°C, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
A_V	DC gain accuracy	V_{IN} = 2 Vpp	0.90	1	1.10	V/V
R_{IN}	Input resistance	DC		4		kΩ
I_O	Output current			±10		mA
V_{OFF}	Output offset voltage	Without offset adjust	-500		+500	mV
		With offset adjust	-10		+10	mV
V_{REF}	Reference voltage		2.30	2.48	2.60	V
I_{REF}	Reference output current	Max reference out current		5		mA
V_F	Frequency set voltage (FC = 5.5 MHz ±10%)	I_F = 0, Measure V_F		1.24		V
R_F	Frequency set input resistance			5.0		kΩ

AC Electrical Characteristics

V_{CC} = 5V, $V_{EE1,2}$ = -5V, C_L = 15pF, R_L = 150Ω, f_{PB} = 5.5 MHz, T_A = 0°C to 70°C, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
Filter Characteristics						
f_{PB}	Passband frequency	$V_F \approx 0V$	10	15		MHz
		$V_F = V_{REF} \approx 2.5V$	.25		1	MHz
f_{CA}	Filter cutoff accuracy(5,6)	f_{PB} = 5.5MHz	-5		+5	%
f_{CT}	Filter cutoff drift(5)	f_{PB} = 5.5MHz	-5		+5	%
Δt_{GD}	Group delay flatness	f_{in} = 100 kHz to 4,9 MHz		±20		ns
V_{IN}	Input signal range	THD < 1 %(7)	1	2		Vpp
C_{IN}	Input capacitance			10		pF
ΔG	Diff. gain, NTSC & PAL	V_{IN} = 286 mVpp, 4.43 MHz		.25		%
ΔP	Diff. phase, NTSC & PAL	V_{IN} = 286 mVpp, 4.43 MHz		.20		°
e_n	RMS output noise voltage	R_S = 75 Ω, 10 MHz BW(7)		1.3	2.0	mV
SR	Positive slew rate(3)	V_{IN} = 2 Vpp		60		V/µs
	Negative slew rate(3)	V_{IN} = 2 Vpp		60		V/µs
R_O	Output resistance			3		Ω
ATT	Attenuation(1)	$f_{in} \leq$ 5.0 MHz, V_{IN} = 1 Vpp		±0.10	±0.25	dB
	Attenuation(2)	$f_{in} \leq$ 5.0 MHz, V_{IN} = 1 Vpp		±0.5	± 1	dB
	Attenuation(2)	f_{in} = 6.75 MHz, V_{IN} = 1 Vpp		-12	-8	dB
	Attenuation(2)	f_{in} = 8 MHz, V_{IN} = 1 Vpp		-40		dB
	Attenuation(2)	8 MHz < f_{in} < 50 MHz, V_{IN} = 1 Vpp		-40	-35	dB
	Attenuation(1,4)	$f_{IN} \leq$ 2.5 MHz, V_{IN} = 1 Vpp		±0.10	±0.25	dB
	Attenuation(2,4)	$f_{IN} \leq$ 2.5 MHz, V_{IN} = 1 Vpp		±0.5	± 1	dB
	Attenuation(2,4)	f_{IN} = 3.375 MHz, V_{IN} = 1 Vpp			-8	dB
	Attenuation(2,4)	f_{IN} = 4 MHz, V_{IN} = 1 Vpp		-40		dB
	Attenuation(2,4)	4 MHz < f_{IN} < 50 MHz, V_{IN} = 1 Vpp			-35	dB
SPW	Sensitivity of cutoff frequency vs. supply voltages	V_S = ±5 V, V_F = 1.25 V		1		%/V

Notes:

1. V_{TRIM} adjusted for optimum response.
2. No external adjustments.
3. Guaranteed no slew limit on 2V p-p input at 9 MHz.
4. Filter programmed for 2.75 MHz cutoff, V_F = 1.85V.
5. Filter cutoff defined to edge of ripple spec.
6. Initial setpoint accuracy of cutoff, excluding temperature and long term drift.
7. Guaranteed by design.

Performance Curves

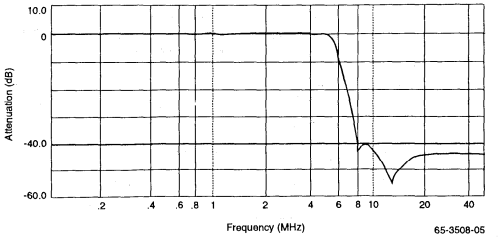


Figure 2. Amplitude Response—Default Setting

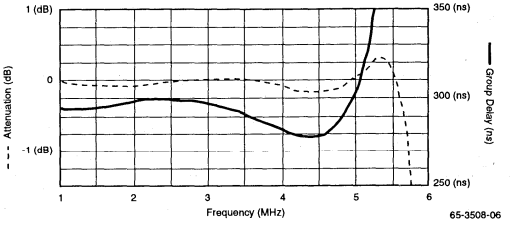


Figure 3. Attentuation and Group Delay

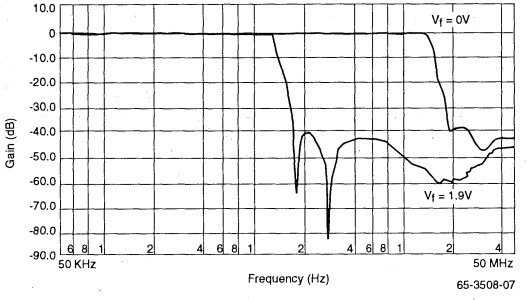


Figure 4. Amplitude Responses over Programming Range

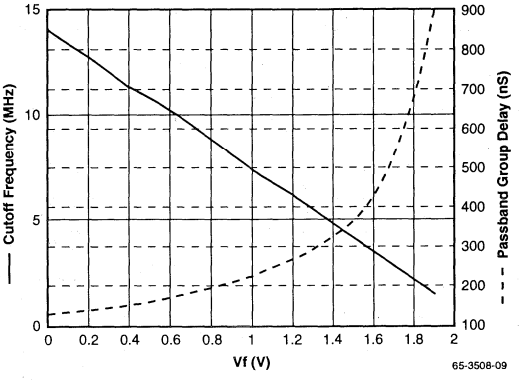


Figure 5. Frequency Programming Using V_f and Passband Group Delay

Typical Application Circuits

The RC6601 is fully integrated in the sense that no critical external components are required for the low pass filtering function. For luminance filtering at a cut-off frequency of 5.5MHz, the only off-chip components are the decoupling capacitors and termination resistors shown in Figure 6. The part also provides temperature and supply independent band-gap reference voltages (2.48V and 1.24V) that can be used for setting the ADC converters or DACs in the system.

The programmable feature of the RC6601 makes it versatile for use in applications with other standard cut-off frequencies. There are three ways of changing the cut-off frequency.

1. **External Voltage setting on V_F:** A higher voltage on V_F than 1.2V gives a lower frequency than 5.5MHz cut-off. The highest frequency (above 10MHz) is obtained by grounding the V_F pin.

2. **Potentiometer at V_{REF} (pin 8) and/or V_F (pin 9):** There is an internal resistor divider of roughly 10K each that sets the default voltage of 1.2V at half the value of V_{REF}. Using a lower value external pot of 1K–2K, the internal setting can be overridden.

3. **Current Source/Sink at V_F:** The typical current output from a DAC can be tied to the V_F pin to program the cut-off frequency from a controller.

In applications requiring dynamic programming of the filter cut-off, a combination of above techniques may be used. Use of the RC6601 in such applications eliminates the need for multiplexers and filter banks. The other adjustment possible on the RC6601 is the output d.c. level. The output d.c. level can be adjusted by connecting a potentiometer between pins R_{OS1} and R_{OS2} (pins 11 and 12) and taking the center tap to V_{CC}. These adjustments are shown in Figure 7 below.

Preliminary Information

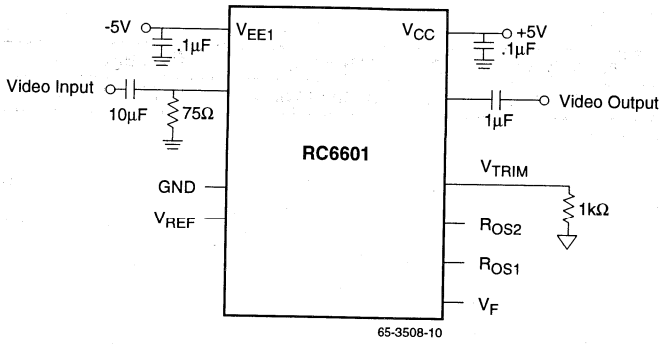


Figure 6. Fixed Filter (Cutoff Frequency Is Factory Set)

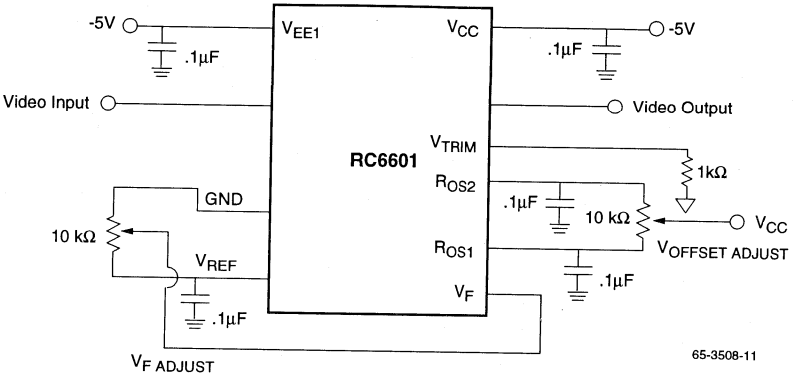


Figure 7. Programmable Filter

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6601M	0° to 70°C	Commercial	16 Pin Wide SOIC	RC6601M

RC6702

RGB to Y, C_R, C_B Transcoder

Features

- RGB to Y, C_R, C_B matrix, meets CCIR 601-1
- Thin film gain setting resistors
- External gain adjustments pins
- 60 MHz -3 dB bandwidth
- 10 MHz 0.1 dB gain flatness
- 0.06 % differential gain, $R_L \geq 150\ \Omega$
- 0.06° differential phase, $R_L \geq 150\ \Omega$
- 300 V/µS slew rate
- Dual ±5 V power supply
- Low power consumption: 70 mW per amplifier
- 16 pin SO package
- Low offset: 3.0 mV

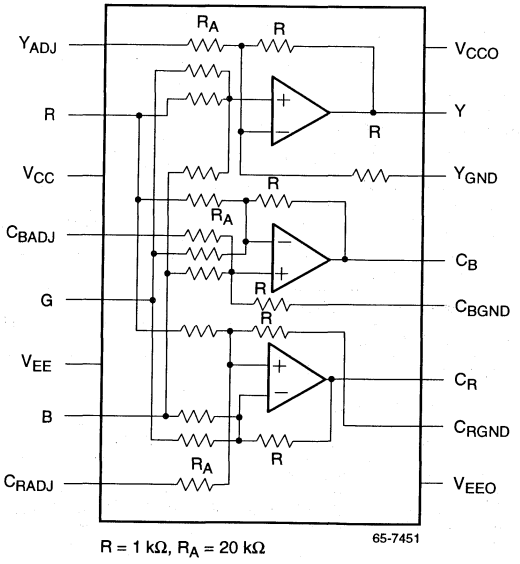
Description

The RC6702 contains three low power, wide bandwidth voltage feedback amplifiers. Internal thin film resistors perform the RGB to Y, C_R, C_B matrixing. The RGB to Y, C_R, C_B matrix is normalized to a gain of two for use in back-terminated video applications. (The sum of the absolute values of R, G and B components in a row is equal to 2.) The matrix gain accuracy is better than 1.0% and the gain temperature drift is below 25 ppm/°C.

Each transcoder has a 60 MHz bandwidth and is flat to ±0.1 dB to 10 MHz. If required, three adjustment inputs allow trimming of the Y gain and C_R, C_B white balance to accuracies better than 0.5%. A 20kΩ potentiometer between +V and -V is required, together with a 50 kΩ series resistor to adjust these offsets (see application circuit).

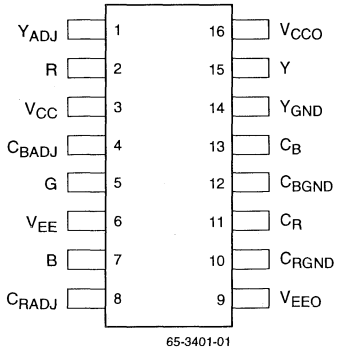
The pinout and layout of the RC6702 minimizes the crosstalk between channels. Each amplifier can drive 35 mA to the load.

Block Diagram



R = 1 kΩ, R_A = 20 kΩ

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
C_{BADJ}	4	C_B Matrix Adjustment Pin
C_{RADJ}	8	C_R Matrix Adjustment Pin
Y_{ADJ}	1	C_R Matrix Adjustment Pin
B	7	B Input
G	5	G Input
R	2	R Input
C_B	13	C_B Output
C_R	11	C_R Output
Y	15	Y Output
V_{CC}	3	+5V Supply
V_{CCO}	16	+5V Output Supply
V_{EE}	6	-5V Supply
V_{EEO}	9	-5V Output Supply
Y_{GND}	14	Y Analog Ground
C_{BGND}	12	C_B Analog Ground
C_{RGND}	10	C_R Analog Ground

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Positive power supply, V_{CC}			7	V
Negative power supply, V_{EE}			-7	V
Differential input voltage			0	V
Operating Temperature	0		+70	°C
Storage Temperature	-40		+125	°C
Junction Temperature			150	°C
Lead Soldering Temperature (10 seconds)			300	°C
Operating Temperature	0		+70	°C
Short circuit tolerance: No more than one output can be shorted to ground.				

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-4.75	-5.0	-5.25	V
θ_{JA}	SO16 Thermal Resistance		105		°C/W

DC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, R_{LOAD} = 150Ω, T_A = 0°C to 70°C, unless otherwise specified. Open Loop.

Parameter		Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	No load		±2	±7	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift[1]			±12		µV/°C
I_B	Input Bias Current [1]			±2	±10	µA
$\Delta I_B/\Delta T$	Input Bias Current Drift[1]			±10	±50	nA/°C
Rin	Input Resistance[1]		1			MΩ
Cin	Input Capacitance[1]			0.5	2	pF
CMIR	Common Mode Input Range		±2.5			V
PSRR	Power Supply Rejection Ratio	No Load	60	70		dB
Is	Quiescent Supply Current	No Load, Whole IC		25	35	mA
R_{OUT}	Output Impedance[1]	Enabled, at DC		0.2		Ω
I_{OUT}	Output Current		35			mA
V_{OUT}	Output Voltage Swing	No load	±2.5	±3.0		V
		R_L=150Ω	±2.5	±3.0		V
Y	White Balance: Gain	R = G = B = 1Vpp	1.97	2.0	2.03	Vpp
C_R, C_B	White Balance, Residual Chroma	R = G = B = 1Vpp	-10	0.0	+10	mVpp
$\Delta A_V/\Delta T$	Closed-loop Gain Drift[1]		25			ppm/°C
Resistor Matrix Characteristics						
A_V	Matrix Gain Accuracy		-1.0		+1.0	%
$\Delta A_V/\Delta T$	Matrix Gain Drift[1]			20		ppm/°C

Note:

1. Guaranteed by design.

AC Characteristics

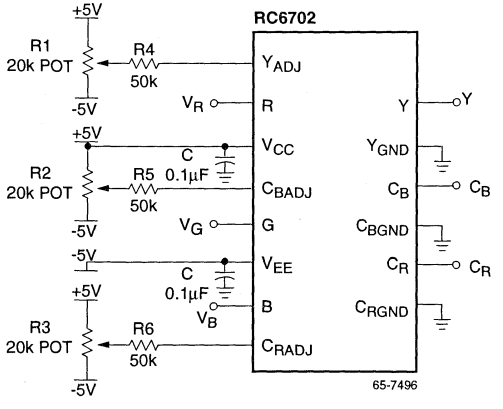
V_{CC} = 5V, V_{EE} = -5V, R_{LOAD} = 150Ω, A_V = 2, T_A = 0 to 70°C, C_L = 10 pF unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
Frequency Response						
BW	-3 dB Bandwidth (A_V = 2)[1]	V_{OUT} = 0.4 Vpp		60		MHz
		V_{OUT} = 0.8 Vpp		55		MHz
Flat	±0.1 dB Bandwidth[1]		10	15		MHz
Peak	Maximum Small Signal AC Peaking[1]			0.4		dB
Time Domain Response						
t_d	Matrix Delay[1]			20		ns
Δt_d	Output's Skew[1]			2		ns
t_{r1}, t_{f1}	Rise and Fall Time 10% to 90%[1]	2V Output Step		7	10	ns
t_s	Settling Time to 0.1 %[1]	2V Output Step		35		ns
OS	Overshoot[1]	2V Output Step		6		%
US	Undershoot[1]	2V Output Step		1.5		%
SR	Slew Rate[1]	V_{OUT} = ±2.0V	200	300		V/µs
Distortion						
HD_2	2nd Harmonic Distortion[1]	V_{OUT} = 0.8 Vpp, @ F_O = 20 MHz		-50		dB
HD_3	3nd Harmonic Distortion [1]	V_{OUT} = 0.8 Vpp, @ F_O = 20 MHz		-50		dB
Equivalent Input Noise						
NF	Noise Floor > 100 KHz[1]			-140		dBm
SND	Spectral Noise Density[1]	100 kHz to 200 MHz		10		nV/√Hz

Note:

1. Guaranteed by design.

Typical Application Circuit



RGB to Y, C_B, C_R matrix, normalized to 2

	R	G	B
Y	+0.299	+0.587	+0.114
C_B	-0.169	-0.331	±0.5
C_R	+0.5	-0.419	-0.081

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6702M	0° to 70°C	Commercial	16 Pin Narrow SOIC	RC6702M

THIS PAGE INTENTIONALLY LEFT BLANK

RC6704

Triple Fixed Gain Video Amplifier

with Separate Enable Inputs

Features

- Triple video amplifier with internal resistors to set gains to +2, +1, and -1
- Independently enabled amplifiers
- 60 MHz -3 dB Bandwidth (A_V = 2)
- 20 MHz ±0.1 dB gain flatness
- 0.06% differential gain (A_V = 2, R_L = 150Ω)
- 0.06° differential phase (A_V = 2, R_L = 150Ω)
- High CMRR (75 dB), High PSRR (70 dB)
- Dual ±5V power supply
- Low offset 2.0 mV
- 16-pin narrow SOIC package
- 300 V/µs slew rate
- Fast settling time: 0.1% in 35 ns
- Voltage gain accuracy better than 0.5%
- TTL or CMOS compatible enable inputs

Applications

- RGB amplifier
- 3:1 crosspoint switch
- RGB switch
- Video instrumentation amplifier
- Selectable gain amplifier
- Programmable filter
- Active filter

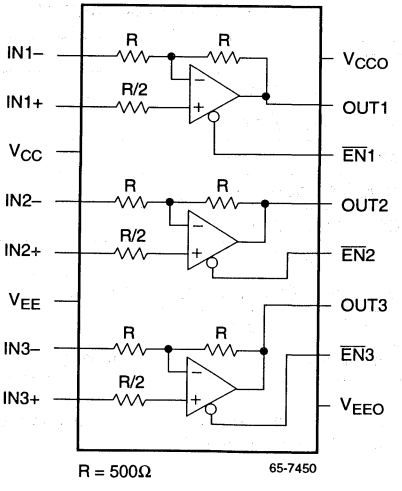
Description

The RC6704 consists of three low power, wide band voltage feedback operational amplifiers. Internal thin-film gain setting resistors provide gains of +2, +1 and -1. Each channel is capable of delivering a load current of at least 35mA.

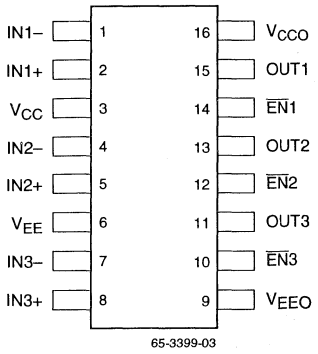
Each amplifier can be independently enabled or disabled with a TTL or CMOS signal. When disabled, the amplifier is in a high impedance output state, presenting a very high input to output isolation. The layout is optimized for low channel to channel crosstalk.

The amplifiers are optimized for video applications where low differential gain and low phase distortion are significant requirements.

Block Diagram



Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
$\overline{EN1}$	14	Enables amplifier 1 when low
$\overline{EN2}$	12	Enables amplifier 2 when low
$\overline{EN3}$	10	Enables amplifier 3 when low
IN1–	1	Amplifier 1 inverting input
IN1+	2	Amplifier 1 non-inverting input
IN2–	4	Amplifier 2 inverting input
IN2+	5	Amplifier 2 non-inverting input
IN3–	7	Amplifier 3 inverting input
IN3+	8	Amplifier 3 non-inverting input
OUT1	15	Amplifier 1 output
OUT2	13	Amplifier 2 output
OUT3	11	Amplifier 3 output
V_{CC}	3	Analog positive supply
V_{CCO}	16	Positive supply for output stages
V_{EE}	6	Analog negative supply
V_{EEO}	9	Negative supply for output stages

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Positive power supply, V_{CC}			7	V
Negative power supply, V_{EE}			-7	V
Differential input voltage			0	V
Operating Temperature	0		+70	°C
Storage Temperature	-40		+125	°C
Junction Temperature			150	°C
Lead Soldering Temperature (10 seconds)			300	°C
Operating Temperature	0		+70	°C
Short circuit tolerance: No more than one output can be shorted to ground.				

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-4.75	-5.0	-5.25	V
θ_{JA}	SO16 thermal resistance		105		°C/W

DC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, R_{LOAD} = 150Ω, T_A = 0°C to 70°C, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	No Load		±2	±5	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift[1]			±12	±50	µV/°C
I_B	Input Bias Current			±2	±10	µA
$\Delta I_B/\Delta T$	Input Bias Current Drift[1]			±10	±50	nA/°C
Rin	Input Resistance[1]		1			MΩ
Cin	Input Capacitance[1]			0.5	2	pF
CMIR	Common Mode Input Range		±2.5			V
CMRR	Common Mode Rejection Ratio	No Load	60	75		dB
PSRR	Power Supply Rejection Ratio	No Load	60	70		dB
Is	Quiescent Supply Current	No Load, Whole IC		25	35	mA
Isd	Supply Current Disabled			3	4	mA
R_{OUT}	Output Impedance[1]	Enabled, at DC		0.2		Ω
C_{OUT}	Output Capacitance[1]	Disabled		0.5		pF
I_{OUT}	Output Current		35			mA
V_{OUT}	Output Voltage Swing	No Load	±2.5	±3.0		V
		R_L = 150Ω	±2.5	±3.0		V
A_V	Closed-loop Gain		1.99	2.0	2.01	dB
$\Delta A_V/\Delta T$	Closed-loop Gain Drift[1]		25			ppm/°C
Venh	Enable High Voltage		2.4			V
Venl	Enable Low Voltage				0.8	V
Ien	Enable Input Current			3	10	µA
t_{off}	Disable Time [1]			1.0		ns
t_{on}	Enable Time [1]	Settling to 1%		200		ns

Note:

1. Guaranteed by design.

AC Characteristics

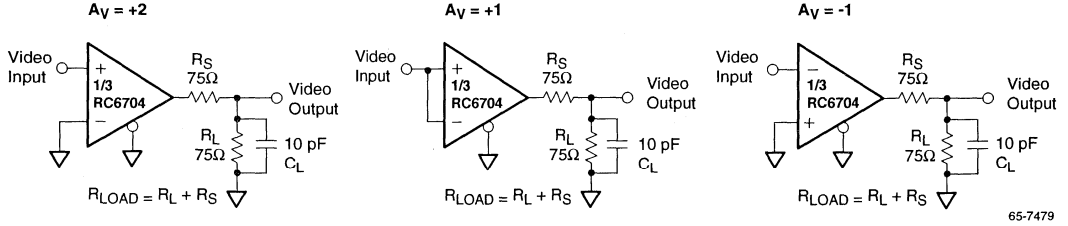
V_{CC} = 5V, V_{EE} = -5V, A_V = 2, T_A = 0 to 70°C, R_{LOAD} = 150Ω, C_L = 10 pF unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
Frequency Response						
BW	-3 dB Bandwidth (A_V = 2)[1]	V_{OUT} = 0.4 Vpp		60		MHz
		V_{OUT} = 0.8 Vpp		55		MHz
Flat	±0.1 dB Bandwidth[1]		15	20		MHz
Peak	Maximum Small Signal AC Peaking[1]			0.4	0.7	dB
ISO	Off Isolation[1]	@ 5 MHz		90		dB
XTALK	Crosstalk Isolation[1]	@ 5 MHz, R_{IN} = 50Ω		70		dB
Time Domain Response						
t_{r1}, t_{f1}	Rise and Fall Time 10% to 90%[1]	2V Output Step		7	10	ns
ts	Settling time to 0.1 %[1]	2V Output Step		35		ns
OS	Overshoot[1]	2V Output Step		6		%
US	Undershoot[1]	2V Output Step		1.5		%
SR	Slew Rate[1]	V_{OUT} = ±2.0V	200	300		V/µs
Distortion						
HD_2	2nd Harmonic Distortion[1]	V_{OUT} = 0.8 Vpp, @ FO = 20 MHz		-50		dB
HD_3	3nd Harmonic Distortion[1]	V_{OUT} = 0.8 Vpp, @ FO = 20 MHz		-50		dB
Equivalent Input Noise						
NF	Noise Floor > 100 KHz[1]			-140		dBm
SND	Spectral Noise Density[1]	100 kHz to 200 MHz		10		nV/√Hz
Video Performance						
DG	Diff. Gain (p-p), NTSC & PAL[1]	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		%
DP	Diff. Phase (p-p), NTSC & PAL[1]	R_L = 150Ω, V_{OUT} = ±1.5V		0.06		Deg.

Note:

1. Guaranteed by design.

Test Circuits



Note:

1. When driving a 75Ω cable, the source terminator resistor must be placed as close as possible to the output of the device.

Applications Discussion

Each of the three sections of the RC6704 is provided with an Enable input, thus the part is useful for selecting and multiplexing. It is suitable for selectable gain and programmable filter applications. A three-channel video multiplexer can be built with just one RC6704 and a decoder, as shown in Figure 1.

Note that RC6704 enable time is shorter than its disable time, hence a make-before-break action is provided, minimizing switching transients on the signal output.

An RGB switch is shown in Figure 2.

Capacitive Load

The RC6704 can drive a capacitive load from 10 to over 100 pF. In back terminated video applications, bandwidth will only be limited by the RC time constants of the external output components. A minimum 10 pF capacitive load is required. When driving a 75Ω cable, place the 75Ω source termination resistor as close to the amplifier output as possible.

Enable/Disable

The enable pins (10, 12, 14), when pulled to a TTL or CMOS logic low or when tied to ground, activate each amplifier individually. When pulled to a TTL or CMOS logic high, the amplifier is tri-stated and presents a high impedance at its output. When disabled the amplifier's power consumption drops, and the non-inverting input signal is isolated from its respective output.

DC Accuracy

The RC6704 is a voltage-feedback amplifier; the inverting and non-inverting inputs have similar impedances and bias currents. To minimize offset voltage, the resistances seen by inverting and non-inverting inputs must be equal.

Circuit Board

High-frequency applications require good grounding, power supply decoupling, low parasitic capacitance and inductance, and good isolation between the inputs to minimize crosstalk. Avoid coupling from output to input to prevent positive feedback.

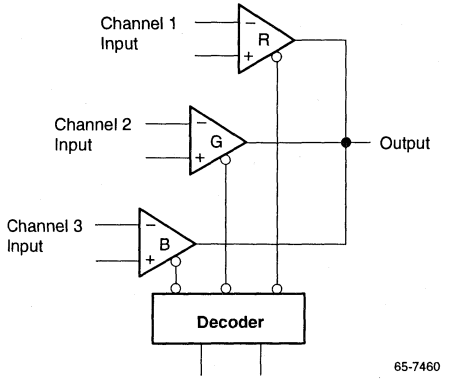


Figure 1.

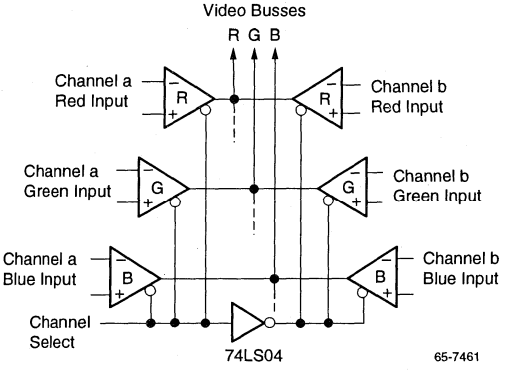


Figure 2.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6704M	0° to 70°C	Commercial	16 Pin Narrow SOIC	RC6704M

RC4190
Micropower Switching Regulator

Features

- High efficiency – 85% typical
- Low quiescent current – 215 µA
- Adjustable output – 1.3V to 30V
- High switch current – 200 mA
- Bandgap reference – 1.31V
- Accurate oscillator frequency – ±10%
- Remote shutdown capability
- Low battery detection circuitry
- Low component count
- 8-lead packages including small outline (SO-8)

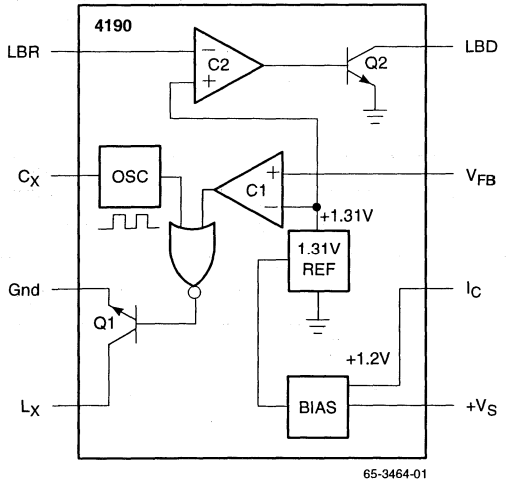
Description

The RC4190 monolithic IC is a low power switch mode regulator intended for miniature power supply applications. This DC-to-DC converter IC provides all of the active components needed to create supplies for micropower circuits (load power up to 400 mW, or up to 10W with an external power transistor). Contained internally are an oscillator, switch, reference, comparator, and logic, plus a discharged battery detection circuit.

Application areas include on-card circuits where a non-standard voltage supply is needed, or in battery operated instruments where an RC4190 can be used to extend battery lifetime.

These regulators can achieve up to 85% efficiency in most applications while operating over a wide supply voltage range, 2.2V to 30V, at a very low quiescent current drain of 215 µA.

Block Diagram



65-3464-01

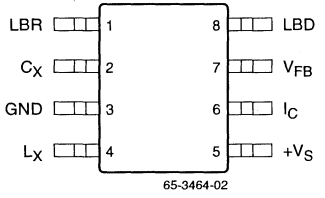
The standard application circuit requires just seven external components for step-up operation: an inductor, a steering diode, three resistors, a low value timing capacitor, and an electrolytic filter capacitor. The combination of simple application circuit, low supply current, and small package make the RC4190 adaptable to a wide range of miniature power supply applications.

The RC4190 is most suited for single ended step-up ($V_{OUT} > V_{IN}$) circuits because the NPN internal switch transistor is referenced to ground. It is complemented by another Raytheon micropower switching regulator, the RC4391, which is dedicated to step-down ($V_{OUT} < V_{IN}$) and inverting ($V_{OUT} = -V_{IN}$) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the RC4391 data sheet for step-down and inverting applications.

With some optional external components the application circuit can be designed to signal a display when the battery has decayed below a predetermined level, or designed to signal a display at one level and then shut itself off after the battery decays to a second level. See the applications section for these and other unique circuits.

The RC4190 micropower switching regulator series consists of three devices, each with slightly different specifications. The RM4190 has a 1.5% maximum output voltage tolerance, 0.2% maximum line regulation, and operation to 30V. The RC4190 has a 5.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 24V. Other specifications are identical. Each type is available in plastic and ceramic DIPs, or SO-8 packages.

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
LBR	1	Low Battery (Set) Resistor
C_X	2	Timing Capacitor
Gnd	3	Ground
L_X	4	External Inductor
$+V_S$	5	Positive Supply Voltage
I_C	6	Reference Set Current
V_{FB}	7	Feedback Voltage
LBD	8	Low Battery Detector Output

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage (Without External Transistor)	RM4190			30	V
	RC4190			24	V
$P_D T_A < 50°C$	SOIC			300	mW
	PDIP			468	mW
	CerDIP			833	mW
Operating Temperature	RM4190	-55		125	°C
	RC4190	0		70	°C
Storage Temperature		-65		150	°C
Junction Temperature	SOIC, PDIP		125		°C
	CerDIP		175		°C
Switch Current	Peak			375	mA
For $T_A > 50°C$ Derate at	SOIC		4.17		mW/°C
	PDIP		6.25		mW/°C
	CerDIP		8.33		mW/°C

Note:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
θ_{JA}	Thermal resistance	SOIC		200		°C/W
		PDIP		160		°C/W
		CerDIP		120		°C/W

Electrical Characteristics

(+V_S = +6.0V, I_C = 5.0 µA over the full operating temperature range unless otherwise noted.)

Symbol	Parameters	Conditions	RM4190			RC4190			Units
			Min	Typ	Max	Min	Typ	Max	
+V_S	Supply Voltage		2.6		30	2.6		24	V
V_{REF}	Reference Voltage (Internal)		1.25	1.31	1.37	1.20	1.31	1.42	V
I_{SY}	Supply Current	Measure at Pin 5 I_4 = 0		235	350		235	350	µA
	Line Regulation	0.5 V_{OUT} < V_S < V_{OUT}		0.2	0.5		0.5	1.0	% V_O
L_I	Load Regulation	V_S = 0.5 V_{OUT} P_L = 150 mW		0.5	1.0		0.5	1.0	% V_O
I_C	Reference Set Current		1.0	5.0	50	1.0	5.0	50	µA
I_{CO}	Switch Leakage Current	V_4 = 24V (RC4190) 30V (RM4190)			30			30	µA
I_{SO}	Supply Current (Disabled)	V_C ≤ 200 mV			30			30	µA
I_{LBD}	Low Battery Output Current	V_8 = 0.4V, V_1 = 1.1V	500	1200		500	1200		µA
	Oscillator Frequency Temperature Drift			±200			±200		ppm/°C

Electrical Characteristics

(+V_S = +6.0V, I_C = 5.0 µA, and T_A = +25°C unless otherwise noted.)

Symbol	Parameters	Conditions	RM4190			RC4190			Units
			Min	Typ	Max	Min	Typ	Max	
$+V_S$	Supply Voltage		2.2		30	2.2		24	V
V_{REF}	Reference Voltage (Internal)		1.29	1.31	1.33	1.24	1.31	1.38	V
I_{SW}	Switch Current	V_4 = 400 mV	100	200		100	200		mA
I_{SY}	Supply Current	Measure at Pin 5 I_4 = 0		215	300		215	300	µA
ef	Efficiency			85			85		%
	Line Regulation	0.5 V_{OUT} < V_S < V_{OUT}		0.04	0.2		0.04	0.5	% V_O
L_I	Load Regulation	V_S = +0.5 V_{OUT} P_L = 150 mW		0.2	0.5		0.2	0.5	% V_O
F_O	Operating Frequency Range		0.1	25	75	0.1	25	75	kHz
I_C	Reference Set Current		1.0	5.0	50	1.0	5.0	50	µA
I_{CO}	Switch Leakage Current	V_4 = 24V (RC4190) 30V (RM4190, RC4190A)		0.01	5.0		0.01	5.0	µA
I_{SO}	Supply Current (Disabled)	$V_C \leq$ 200 mV		0.1	5.0		0.1	5.0	µA
I_1	Low Battery Bias Current	V_1 = 1.2V		0.7			0.7		µA
I_{CX}	Capacitor Charging Current			8.6			8.6		µA
	Oscillator Frequency Tolerance			±10			±10		%
$+V_{THX}$	Capacitor Threshold Voltage +			1.4			1.4		V
$-V_{THX}$	Capacitor Threshold Voltage –			0.5			0.5		V
I_{FB}	Feedback Input Current	V_7 = 1.3V		0.1			0.1		µA
I_{LBD}	Low Battery Output Current	V_8 = 0.4V, V_1 = 1.1V	500	1500		500	1500		µA

Typical Performance Characteristics

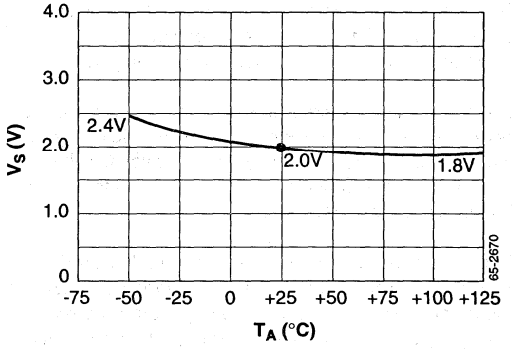


Figure 1. Minimum Supply Voltage vs. Temperature

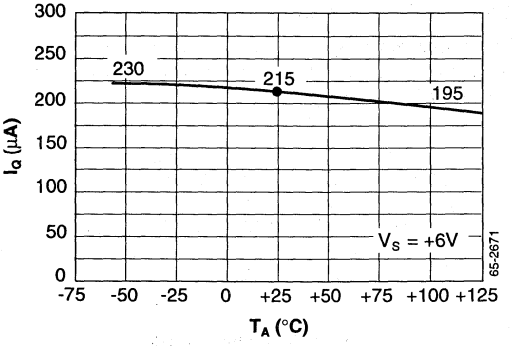


Figure 2. Quiescent Current vs. Temperature

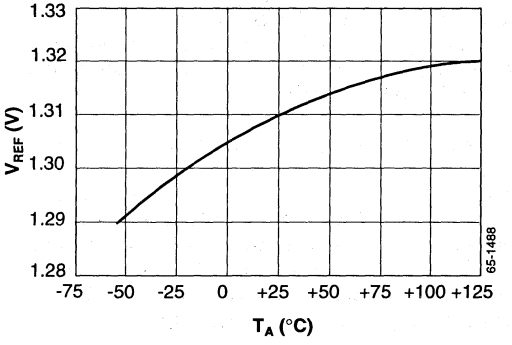


Figure 3. Reference Voltage vs. Temperature

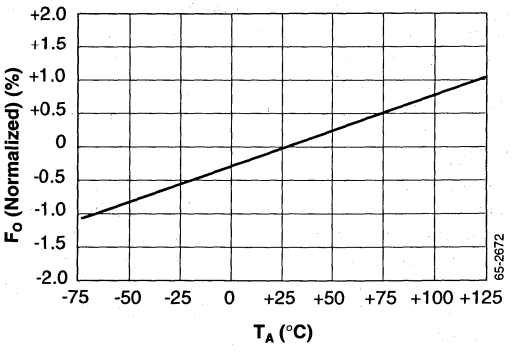


Figure 4. Oscillator Frequency vs. Temperature

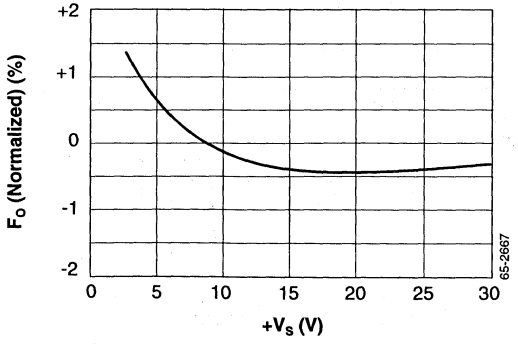


Figure 5. Minimum Supply Voltage vs. Temperature

Principles of Operation

Simple Step-Up Converter

The most common application, the step-up regulator, is derived from a simple step-up ($V_{OUT} > V_{BAT}$) DC-to-EC Converter (Figure 6).

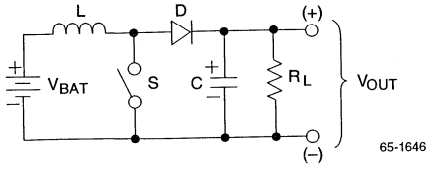


Figure 6. Simple Set-Up

When switch S is closed, the battery voltage is applied across the inductor L. Charging current flows through the inductor, building up a magnetic field, increasing as the switch is held closed. While the switch is closed, the diode D is reverse biased (open circuit) and current is supplied to the load by the capacitor C. Until the switch is opened, the inductor current will increase linearly to a maximum value determined by the battery voltage, inductor value, and the amount of time the switch is held closed ($I_{MAX} = V_{BAT}/L \times T_{ON}$). When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a discharge current which flows through the inductor in the same direction as the charging current. Because there is no path for current to flow through the switch, the current must flow through the switch, the current must flow through the diode to supply the load and charge the output capacitor.

If the switch is opened and closed repeatedly, at a rate much greater than the time constant of the output RC, then a constant dc voltage will be produced at the output.

An output voltage higher than the input voltage is possible because of the high voltage produced by a rapid change of current in the inductor. When the switch is opened, the inductor voltage will instantly rise high enough to forward bias the diode, to $V_{OUT} + V_D$.

In the complete RC4190 regulator, a feedback control system adjusts the on time of the switch, controlling the level of inductor current, so that the average inductor discharge current equals the load current, thus regulating the output voltage.

Complete Step-Up Regulator

A complete schematic of the minimum step-up application is shown in Figure 7. The ideal switch in the DC-to-DC Converter diagram is replaced by an open collector NPN transistor Q1. C_F functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the current in R1 supplies bias current to pin 6 (I_C). This current is stabilized by a unity gain current source amplifier and then used as bias current for the 1.31V bandgap reference. A very stable bias current generated by the bandgap is mirrored and used to bias the remainder of the chip. At the same time the RC4190 is starting up, current will flow through the inductor and the diode to charge the output capacitor to $V_{BAT} - V_D$.

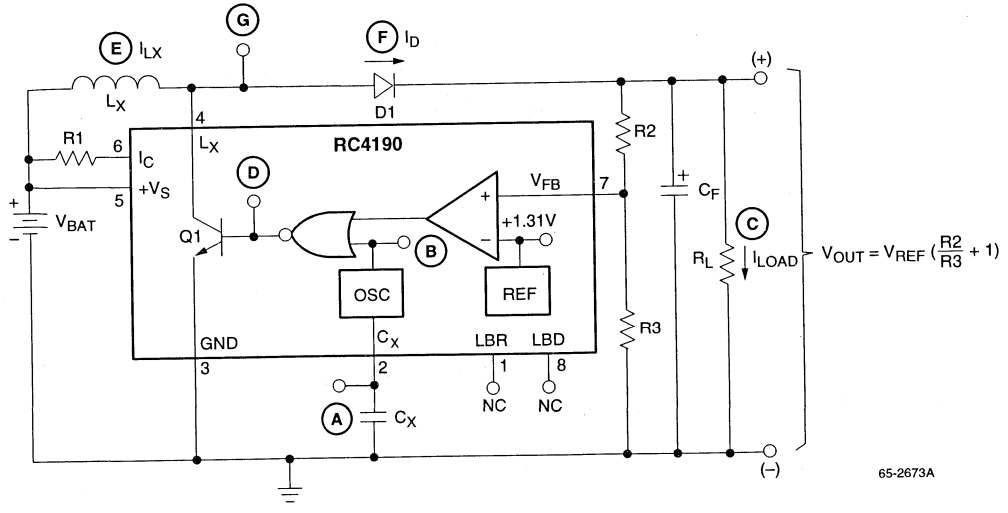


Figure 7. Complete Step-Up Regulator

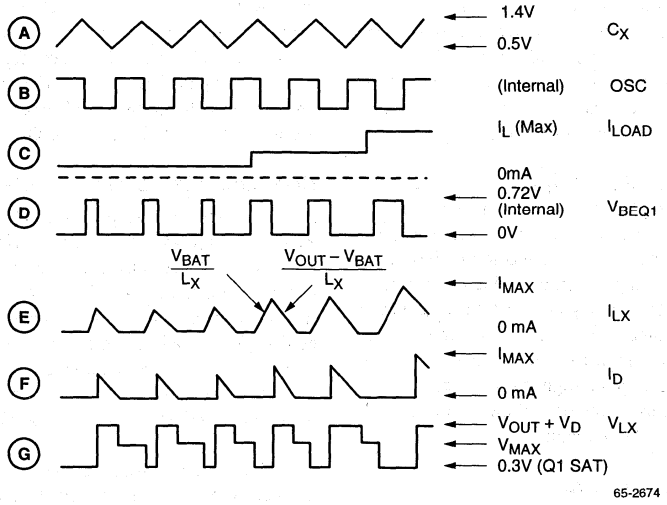


Figure 8. Step-Up Regulator Waveforms

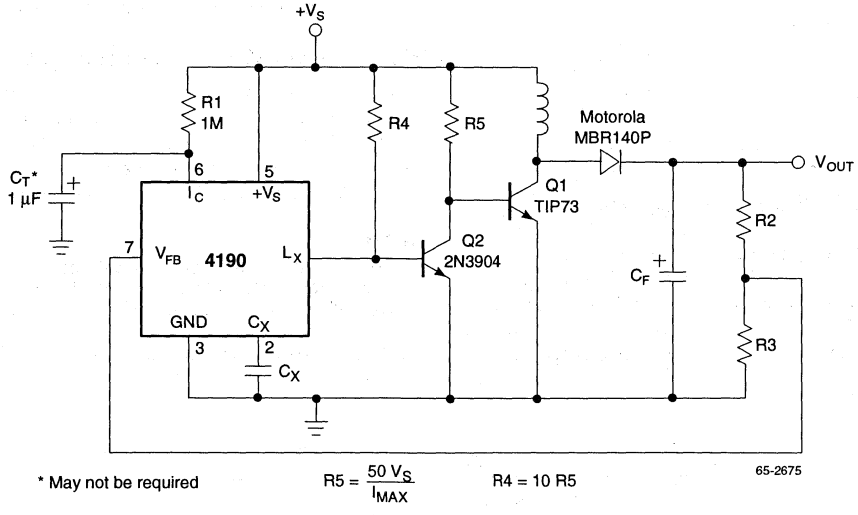


Figure 9. High Power Step-Up Regulator
(With the addition of a power transistor (TIP73) and a few components, the 4190 can accomodate load power up to 10W.)

At this point, the feedback (pin 7) senses that the output voltage is too low, by comparing a division of the output voltage (set by the ratio of R2 to R3) to the +1.31V reference. If the output voltage is too low then the comparator output changes to a logical zero. The NOR gate then effectively ANDs the oscillator square wave with the comparator signal; if the comparator output is zero AND the oscillator output is low, then the NOR gate output is high and the switch transistor will be forced on. When the oscillator goes high again, the NOR gate output goes low and the switch transistor will turn off. This turning on and off of the switch transistor performs the same function that opening and closing the switch in the simple DC-to-DC Converter does; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

The comparator will continue to allow the oscillator to turn the switch on and off until enough charge has been delivered to the capacitor to raise the feedback voltage above 1.31V.

Thereafter, this feedback system will vary the duration of the on time in response to changes in load current or battery

voltage (see Figure 8). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle (waveform B), thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and time.

The inductor value and oscillator frequency must be carefully tailored to the battery voltage, output current, and ripple requirements of the application (refer to the Design Equations Section). If the inductor value is too high or the oscillator frequency is too high, then the inductor current will never reach a value high enough to meet the load current drain and the output voltage will collapse. If the inductor value is too low or the oscillator frequency too low, then the inductor current will build up too high, causing excessive output voltage ripple, or over stressing of the switch transistor, or possibly saturating the inductor.

Simple Step-Down Converter

Figure 10 shows a step-down DC-to-DC Converter ($V_{OUT} \leq V_{BAT}$) with no feedback control.

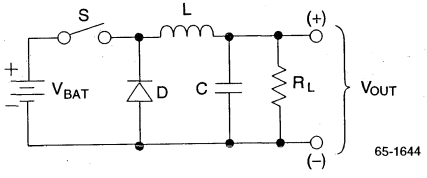


Figure 10. Simple Step-Down Converter

When S is closed, the battery voltage minus the output voltage is applied across the inductor. All of the inductor current will flow into the load until the inductor current exceeds the load current. The excess current will then charge the capacitor and the output voltage will rise. When S is opened, the voltage applied across the inductor will discharge into the load. As in the step-up case, the average inductor current equals the load current. The maximum inductor current I_{MAX} will equal $(V_{BAT} - V_{OUT})/L$ times the maximum on time of the switch transistor (T_{ON}). Current flows to the load during both half cycles of the oscillator.

Complete Step-Down Regulator

Most step-down applications are better served by the RC4391 step-down and inverting switching regulator (refer to the RC4391 data sheet). However, there is a range of load power for which the RC4190 has an advantage over the RC4391 in step-down applications. From approximately 500 mW to 2W of load power, the RC4190 step-down circuit of Figure 6 offers a lower component count and simpler circuit than the comparable RC4391 circuit, particularly when stepping down a voltage greater than 30V.

Since the switch transistor in the RC4190 is in parallel with the load, a method must be used to convert it to a series connection for step-down applications. The circuit of Figure 11 accomplishes this. The 2N2907 replaces S of Figure 10, and R6 and R7 are added to provide the base drive to the 2N2907 in the correct polarity to operate the circuit properly.

Greater Than 30V Step-Down Regulator

Adding a zener diode in series with the base of the 2N2907 allows the battery voltage to increase by the value of the zener, with only a slight decrease in efficiency. As an example, if a 24V zener is used, the maximum battery voltage can go to $48V^2$ when using a RC4190. Refer to Figure 12.

Notes:

1. The addition of the zener diode will not alter the maximum change of supply. With a 24V zener, the circuit will stop operating when the battery voltage drops below 24V + 2.2V = 26.2V.
2. Maximum battery voltage is 54V when using RM4190 (30V + 24V).

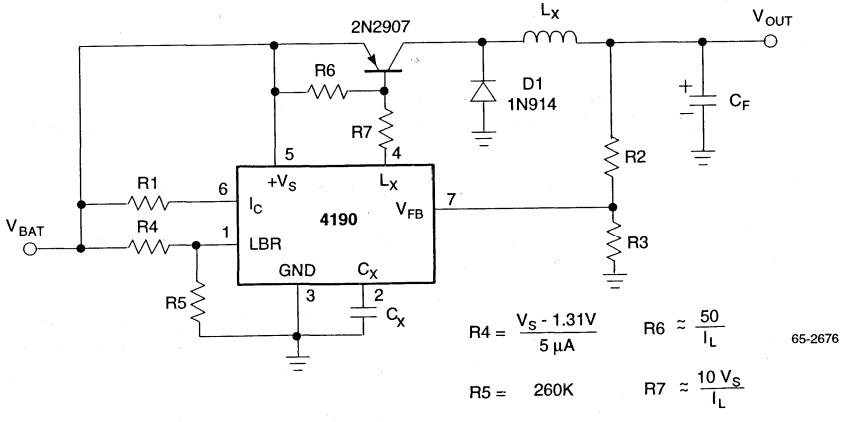


Figure 11. Complete Step-Down Regulator

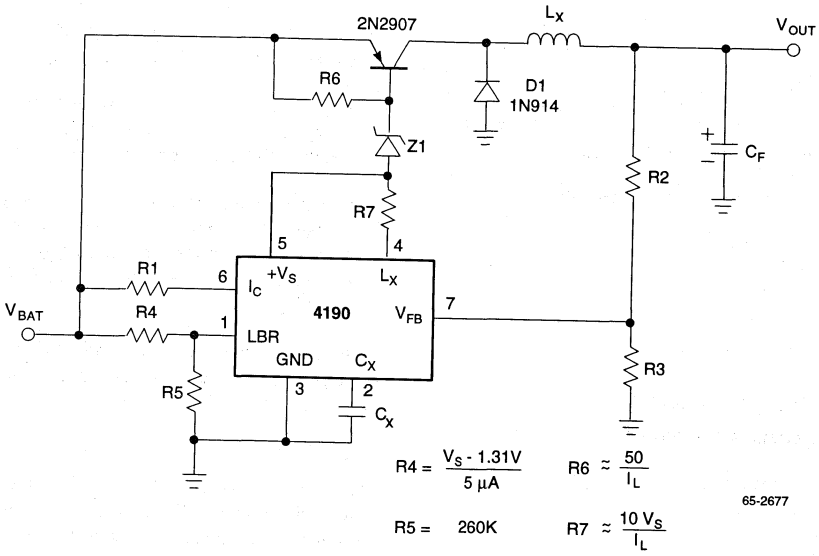


Figure 12. Step-Down Regulator Greater Than 30V

Design Equations

The inductor value and timing capacitor (C_X) value must be carefully tailored to the input voltage, input voltage range, output voltage, and load current requirements of the application. The key to the problem is to select the correct inductor value for a given oscillator frequency, such that the inductor current rises to a high enough peak value (I_{MAX}) to meet the average load current drain. The selection of this inductor value must take into account the variation of oscillator frequency from unit to unit and the drift of frequency over temperature. Use ±20% as a maximum change from the nominal oscillator frequency.

The worst-case conditions for calculating ability to supply load current are found at the minimum supply voltage; use $+V_S$ (min) to calculate the inductor value. Worst-case conditions for ripple are at $+V_S$ (max).

The value of the timing capacitor is set according to the following equation:

$$f_O\,(Hz) = \frac{2.4 \times 10^6}{C_X\,(pF)}$$

The squarewave output of the oscillator is internal and cannot be directly measured, but is equal in frequency to the triangle waveform measurable at pin 4. The switch transistor is normally on when the triangle waveform is ramping up and off when ramping down. Capacitor selection depends on the application; higher operating frequencies will reduce the output voltage ripple and will allow the use of an inductor with a physically smaller inductor core, but excessively high frequencies will reduce load driving capability and efficiency.

Find a value for the start-up resistor R1:

$$R1 = \frac{V_S - 1.2V}{5\mu A}$$

Find a value for the feedback resistors R2 and R3:

$$R2 = \frac{V_{OUT} - 1.31V}{I_A}$$

$$R3 = \frac{1.31V}{I_A}$$

Where I_A is the feedback divider current (recommended value is between 50 µA and 100 µA).

Step-Up Design Procedure

1. Select an operating frequency and timing capacitor as shown above (10 kHz to 40kHz is typical).

2. Find the maximum on time (add 5 µS for the turn-off base recombination delay of Q1):

$$T_{ON} = \frac{1}{2F_O} + 5\mu s$$

3. Calculate the peak inductor current I_{MAX} (if this value is greater than 375 mA, then an external power transistor must be used in place of Q1):

$$I_{MAX} = \left(\frac{V_{OUT} + V_D - V_S}{(F_O)\,T_{ON}\,[V_S - V_{SW}]}\right) 2I_L$$

where: V_S = supply voltage
V_D = diode forward voltage
I_L = dc load current
V_{SW} = saturation voltage of Q1 (typ 0.5V)

4. Find an inductance value for L_X:

$$L_X(\text{Henries}) = \left(\frac{V_S - V_{SW}}{I_{MAX}}\right) T_{ON}$$

5. The inductor chosen must exhibit approximately this value at a current level equal to I_{MAX}.

6. Calculate a value for the output filter capacitor:

$$C_F(\mu F) = \frac{T_{ON}\left(\frac{V_S I_{MAX}}{V_{OUT}} + I_L\right)}{V_R}$$

where V_R = ripple voltage (peak)

Step-Down Design Procedure

1. Select an operating frequency.

2. Determine the maximum on time (T_{ON}) as in the step-up design procedure.

3. Calculate I_{MAX}:

$$I_{MAX} = \frac{2I_L}{(F_O)(T_{ON})\left(\frac{V_S - V_{OUT}}{V_{OUT} - V_D}\right) + 1}$$

4. Calculate L_X:

$$L_X = \left(\frac{V_S - V_{OUT}}{I_{MAX}}\right)(T_{ON})$$

5. Calculate a value for the output filter capacitor:

$$C_F(\mu F) = \frac{T_{ON}\left(\frac{(V_S - V_{OUT})\, I_{MAX}}{V_{OUT}} + I_L\right)}{V_R}$$

Alternate Design Procedure

The design equations above will not work for the certain input/output voltage ratios, and for these circuits another method of defining component values must be used. If the slope of the current discharge waveform is much less than the slope of the current charging waveform, then the inductor current will become continuous (never discharging completely), and the equations will become extremely complex. So, if the voltage applied across the inductor during the charge time is greater than during the discharge time, used the design procedure below. For example, a step-down circuit with 20V input and 5V output will have approximately 15V across the inductor when charging, and approximately 5V when discharging. So in this example, the inductor current will be continuous and the alternate procedure will be necessary.

1. Select an operating frequency (a value between 10 kHz and 40 kHz is typical).

2. Build the circuit and apply the worst case conditions to it, i.e., the lowest battery voltage and the highest load current at the desired output voltage.

3. Adjust the inductor value down until the desired output voltage is achieved, then go a little lower (approximately 20%) to cover manufacturing tolerances.

4. Check the output voltage with an oscilloscope for ripply, at high supply voltages, at voltages as high as are expected. Also check for efficiency by monitoring supply and output voltages and currents [eff = (V_{OUT})(I_{OUT})/(+V_S)(I_{SY}) x 100%$].

5. If the efficiency is poor, go back to (1) and start over. If the ripple is excessive, then increase the output filter capacitor value or start over.

Compensation

When large values (>50 kΩ) are used for the voltage setting resistors, R2 and R3 of Figure 7, stray capacitance at the V_{FB} input can add a lag to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This can often be avoided by minimizing the stray capacitance at the V_{FB} node. It can also be remedied by adding a lead compensation capacitor of 100 pF to 10 nF in parallel with R2 in Figure 7.

Inductors

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite pot core is recommended; the wind-yourself type with an air gap adjustable by washers or spacers is very useful for breadboarding prototypes. Care must be taken to choose a permeable enough core to handle the magnetic flux produced at I_{MAX}; if the core saturates, then efficiency and output current capability are severely degraded and excessive current will flow though the switch transistor. A pot core inductor design section is provided later in this datasheet.

An isolated AC current probe for an oscilloscope (example: Tektronix P6042) is an excellent tool for saturation problems; with it the inductor current can be monitored for nonlinearity at the peaks (a sign of saturation).

Low Battery Detector

An open collector signal transistor Q2 with comparator C2 provides the designer with a method of signaling a display or computer whenever the battery voltage falls below a programmed level (see Figure 8). This level is determined by the +1.3V reference level and by the selection of two external resistors according to the equation:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

Where V_{TH} = Threshold Voltage for Detection

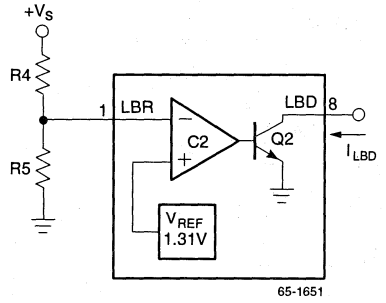


Figure 13. Low Battery Detector

When the battery voltage drops below this threshold Q2 will turn on and sink over 1500 µA typically. The low battery detector circuitry may also be used for other, less conventional applications (see Figures 19 and 20).

Automatic Shutdown

The bias control current for the reference is externally set by a resistor from the IC pin to the battery. This current can vary from 1.0 µA to 50 µA without affecting the operation of the IC. Interrupting this current will disable the entire circuit, causing the output voltage to go to 0V for step-down applications, and reducing the supply current to less than 1.0 µA.

Automatic shutdown of the RC4190 can be achieved using the circuit of Figure 14.

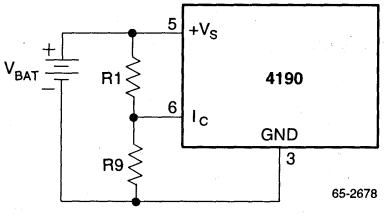


Figure 14. Automatic Shutdown

A resistor is placed from the IC pin to ground, creating a voltage divider. When the voltage at the IC pin is less than 1.2V, the RC4190 will begin to turn off. This scheme should only be used in limited temperature range applications since the "turn off" voltage at the IC pin has a temperature coefficient of -4.0 mV/°C. At 25°C, typically 250 nA is the minimum current required by the IC pin to sustain operation. A 5.0 µA voltage divider works well taking into account the sustaining current of 250 nA and a threshold voltage of 0.4V at turn off. As an example, if 3.0V is to be the turn off voltage, then R9 = 1.1/4.75 µA and R1 = (3.0 – 1.1) 5.0 µA or about 240 kΩ and 390 kΩ respectively. The tempco at the top of the divider will be -4.0 mV (R1 + R9)/R9 or -10.5 mV/°C, an acceptable number for many applications.

Another method of automatic shutdown without temperature limitations is the use of a zener diode in series with the IC pin and set resistor. When the battery voltage falls below VZ + 1.2V the circuit will start to shut down. With this connection and the low battery detector, the application can be designed to signal a display when the battery voltage has dropped to the first programmed level, then shut itself off as the battery reaches the zener threshold.

The set current can also be turned off by forcing the IC pin to 0.2V or less using an external transistor or mechanical switch. An example of this is shown in Figure 15.

In this circuit an external control voltage is used to determine the operating state of the RC4190. If the control voltage VC is a logic 1 at the input of the 4025 (CMOS Triple NOR Gate), the voltage at the IC pin will be less than 0.5V forcing the 4190 off (<0.1 µA ICC). Both the 2N3904 and 2N2907 will be off insuring long shelf for the battery since less than 1.0 µA is drawn by the circuit.

When VC goes to a logic 0, 2.0 µA is forced into the IC pin through the 2.2 MΩ resistor and the NOR gate, and at the same time the 2N3904 and 2N2907 turn on, connecting the battery to the load.

As long as VC remains low the circuit will regulate the output to 5.0V. This type of circuit is used to back up the main supply voltage when line interruptions occur, a particularly useful feature when using volatile memory systems.

9.0V Battery Life Extender

Figure 16 shows a common application: a circuit to extend the lifetime of a 9.0V battery. The regulator remains in its quiescent state (drawing only 215 µA) until the battery voltage decays below 7.5V, at which time it will start to switch and regulate the output at 7.0V until the battery falls below 2.2V.

If this circuit operates at its typical efficiency of 80%, with an output current of 10 mA, at 5.0V battery voltage, then the average input current will be IIN = (VOUT x IL) + (VBAT x ef) or (7.0V x 10 mA) + (5.0V x 0.8 mA) = 17.5 mA.

Bootstrapped Operation (Step-Up)

In step-up applications, power to the RC4190 can be derived from the output voltage by connecting the +VS pin and the top of R1 to the output voltage (Figure 17).

One requirement for this circuit is that the battery voltage must be greater than 3.0V when it is energized or else there will not be enough voltage at pin 5 to start up the IC. The big advantage of this circuit is the ability to operate down to a discharged battery voltage of 1.0V.

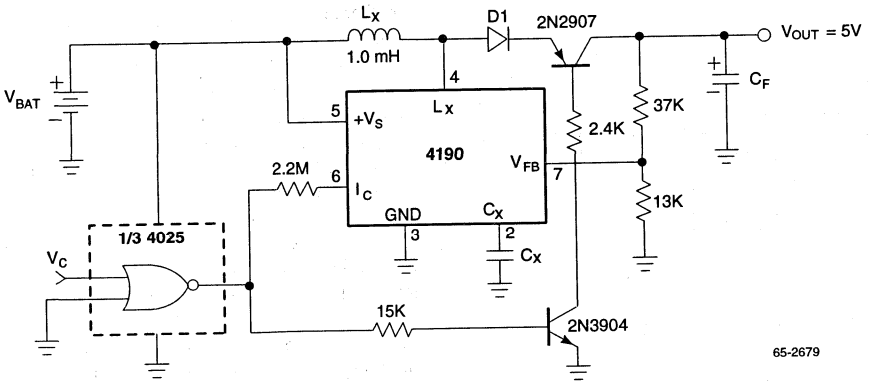


Figure 15. Battery Back-Up Circuit

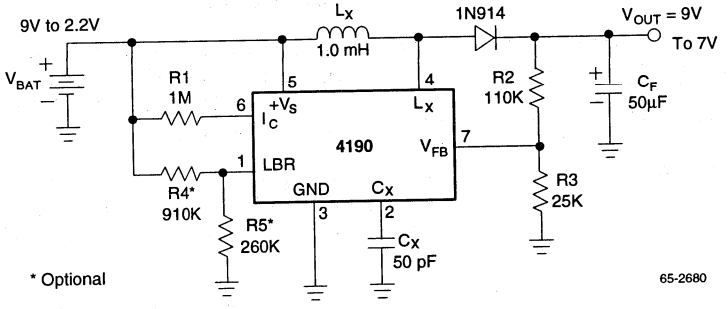


Figure 16. 9.0V Battery Life Extender

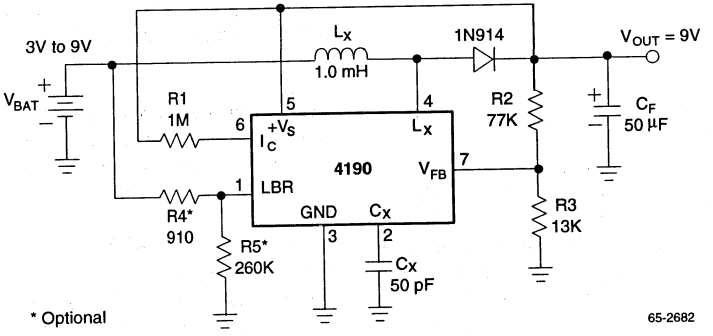


Figure 17. Bootstrapped Operation (Step-Up)

Buck-Boost Circuit (Step-Up/Down)

A disadvantage of the standard step-up and step-down circuits is the limitation of the input voltage range; for a step-up circuit, the battery voltage must always be less than the programmed output voltage, and for a step-down circuit, the battery voltage must always be greater than the output voltage. The following circuit eliminates this disadvantage, allowing a battery voltage above the programmed output voltage to decay to well below the output voltage (see Figure 18).

The circuit operation is similar to the step-up circuit operation, except that both terminal of the inductor are connected to switch transistors. This switching method allows the inductor to be disconnected from the battery during the time the inductor is being discharged. A new discharge path is provided by D1, allowing the inductor to be referenced to ground and independent of the battery voltage. The efficiency of this circuit will be reduced to 55-60% by losses in the extra switch transistor and diode. Efficiency can be improved by choosing transistors with low saturation voltages and by using power Schottky diodes such as Motorola's MBR030.

Step-Up Voltage Dependent Oscillator

The RC4190's ability to supply load current at low battery voltages depends on the inductor value and the oscillator frequency. Low values of inductance or a low oscillator frequency will cause a higher peak inductor current and therefore increase the load current capability. A large inductor current is not necessarily best, however, because the large amount of energy delivered with each cycle will cause a large voltage ripple at the output, especially at high input voltages. This trade-off between load current capability and output ripple can be improved with the circuit connection shown in Figure 19. This circuit uses the low battery detector to sense for a low battery voltage condition and will decrease the oscillator frequency after a pre-programmed threshold is reached.

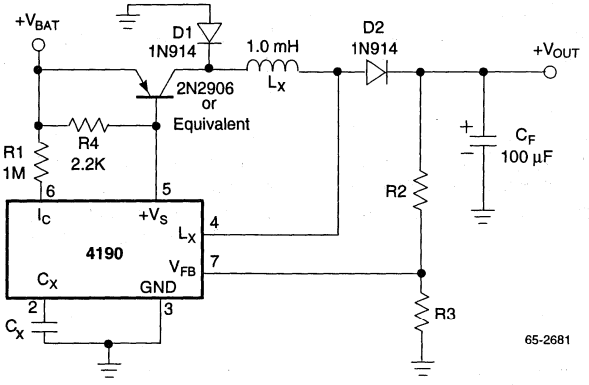


Figure 18. Buck Boost Circuit (Step-Up/Down)

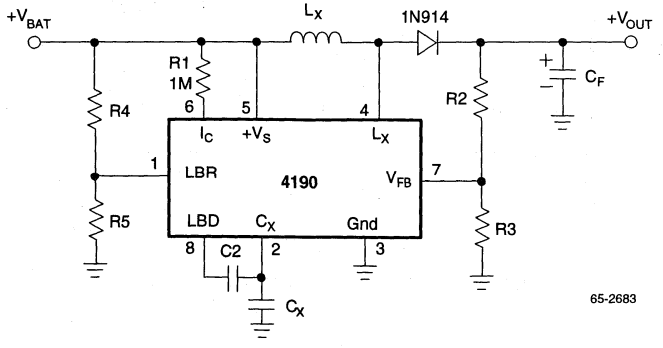


Figure 19. Step-Up Voltage Dependent Oscillator

The threshold is programmed exactly as the noram low battery detector connection:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

When the battery voltage reaches this threshold, the comparator will turn on the open collector transistor at pin 8, effectively putting C2 in parallel with C_X. This added capacitance will reduce the oscillator frequency according to the following equation:

$$F_O = \frac{2.4 \times 10^{-6}}{C_X + C2}$$

Where C is in pF and F_O is in Hz.

Component values for a typical application might be R2 = 330 kΩ, R5 = 150 kΩ, C_X = 100 pF, and C2 = 100 pF. These values would set the threshold voltage at 4.1V and change the operating frequency from 48 kHz to 24 kHz. Note that this technique may be used for step-up, step-down, or inverting applications.

Step-Down Regulator With Protection

One disadvantage of the simple application circuits is their lack of short circuit protection, especially for the step-up circuit, which has a very low resistance path for current flow from the input to the output. A current limiting circuit which senses the output voltage and shuts down the 4190 if the output voltage drops too low can be built using the low battery detector circuitry. The low battery detector is connected to sense the output voltage and will shut off the oscillator by forcing pin 2 low if the output voltage drops. Figure 20 shows a schematic of a step-down regulator with this connection.

R2 and R3 set the output voltage, as in the circuit of Figure 2. Choose resistor values so R5 = R3 and R4 = R2, and make R8 25 to 35 times higher than R3. When the output is shorted, the open collector transistor at pin 8 will force pin 2 low and shut off the oscillator and therefore shut off the external switch transistor. The regulator will then remain in a low current off condition until power is removed and reapplied. C2 provides momentary current to ensure proper start-up. This scheme will not work with the simple step-up regulator, but will work with the boost-buck converter, providing short circuit protection in both step-up and step-down modes.

RC4190/RC4391 ± Power Supply

A positive and negative dual tracking power supply using a step-up RC4190 and an inverting RC4391 is shown in Figure 21. The inductor and capacitor values were chosen to achieve the highest practical output currents from a +12V battery, as it decays, while keeping the output voltage ripple under 100 mV_{p-p} at ±15V output.

The circuit may be adapted to other voltages and currents, but note that the RC4190 is step-up, so V_{OUT} must be greater than V_{BAT}.

The output voltages may both be trimmed by adjusting a single resistor value (R3 or R4), because the reference for the negative output is derived from $+V_{OUT}$. This connection also allows the output voltages to track each other with changes in temperature and line voltage.

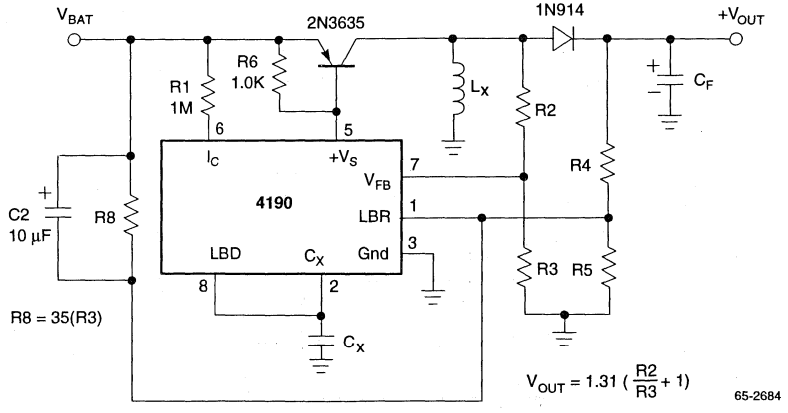


Figure 21. Step-Down Regulator with Protection

The timing capacitors are set up exactly as in the voltage dependent oscillator application of Figure 19. The values of R2, R5, C6, and C4 that are given were chosen to optimize for the +12V battery conditions, setting the threshold for oscillator frequency change at V_{BAT} = +8.5V.

As given, this power supply is capable of delivering +45 mA and -15 mA with regulation, until the battery decays below 5.0V.

For information on adjusting the RC4391 to meet a specific application refer to the Raytheon RC4391 data sheet.

Negative Step-Up Regulator

In the circuit of Figure 22, a bootstrap arrangement of supply and ground pins helps generate an output voltage more negative than the input voltage. On power-up, the output filter capacitor (C_F) will charge through D2 and L_X. When the voltage goes below -2.4V, the RC4190 begins switching and charging C_F. The output will regulate at a value equal to the reference voltage (1.31V) plus the zener voltage of D1. R_Z sets the value of zener current, stabilized at 1.31V/R2.

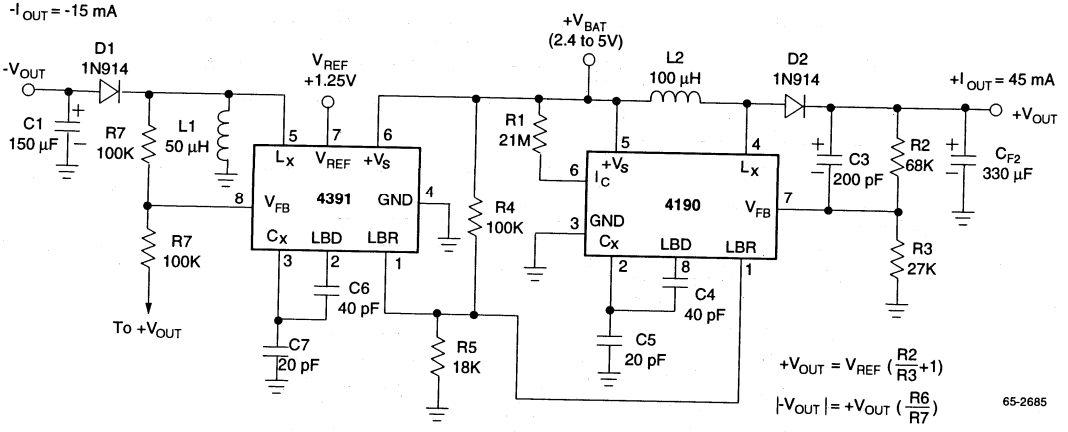


Figure 21. RC4190/RC4391 Power Supply (±15V)

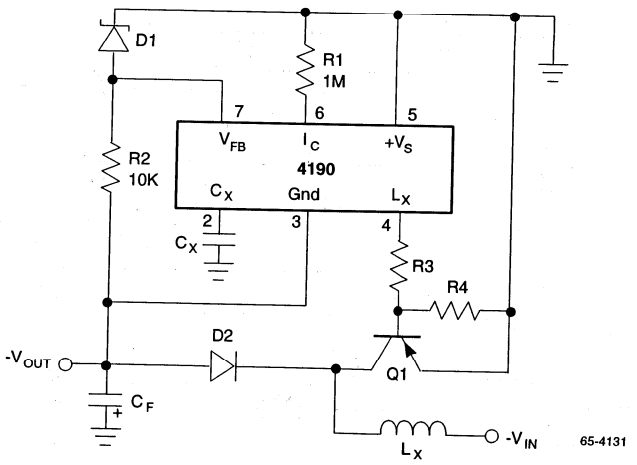
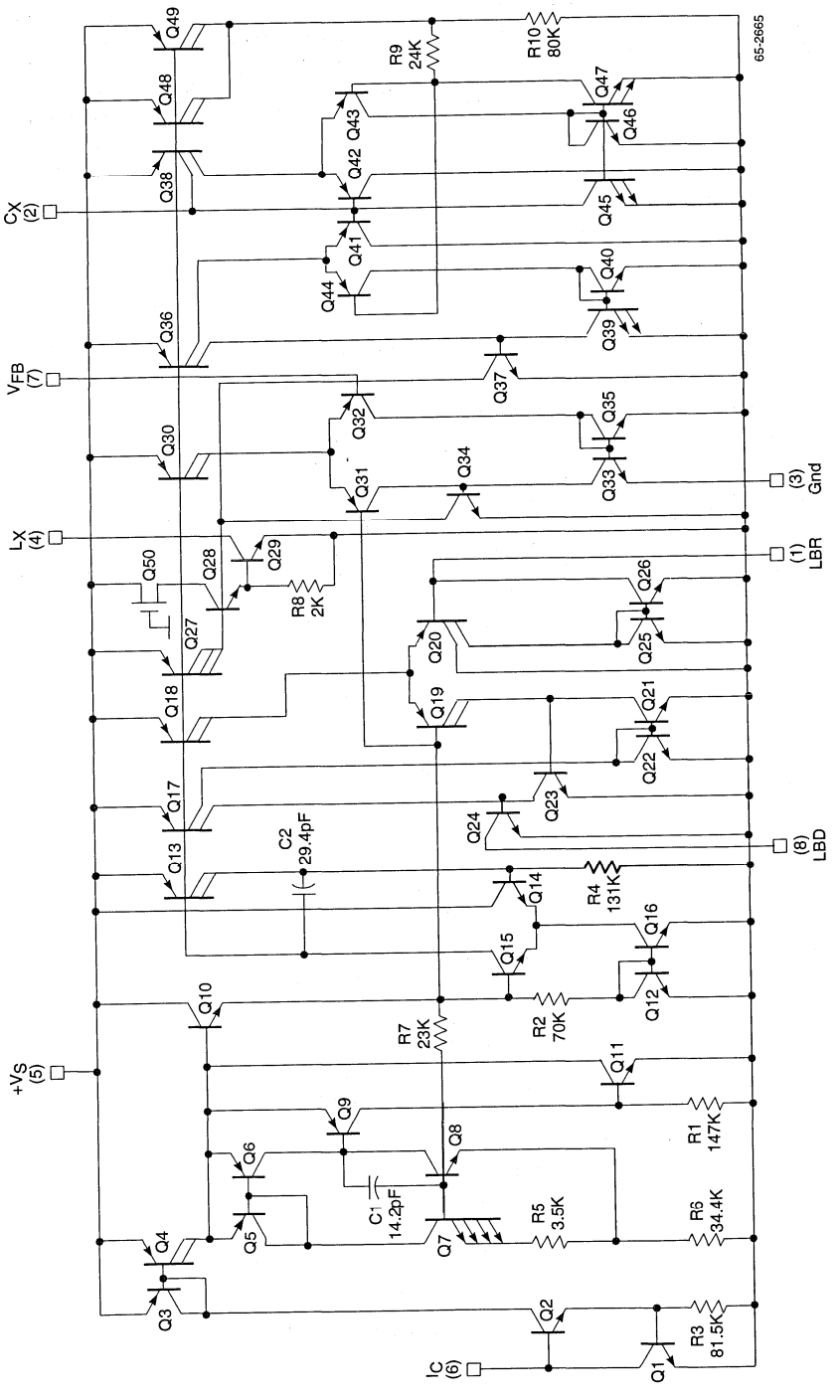
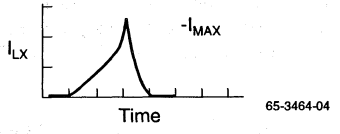
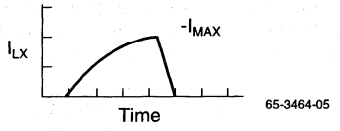
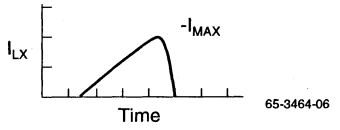


Figure 22. Negative Step-Up Regulator

Simplified Schematic Diagram



Troubleshooting Chart

Symptom	Possible Problem
Draws excessive supply current on start-up	Battery not "stiff" — inadequate supply bypass capacitor.
	Inductance value too low.
	Operating frequency (F_O) too low.
Output voltage is low.	Inductance value too high for F_O or core saturating.
Inductor "sings" with audible hum.	Not potted well or bolted loosely.
L_X in appears noisy — scope will not synchronize.	Normal operating condition.
Inductor current shows nonlinear waveform.  	Inductor is saturating: 1. Core too small. 2. Core too hot. 3. Operating frequency too low.
Inductor current shows nonlinear waveform.  	Waveform has resistive component: 1. Wire size too small. 2. Power transistor lacks base drive. 3. Components not rated high enough. 4. Battery has high series resistance.
Inductor current is linear until high current is reached.  	External transistor lacks base drive or beta is too low.
Poor efficiency.	Core saturating.
	Diode or transistor: 1. Not fast enough. 2. Not rated for current level (high V_{CE} SAT).
	High series resistance.
	Operating frequency too high.
Motorboating (erratic current pulses).	Loop stability problem — needs feedback capacitor from V_{OUT} to V_{FB} (pin 7), 100 to 1000 pF.

Background Information

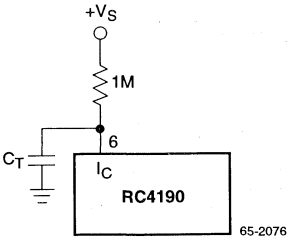
During the past several years there have been various switching regulator ICs introduced by many manufacturers, all of which attended to the same market, namely controllers for use in power supplies delivering greater than 10W of DC power. Raytheon felt there was another area which could use a switching regulator to even more advance the area of battery powered equipment. Battery powered systems have problems peculiar unto themselves: changes in supply voltage, space considerations, battery life and usually cost. The RC4190 was designed with each of these in mind.

The RC4190 was partitioned to work in an eight pin package, making it smaller than other controllers which go into 14 and 16 pin packages.

Battery powered applications require the load as seen by the battery to be as small as possible to extend battery life. To this end, the quiescent current of the RC4190 is 15 to 100 times less than controllers designed for nonbattery applications. At the same time, the switch transistor can sink 200 mA at 0.4V, comparable to or better than higher powered controllers. As an example, the 4190 configured in the step-up mode can supply 5.0V at 40 mA output with an input of 3.0V.

Cost is usually a primary consideration in battery powered systems. The RC4190, guaranteed to work down to 2.2V, can save the designer and end user money as well because battery costs decrease as the number of cells needed goes down.

Soft Start



The delay introduced by the RC time constant at start-up allows the output filter capacitor to charge up, reducing the instantaneous supply current. A typical value for C is in the 0.1µF range.

Bootstrapped Low Voltage Start-Up

Figure 24 shows the bootstrapped application can be "kicked on" using an extra capacitor and triple pole double throw switch (3PDT). This connection allows the circuit to start up using a single Ni-Cad cell of 1.2V to 1.6V. When power is first applied the 1.2V battery does not provide enough voltage to meet the minimum 2.2V supply voltage requirement. The 22µF capacitor, when switched, temporarily doubles the battery voltage to bias up the RC4190.

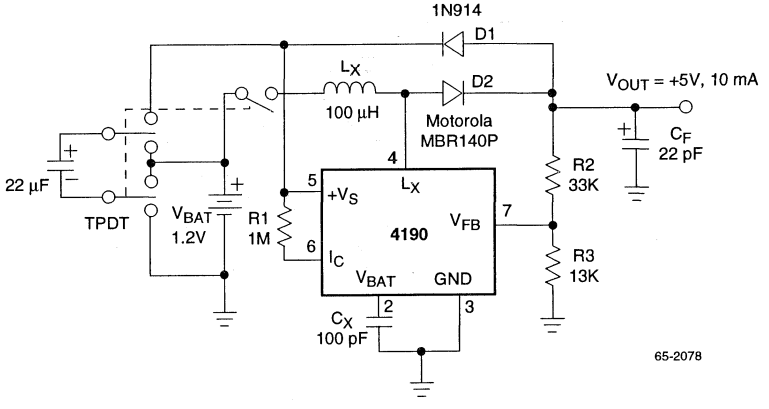


Figure 24. Bootstrapped Low Voltage Start-Up

When the switch is the down position, the capacitor charges up to the battery voltage. The, when the switch is changed to the up position, the capacitor is put in series connection with the battery, and the doubled voltage is applied directly to the positive power supply lead of the RC4190. This voltage is enough to bias the junctions internal to the RC4190 and gets it started. Then, when the stepped up output voltage reaches a high enough value, diode D1 is forward biased and the output voltage takes over supplying power to the RC4190. The circuit is shown with component values for +5V output, but the circuit can be set up for other voltages.

Electricity Versus Magnetism

Electrically the inductor must meet just one requirement, but that requirement can be hard to satisfy. The inductor must exhibit the correct value of inductance (L, in Henrys) as the inductor current rises to its highest operating value (I_{MAX}). This requirement can be met most simply by choosing a very large core and winding it until it reaches the correct inductance value, but that brute force technique wastes size, weight and money. A more efficient design technique must be used.

Question: What happens if too small a core is used?

First, one must understand how the inductor's magnetic field works. The magnetic circuit in the inductor is very similar to a simple resistive electrical circuit (see Figure 20). There is a magnetizing force (H, in oersteds), a flow of magnetism, or flux density (B, in Gauss), and resistance to the flux, called permeability (U, in Gauss per oersted). H is equivalent to voltage in the electrical model, flux density is like current flow, and permeability is like resistance (except for two important differences discussed on the following page).

First Difference: Permeability, instead of being analogous to resistance, is actually more like conductance (1/R). As permeability increases, flux increases.

Second Difference: Resistance is a linear function. As voltage increases, current increases proportionally, and the resistance value stays the same. In a magnetic circuit the value of permeability varies as the applied magnetic force varies. This nonlinear characteristic is usually shown in graph form in ferrite core manufacturer's data sheets. See Figure 26.

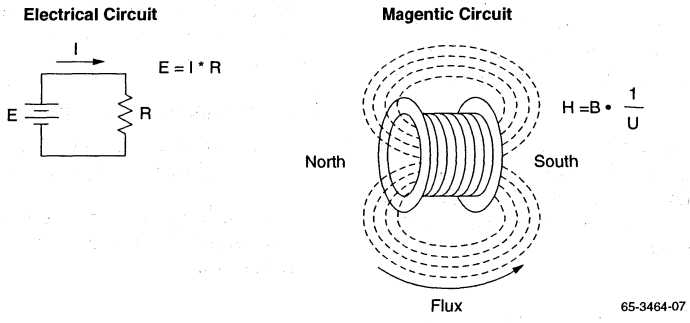


Figure 25. Electricity Versus Magnetism

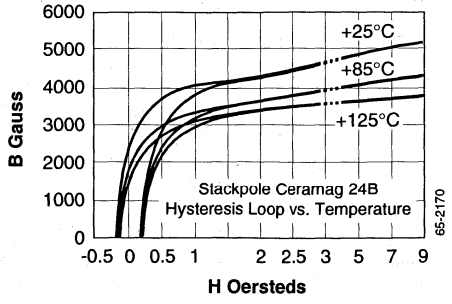


Figure 26. Typical Manufacturer's Curve Showing Saturation Effect

As the applied magnetizing force increases, at some point the permeability will start decreasing, and therefore the amount of magnetic flux will not increase any further, even as the magnetizing force increases. The physical reality is that, at the point where the permeability decreases, the magnetic field has realigned all of the magnetic domains in the core material. Once all of the domains have been aligned the core will then carry no more flux than just air; it becomes as if there were no core at all. This phenomenon is called saturation. Because the inductance value, L, is dependent on the amount of flux, core saturation will cause the value of L to decrease dramatically, in turn causing excessive and possibly destructive inductor current.

Pot Cores for RC4190

Pot core inductors are best suited for the RC4190 micropower switching regulator for several reasons:

1. **They are available in a wide range of sizes.** RC4190 applications are usually low power with relatively low peak currents (less than 500mA). A small inexpensive pot core can be chosen to meet the circuit requirements.

2. **Pot cores are easily mounted.** They can be bolted directly to the PC card adjacent to the regulator IC.

3. **Pot cores can be easily air-gapped.** The length of the gap is simply adjusted using different washer thicknesses. Cores are also available with predetermined air gaps.

4. **Electromagnetic interference (EMI) is kept to a minimum.** The completely enclosed design of pot core reduces stray electromagnetic radiation—an important consideration of the regulator circuit is built on a PC card with other circuitry.

Core Size

Question: Is core size selected according to load power?

Not quite. Core size is dependent on the amount of energy stored, not on load power. Raising the operating frequency allows smaller cores and windings. Reduction of the size of the magnetics is the main reason switching regulator design tends toward higher operating frequency. Designs with the RC4190 should use 75kHz as a maximum running frequency, because the turn off delay of the power transistor and stray capacitive coupling begin to interfere. Most applications are in the 10 to 50kHz range, for efficiency and EMI reasons.

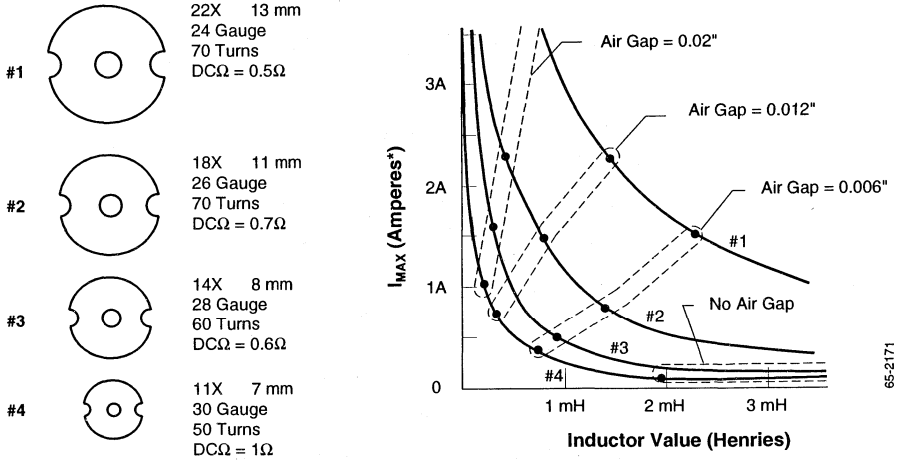
The peak inductor current (I_{MAX}) must reach a high enough value to meet the load current drain. If the operating frequency is increased, and simultaneously the inductor value is decreased, then the core can be made smaller. For a given core size and winding, an increase in air gap spacing (an air gap is a break in the material in the magnetic path, like a section broken off a doughnut) will cause the inductance to decrease and I_{MAX} (the usable peak current before saturation) to increase.

The curves shown in Figure 26 are typical of the ferrite manufacturer's power HF material, such as Siemens N27 or Stackpole 24B, which are usually offered in standard millimeter sizes including the sizes shown.

Use of the Design Aid Graph (Figure 27)

1. From the application requirement, determine the inductor value (L) and the required peak current (I_{MAX}).

2. Observe the curves of the design aid graph and determine the smallest core that meets both the L and I requirements.



*Includes safety margin (25%) to ensure nonsaturation

Figure 27. Inductor Design Aid

3. Note the approximate air gap at I_{MAX} for the selected core, and order the core with the gap. (If the gapping is done by the user, remember that a washer spacer results in an air gap of twice the washer thickness, because two gaps will be created, one at the center post and one at the rim, like taking two bites from a doughnut.)

4. If the required inductance is equal to the indicated value on the graph, then wind the core with the number of turns shown in table of sizes. The turns given are the maximum number for that gauge of wire that can be easily wound in the cores winding area.

5. If the required inductance is less than the value indicated on the graph, a simple calculation must be done to find the adjusted number of turns. Find A_L (inductance index) for a specific air gap.

$$\frac{L\,(\text{indicated})}{\text{Turns}^2} = A_L$$

in Henrys/turn^2

Then divide the required inductance value by A_L to give the actual turns squared, and take the square root to find the actual turns needed.

$$\text{ActualTurns} = \frac{L\,(\text{required})}{A_L}$$

If the actual number of turns is significantly less than the number from the table then the wire size can be increased to use up the left-over winding area and reduce resistive losses.

6. Wind and gap the core as per calculations, and measure the value with an inductance meter. Some adjustment of the number of turns may be necessary.

The saturation characteristics may be checked with the inductor wired into the switching regulator application circuit. To do so, build and power up the circuit. Then (recommend Tektronix P6042 or equivalent) around the inductor lead and monitor the current in the inductor. Draw the maximum load current from the application circuit so that the regulator is running at close to full duty cycle.

Compare the waveform you see to those pictured in Figure 28.

Check for saturation at the highest expected ambient temperature.

7. After the operation in circuit has been checked, reassemble and pot the core using a potting compound recommended by the manufacturer.

If the core material differs greatly in magnetic characteristics from the standard power material shown in Figure 22, then the following general equation can be used to help in winding and gapping. This equation can be used for any core geometry, such as an E-E core.

$$L_X = \frac{(1.26)\,(N^2)\,(Ae)\,(10^8)}{g = (le)/(ue)}$$

Where: N = number of turns
Ae = core area from data sheet (in cm2)
le = magnetic path length from data sheet (in cm)
ue = permeability of core from manufacturer's graph
g = center post air gap (in cm)

Manufacturers

Below is a list of several pot core manufacturers:

Ferroxcube Company
5083 Kings Highway
Saugerties, NY 12477

Indiana General Electronics
Keasley, NJ 08832

Siemens Company
186 Wood Avenue South
Isclin, NJ 08830

Stackpole Company
201 Stackpole Street
St. Mary, PA 15857

TDK Electronics
13-1-Chome
Nihonbaski, Chuo-ku, Tokyo

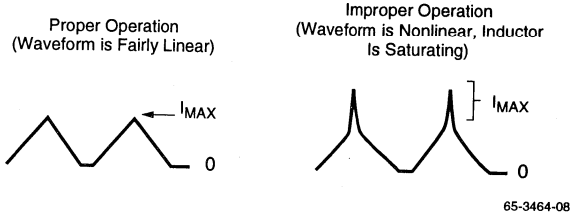


Figure 28. Inductor Current Waveforms

Ordering Information

Product Number	Temperature Range	Screening	Package
RC4190M	0° to 70°C	Commercial	8 Pin Narrow SOIC
RC4190N	0° to 70°C	Commercial	8 Pin Plastic DIP
RM4190D	-55°C to +125°C		8 Pin Ceramic DIP
RM4190D/883B	-55°C to +125°C	Military	8 Pin Ceramic DIP
RV4190N	-25°C to +85°C	Industrial	8 Pin Plastic DIP

Note:

1. /883B suffix denotes MIL-STD-883, Level B processing.

RC4191/RC4192/RC4193

Micropower Switching Regulator

Features

- High efficiency – 85% typical
- Low quiescent current – 215 µA
- Adjustable output – 1.3V to 30V
- High switch current – 200 mA
- Bandgap reference – 1.31V
- Accurate oscillator frequency – ±10%
- Remote shutdown capability
- Low battery detection circuitry
- Low component count
- 8-lead packages

Description

The RC4191/4192/4193 series of monolithic ICs are low power switch mode regulators intended for miniature power supply applications. These DC-to-DC converter ICs provide all of the active components needed to create supplies for micropower circuits. Contained internally are an oscillator, switch, reference, comparator, and logic, plus a discharged battery detection circuit.

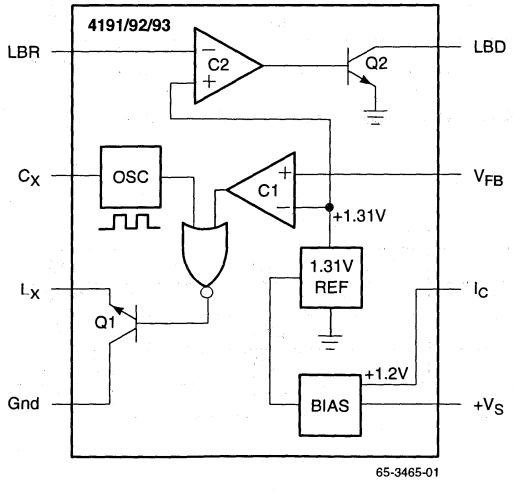
These regulators can achieve up to 85% efficiency in most applications while operating over a wide supply voltage range, 2.2V to 30V, at a very low quiescent current drain of 215 µA.

The standard application circuit requires just seven external components for step-up operation: an inductor, a steering diode, three resistors, a low value timing capacitor, and an electrolytic filter capacitor. The combination of simple application circuit, low supply current, and small package make the RC4193 adaptable to a wide range of miniature power supply applications.

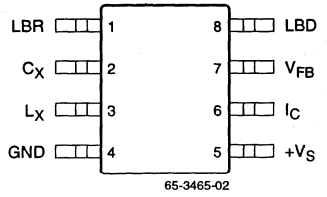
The RC4193 is most suited for single ended step-up ($V_{OUT} > V_{IN}$) circuits because the NPN internal switch transistor is referenced to ground. It is complemented by Raytheon's micropower switching regulator, the RC4391, which is dedicated to step-down ($V_{OUT} < V_{IN}$) and inverting $V_{OUT} = -V_{IN}$) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the RC4391 data sheet for step-down and inverting applications.

The RC4191/92/93 series of micropower switching regulators consists of three devices, each with slightly different specifications. The RM4191 has a 1.5% maximum output voltage tolerance, 0.2% maximum line regulation, and operation to 30V. The RC4192 has a 3.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 30V. The RC4193 has a 5.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 24V. Other specifications are identical for the RC4191, RC4192 and RC4193. Each type is available in commercial, industrial, and military temperature ranges, and in plastic and ceramic DIPs and S0-8 packages.

Block Diagram



Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
LBR	1	Low Battery (Set) Resistor
C_X	2	Timing Capacitor
L_X	3	External Inductor
Gnd	4	Ground
$+V_S$	5	Positive Supply Voltage
I_C	6	Reference Set Current
V_{FB}	7	Feedback Voltage
LBD	8	Low Battery Detector Output

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage (Without External Transistor)	4191, 4192			30	V
	4193			24	V
$P_D T_A < 50°C$	SOIC			300	mW
	PDIP			468	mW
	CerDIP			833	mW
Operating Temperature	RM4191/2/3	-55		125	°C
	RV4191/2/3	-25		85	°C
	RC4191/2/3	0		70	°C
Storage Temperature		-65		150	°C
Junction Temperature	SOIC, PDIP		125		°C
	CerDIP		175		°C
Switch Current	Peak			375	mA
For $T_A > 50°C$ Derate at	SOIC		4.17		mW/°C
	PDIP		6.25		mW/°C
	CerDIP		8.33		mW/°C

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
θ_{JA}	Thermal resistance	SOIC		240		°C/W
		PDIP		160		°C/W
		CerDIP		150		°C/W

Electrical Characteristics

(+V_S = +6.0V, I_C = 5.0 µA over the full operating temperature range unless otherwise noted.)

Parameters		Conditions	4191			4192			4193			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$+V_S$	Supply Voltage		2.6		30	2.6		30	2.6		24	V
V_{REF}	Reference Voltage (Internal)		1.25	1.31	1.37	1.23	1.31	1.39	1.20	1.31	1.42	V
I_{SY}	Supply Current	Measure at Pin 5 I_3 = 0		225	350		235	350		225	350	µA
	Line Regulation	0.5 V_O < V_S < V_O		0.2	0.5		0.5	1.0		0.5	1.0	% V_O
L_I	Load Regulation	V_S = 0.5 V_O P_L = 150 mW		0.5	1.0		0.5	1.0		0.5	1.0	% V_O
I_C	Reference Set Current		1.0	5.0	50	1.0	5.0	50	1.0	5.0	50	µA
I_{CO}	Switch Leakage Current	V_3 = 24V (4193) 30V (4191, 4192)			30			30			30	µA
I_{SO}	Supply Current (Disabled)	$V_C \leq$ 200 mV			30			30			30	µA
I_{LBD}	Low Battery Output Current	V_8 = 0.4V, V_1 = 1.1V	400	1200		400	1200		400	1200		µA
	Oscillator Frequency Temperature Drift			±200			±200			±200		ppm/ °C

Electrical Characteristics

(+V_S = +6.0V, I_C = 5.0 µA, and T_A = +25°C unless otherwise noted.)

Parameters		Conditions	4191			4192			4193			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
+V_S	Supply Voltage		2.2		30	2.2		30	2.2		24	V
V_{REF}	Reference Voltage (Internal)		1.29	1.31	1.33	1.27	1.31	1.35	1.24	1.31	1.38	V
I_{SW}	Switch Current	V_3 = 400 mV	100	200		100	200		100	200		mA
I_{SY}	Supply Current	Measure at Pin 5 I_3 = 0		215	300		215	300		215	300	µA
ef	Efficiency			85			85			85		%
	Line Regulation	0.5 V_O < V_S < V_O		0.04	0.2		0.04	0.5		0.04	0.5	% V_O
L_I	Load Regulation	V_S = +0.5 V_{OUT} P_L = 150 mW		0.2	0.5		0.2	0.5		0.2	0.5	% V_O
F_O	Operating Frequency Range		0.1	25	75	0.1	25	75	0.1	25	75	kHz
I_C	Reference Set Current		1.0	5.0	50	1.0	5.0	50	1.0	5.0	50	µA
I_{CO}	Switch Leakage Current	V_3 = 24V (4193), 30V (4191/2)		0.01	5.0		0.01	5.0		0.01	5.0	µA
I_{SO}	Supply Current (Disabled)	V_C ≤ 200 mV		0.1	5.0		0.1	5.0		0.1	5.0	µA
I_1	Low Battery Bias Current	V_1 = 1.2V		0.7			0.7			0.7		µA
I_{CX}	Capacitor Charging Current			8.6			8.6			8.6		µA
	Oscillator Frequency Tolerance			±10			±10			±10		%
+V_{THX}	Capacitor Threshold Voltage +			1.4			1.4			1.4		V
-V_{THX}	Capacitor Threshold Voltage –			0.5			0.5			0.5		V
I_{FB}	Feedback Input Current	V_7 = 1.3V		0.1			0.1			0.1		µA
I_{LBD}	Low Battery Output Current	V_8 = 0.4V, V_1 = 1.1V	500	1500		500	1500		500	1500		µA

Typical Performance Characteristics

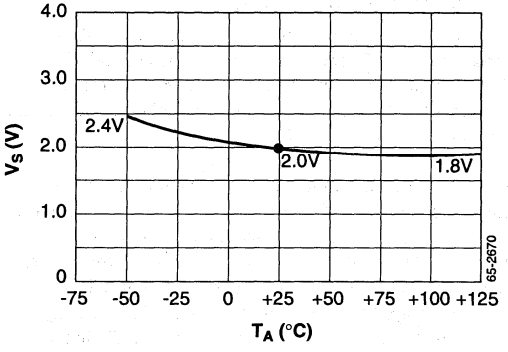


Figure 1. Minimum Supply Voltage vs. Temperature

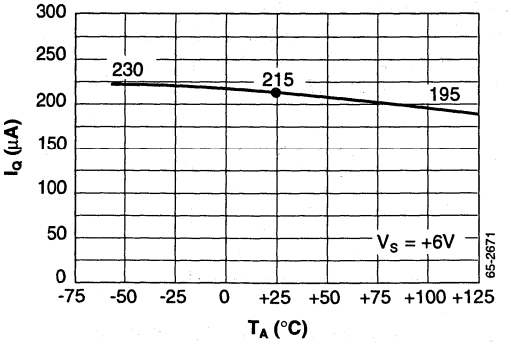


Figure 2. Quiescent Current vs. Temperature

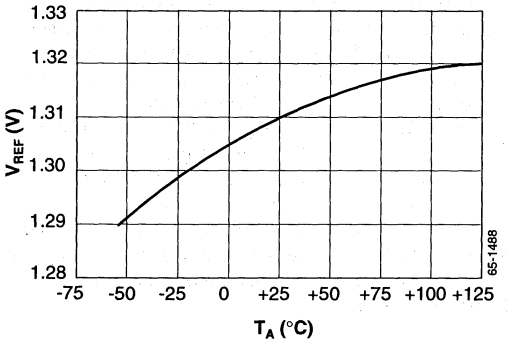


Figure 3. Reference Voltage vs. Temperature

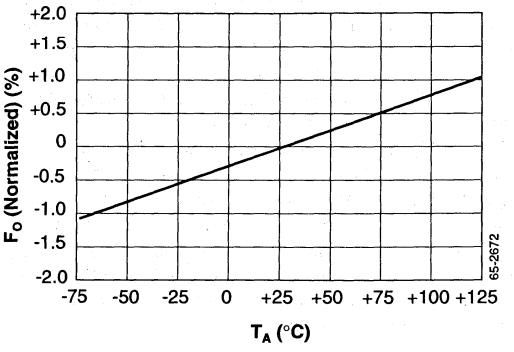


Figure 4. Oscillator Frequency vs. Temperature

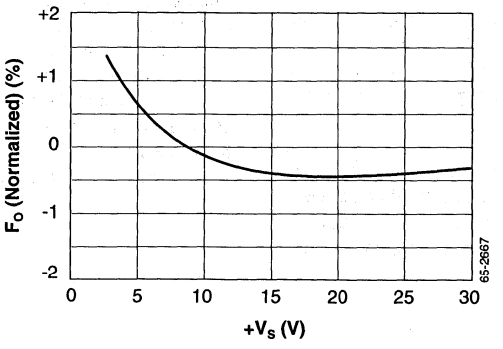


Figure 5. Minimum Supply Voltage vs. Temperature

Applications Discussion

Simple Step-Up Converter

The most common application, the step-up regulator, is derived from a simple step-up ($V_{OUT} > V_{BAT}$) DC-to-EC Converter (Figure 6).

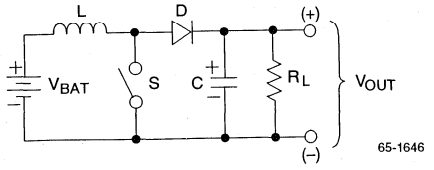


Figure 6. Simple Set-Up Converter

When switch S is closed, the battery voltage is applied across the inductor L. Charging current flows through the inductor, building up a magnetic field, increasing as the switch is held closed. While the switch is closed, the diode D is reverse biased (open circuit) and current is supplied to the load by the capacitor C. Until the switch is opened, the inductor current will increase linearly to a maximum value determined by the battery voltage, inductor value, and the amount of time the switch is held closed ($I_{MAX} = V_{BAT}/L \times T_{ON}$). When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a discharge current which flows through the inductor in the same direction as the charging current. Because there is no path for current to flow through the switch, the current must flow through the switch, the current must flow through the diode to supply the load and charge the output capacitor.

If the switch is opened and closed repeatedly, at a rate much greater than the time constant of the output RC, then a constant DC voltage will be produced at the output.

An output voltage higher than the input voltage is possible because of the high voltage produced by a rapid change of current in the inductor. When the switch is opened, the inductor voltage will instantly rise high enough to forward bias the diode, to $V_{OUT} + V_D$.

In the complete RC4193 regulator, a feedback control system adjusts the on time of the switch, controlling the level of inductor current, so that the average inductor discharge current equals the load current, thus regulating the output voltage.

Complete Step-Up Regulator

A complete schematic of the minimum step-up application is shown in Figure 7. The ideal switch in the DC-to-DC Converter diagram is replaced by an open collector NPN transistor Q1. C_F functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the current in R1 supplies bias current to pin 6 (I_C). This current is stabilized by a unity gain current source amplifier and then used as bias current for the 1.31V bandgap reference. A very stable bias current generated by the bandgap is mirrored and used to bias the remainder of the chip. At the same time the RC4193 is starting up, current will flow through the inductor and the diode to charge the output capacitor to $V_{BAT} - V_D$.

At this point, the feedback (pin 7) senses that the output voltage is too low, by comparing a division of the output voltage (set by the ratio of R2 to R3) to the +1.31V reference. If the output voltage is too low then the comparator output changes to a logical zero. The NOR gate then effectively ANDs the oscillator square wave with the comparator signal; if the comparator output is zero AND the oscillator output is low, then the NOR gate output is high and the switch transistor will be forced on. When the oscillator goes high again, the NOR gate output goes low and the switch transistor will turn off. This turning on and off of the switch transistor performs the same function that opening and closing the switch in the simple DC-to-DC Converter does; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

The comparator will continue to allow the oscillator to turn the switch on and off until enough charge has been delivered to the capacitor to raise the feedback voltage above 1.31V.

Thereafter, this feedback system will vary the duration of the on time in response to changes in load current or battery voltage (see Figure 8). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle (waveform B), thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and time.

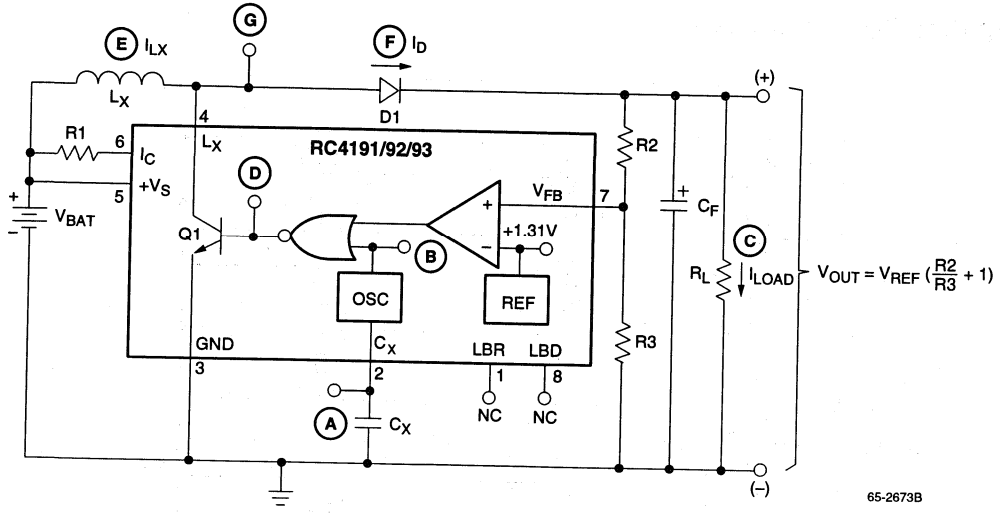


Figure 7. Complete Step-Up Regulator

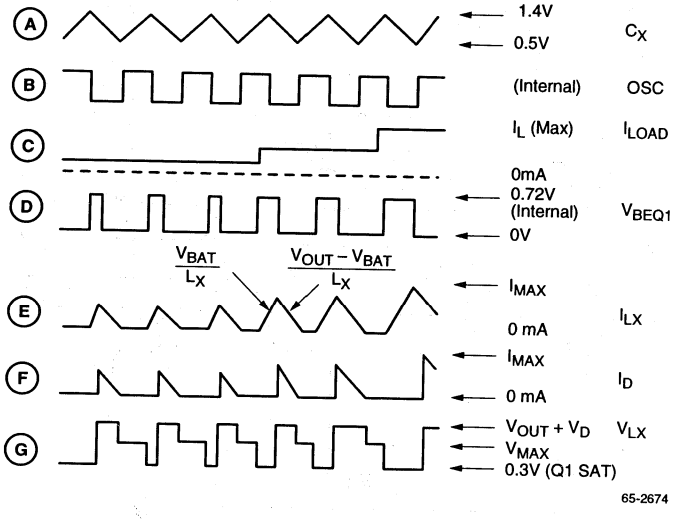
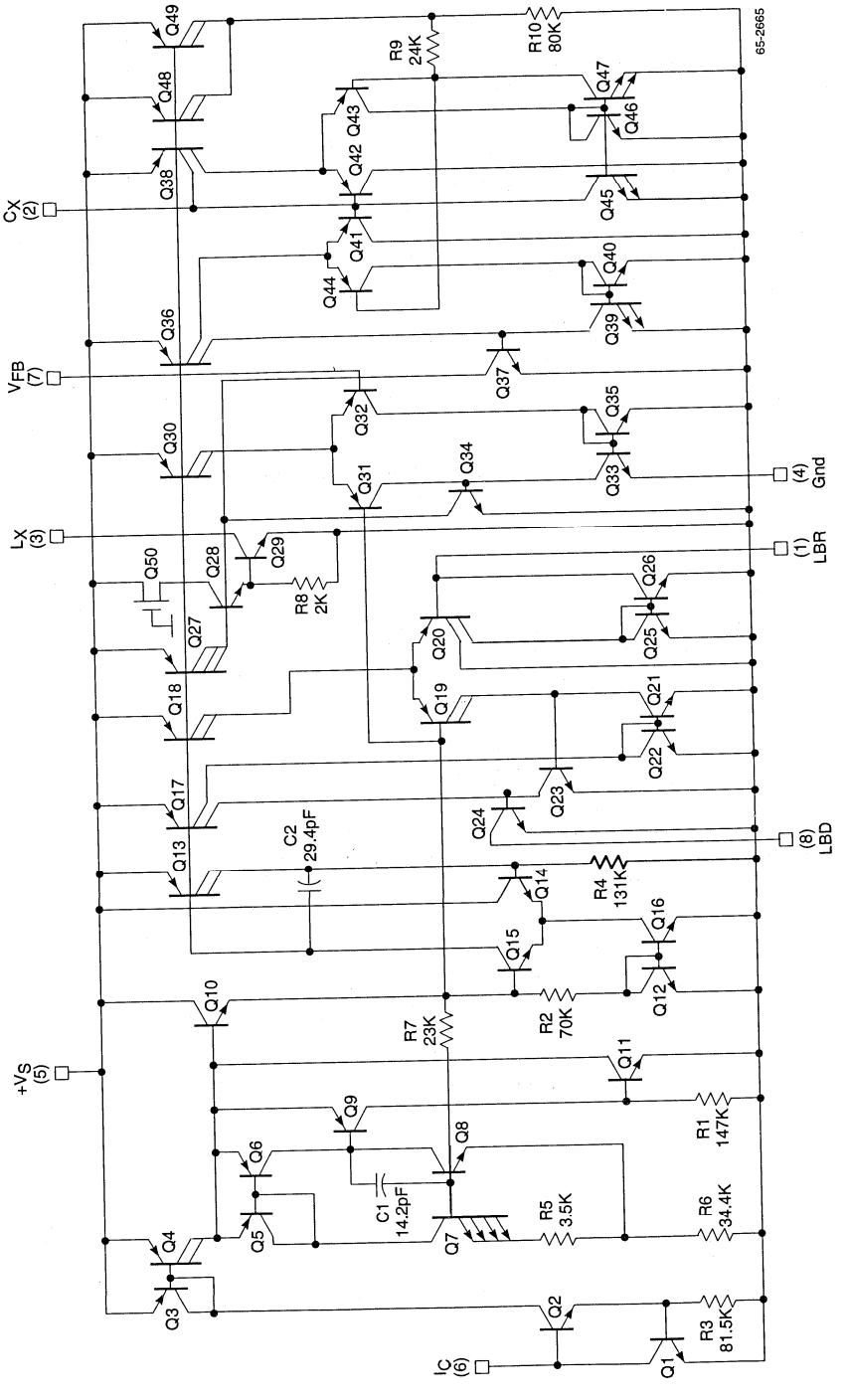


Figure 8. Step-Up Regulator Waveforms

Simplified Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package
RC4191M/2M/3M	0° to +70°C	Commercial	8 Pin Wide SOIC
RC4191N/2N/3N	0° to +70°C	Commercial	8 Pin Plastic DIP
RV4191N/92N/93N	-25° to +85°C		8 Pin Plastic DIP
RM4191D/92D/93D	-55°C to +125°C		8 Pin Ceramic DIP
RM4191D/883	-55°C to +125°C	Military	8 Pin Ceramic DIP

Note:

1. /883 suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

THIS PAGE INTENTIONALLY LEFT BLANK

RC4194

Dual Tracking Voltage Regulators

Features

- Simultaneously adjustable outputs with one resistor to ±42V
- Load current – ±200 mA with 0.04% load regulation
- Internal thermal shutdown at T_J = +175°C
- External balance for ±V_{OUT} unbalancing
- 3W power dissipations

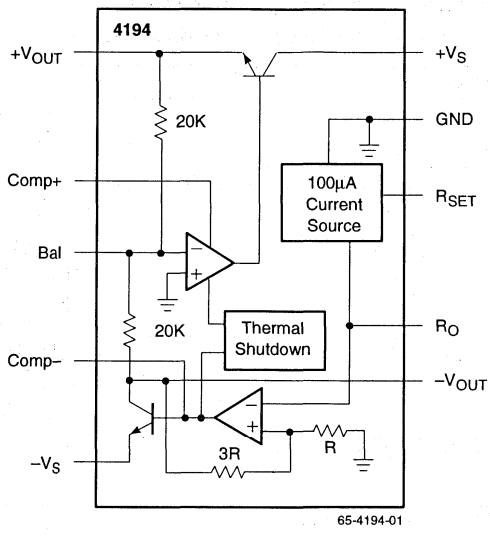
Description

The RC/RM4194 are dual polarity tracking regulators designed to provide balanced or unbalanced positive and negative output voltages at currents to 200 mA.
A single external resistor adjustment can be used to change both outputs between the limits of ±50 mV and ±42V.

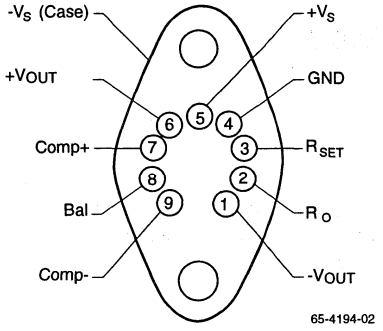
These devices are designed for local "on-card" regulation, eliminating distribution problems associated with single-point regulation. To simplify application the regulators require a minimum number of external parts.

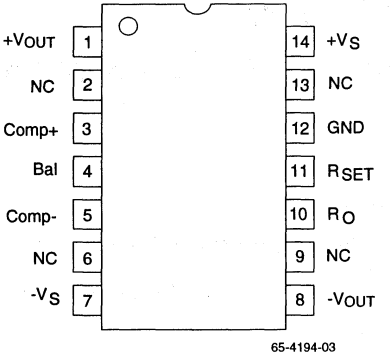
The device is available in three package types to accommodate various power requirements. The K (TO-66) power package can dissipate up to 3W at T_A = +25°C. The D 14-pin dual in-line will dissipate up to 1W and the N 14-pin dual in-line will dissipate up to 625 mW.

Block Diagram



Pin Assignments





Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage	RC4194			±35	V
	RM4194			±45	V
Supply Input to Output Voltage Differential	RC4194			±35	V
	RM4194			±45	V
Load Current	PDIP			100	mA
	CerDIP			150	mA
	TO-66 Metal Can			250	mA
$P_D T_A < 50°C$	PDIP			468	mW
	CerDIP			1042	mW
	TO-66 Metal Can			2381	mW
Operating Temperature (T_j)	RC4194	0		70	°C
	RM4194	-55		125	°C
Storage Temperature		-65		150	°C
Junction Temperature	PDIP			125	°C
	CerDIP			175	°C
	TO-66 Metal Can			150	°C
Lead Soldering Temperature (60 seconds)				300	°C
For $T_A > 50°C$ Derate at	TO-66 Metal Can		23.81		mW/°C
	PDIP		6.25		mW/°C
	CerDIP		8.38		mW/°C

Note:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter			Min	Typ	Max	Units
θJC	Thermal Resistance	CerDIP		60		°C/W
		TO-66 Metal Can		7		°C/W
θJA	Thermal Resistance	PDIP		160		°C/W
		CerDIP		120		°C/W
		TO-66 Metal Can		42		°C/W

Electrical Characteristics

($\pm 5 \le V_{OUT} \le V_{MAX}$; $-V_{IN} \le -8V$; $I_L = \pm 1mA$; RM4194: $-55°C \le T_j \le +125°C$; RC4194: $0°C \le T_j \le +70°C$ unless otherwise specified)

Parameters	Test Conditions	Min	Typ	Max	Units
Line Regulation	$\Delta V_S = 0.1\ V_{IN}$		0.04	0.1	$\%V_{OUT}$
Load Regulation[1]	4194K: $I_L < 200$ mA 4194D: $I_L < 100$ mA $\pm V_S = \pm (V_{OUT} + 5)V$		0.002	0.004	$\%V_{OUT}/I_L$ (mA)
Output Voltage Drift With Temperature[2]					
Positive Output	$V_{OUT} = \pm 5V$		0.002	0.015	%/°C
Negative Output	$V_{OUT} = \pm 5V$		0.003	0.015	%/°C
Supply Current[3] (Positive)	$V_S = \pm V_{MAX}$, $V_{OUT} = 0V$, $I_L = 0$ mA		+0.8	+2.5	mA
Supply Current[4] (Negative)	$V_S = \pm V_{MAX}$, $V_{OUT} = 0V$, $I_L = 0$ mA		-1.8	-4.0	mA
Supply Voltage	RM4194	±9.5		±45	V
	RC4194	±9.5		±35	V
Output Voltage Scale Factor	$R_{SET} = 71.5\ k\Omega$, $T_j = +25°C$, $V_S = \pm V_{MAX}$	2.38	2.5	2.62	kΩ/V
Output Voltage Range	RM4194: $R_{SET} = 71.5\ k\Omega$, $I_L = 25$ mA	0.05		±42	V
	RC4194: $R_{SET} = 71.5\ k\Omega$, $I_L = 25$ mA	0.05		±42	V
Output Voltage Tracking			±0.4	±2.0	%
Ripple Rejection	F = 120 Hz, $T_j = +25°C$		70		dB
Input-Output Voltage Differential	$I_L = 50$ mA, $T_j = +25°C$	3.0			V
Short Circuit Current	$V_S = \pm 30V$, $T_j = +25°C$		300		mA
Output Noise Voltage	$C_L = 4.7\ \mu F$, $V_{OUT} = \pm 15V$, F = 10 Hz to 100 kHz		250		μV_{RMS}
Internal Thermal Shutdown			175		°C

Notes:

1. Measured as $\left(\frac{\Delta V_{OUT}}{V_{OUT}} \times 100\%\right) \S\ I_L$ (mA)
2. Output voltage temperature drift guaranteed by design.
3. The current drain will increase by $50\mu A/V_{OUT}$ on positive side and $100\mu A/V_{OUT}$ on negative side.
4. The specifications above apply for the given junction temperatures since pulse test conditions are used.

Typical Performance Characteristics

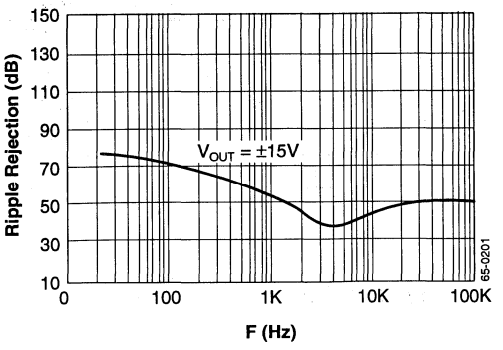


Figure 1. Ripple Rejection vs. Frequency

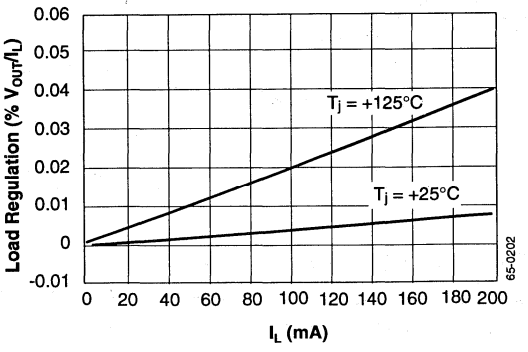
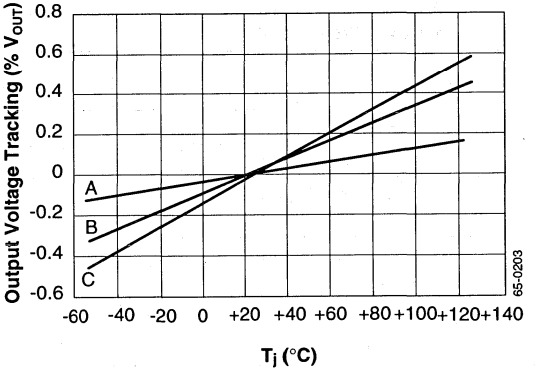


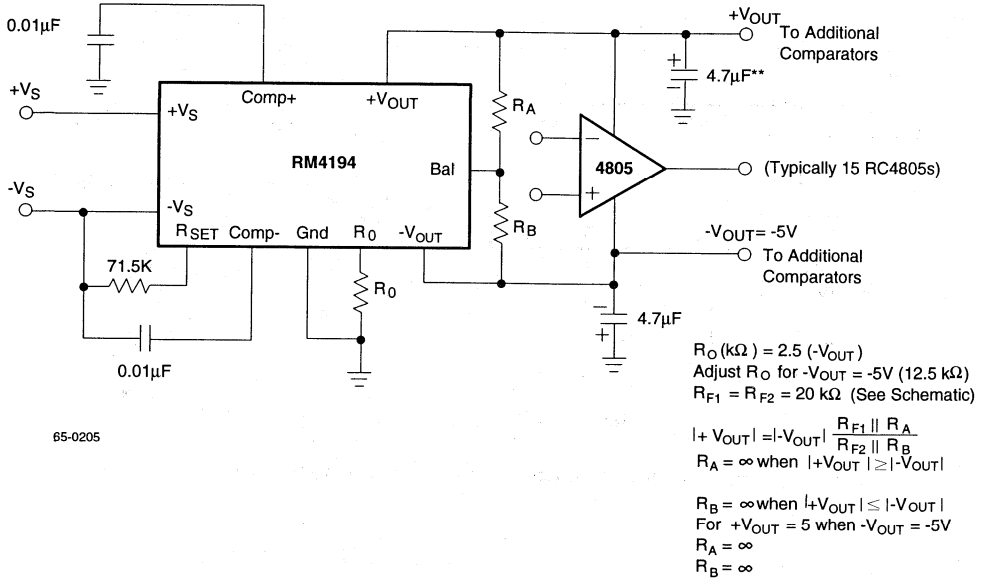
Figure 2. Load Regulation vs. Load Current



A = % Tracking of V_{OUT}
B = T.C. for Positive Regulator
C = T.C. for Negative Regulator

Figure 3. Output Voltage Tracking vs. Temperature

Typical Applications



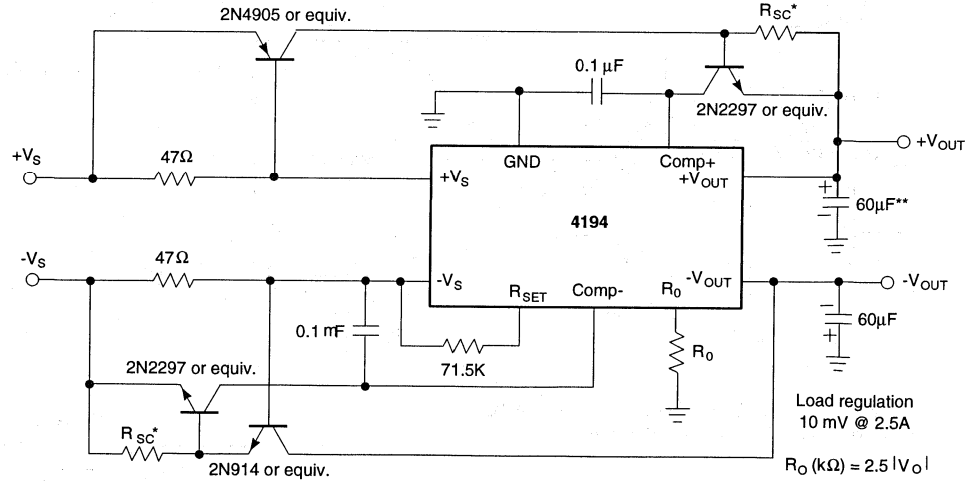
$R_O (k\Omega) = 2.5 (-V_{OUT})$
Adjust R_O for $-V_{OUT} = -5V$ (12.5 kΩ)
$R_{F1} = R_{F2} = 20\ k\Omega$ (See Schematic)

$$|+V_{OUT}| = |-V_{OUT}| \frac{R_{F1} \parallel R_A}{R_{F2} \parallel R_B}$$

$R_A = \infty$ when $|+V_{OUT}| \geq |-V_{OUT}|$

$R_B = \infty$ when $|+V_{OUT}| \leq |-V_{OUT}|$
For $+V_{OUT} = 5$ when $-V_{OUT} = -5V$
$R_A = \infty$
$R_B = \infty$

Figure 4. Unbalanced Output Voltage — Comparator Application



$$*R_{SC} = \frac{0.7}{I_{SC}}$$

**Optional usage - Not as critical as $-V_O$ bypass capacitors.

Note: Compensation and bypass capacitor connections should be close as posibe to the 4194

65-0206

Figure 5. High Output Application

Typical Applications (continued)

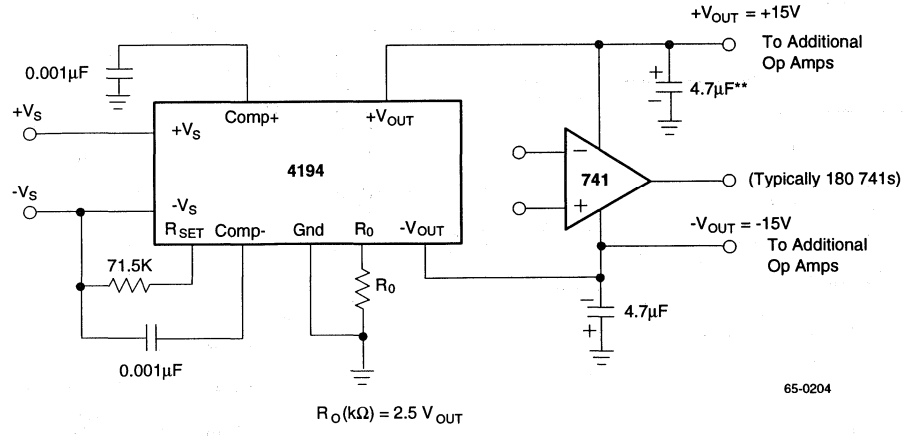


Figure 6. Balanced Output Voltage — Op Amp Application

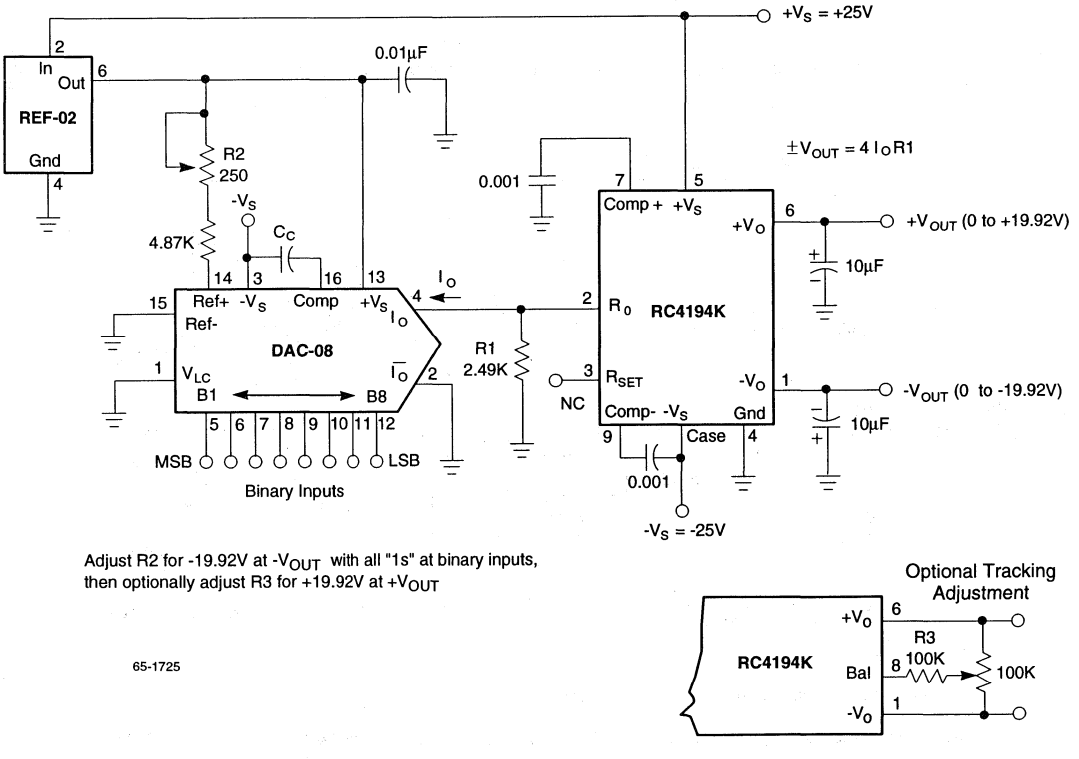


Figure 7. Digitally Controlled Dual 200 mA Voltage Regulator

RC4194 Switchable Power Supply

The outputs of the RC4194 can be simultaneously switched on or off under logic control as shown in Figure 8. In the "off" state, the outputs will be forced to a minimum voltage, or about ±20 mV, rather than becoming open-circuit. The turn-on time, with the outputs programmed to ±12V, is approximately 200 µS. This circuit works by forcing the R0 pin to ground with an analog switch.

Refer to the RC4194 internal schematic diagram. A reference voltage that regulates with respect to $-V_S$ is generated at the RSET pin by the zener diode Q12 and the buffer circuit of Q11 and Q13. When the external 71.5k RSET resistor is connected between the R_{SET} pin and $-V_S$, a precision current of 100 µA is generated which then flows into Q13's collector. Since Q13's collector is tied to the R0 pin, the 100 µA current will develop a ground-referenced voltage drop proportional to the value of R0, which is then amplified by the internal error amplifier. When the analog switch in Figure 8 turns on, it effectively shorts out R0 and causes 0V to be applied to the error amplifier. The output voltage in the off state will be approxi-mately ±20 mV. If a higher value (50 to 100 mV) is acceptable, then the DG201 analog switch can be replaced with a low-cost small signal transistor, as shown in the alternate switch configuration.

Compensation

For most applications, the following compensation technique is sufficient. The positive regulator section of the RC4194 is compensated by a 0.001 µF ceramic disc capacitor from the Comp+ terminal to ground. The negative regulator requires compensation at two points. The first is the Comp– pin, which should have 0.001 µF to the $-V_S$ pin, or case. A ceramic disc is ideal here. The second compen-sation point for the negative side is the $-V_{OUT}$ terminal, which ideally should be a 4.7 µF solid tantalum capacitor with enough reserve voltage capacity to avoid the momentary shorting and reforming which can occur with tantalum caps. For systems where the cost of a solid tantalum capacitor cannot be justified, it is usually sufficient to use an aluminum capacitor with a 0.03 µF ceramic disc in parallel to bypass high frequencies. In addition, if the rectifier filter capacitors have poor high frequency characteristics (like aluminum electrolytics) or if any impedance is in series with the $+V_S$ and $-V_S$ terminals, it is necessary to bypass these two points with 0.01 µF ceramic disc capacitors. Just as with monolithic op amps, some applications may not require these bypass caps, but if in doubt, be sure to include them.

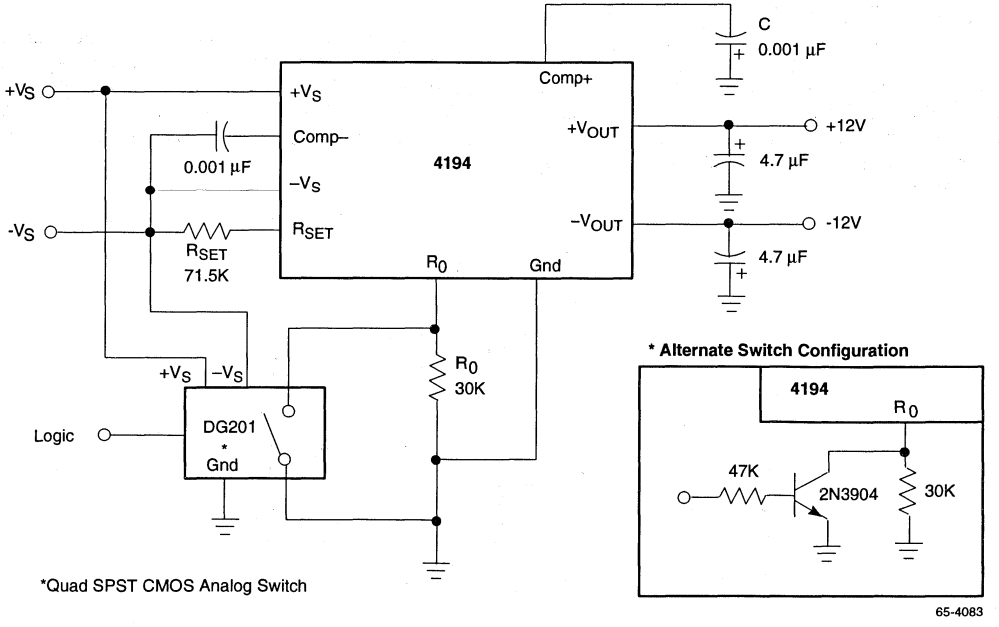


Figure 8. ±12V Switchable Power Supply

All compensation and bypass caps should have short leads, solid grounds, and be located as close to the 4194 as possible. Refer to Figure 9 for recommended compensation circuitry.

Protection

In systems using monolithic voltage regulators, a number of conditions can exist which, left uncorrected, will destroy the regulator. Fortunately, regulators can easily be protected against these potentially destructive conditions. Monolithic regulators can be destroyed by any reversal of input or output voltage polarity, or if the input voltage drops below the output voltage in magnitude. These conditions can be caused by inductive loads at the inputs or outputs of the regulator. Other problems are caused by heavy loads at the unregulated inputs to the regulator, which might cause the input voltage to drop below the output voltage at turn-off. If any of the preceding problem conditions are present in your system, it is recommended that you protect the regulator using diodes. These diodes should be high speed types capable of handling large current surges. Figure 10 shows all six of the possible protection diodes. The diodes at the inputs and outputs prevent voltages at those points from becoming reversed. Diodes from outputs to inputs prevent the output voltage from exceeding the input voltage. Chances are that the system under consideration will not require all six diodes, but if in doubt, be sure to include them.

Brownout Protection

The RC4194 is one of the most easily applied and trouble-free monolithic ICs available. When used within the data sheet ratings (package power dissipation, maximum output current, minimum and maximum input voltages) it provides the most cost-effective source of regulated ±15V for powering linear ICs.

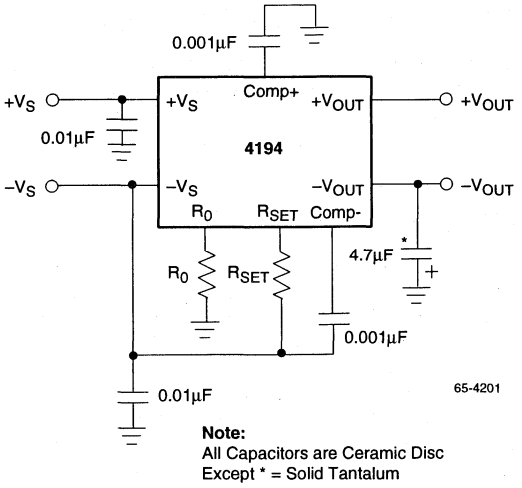


Figure 9. RC4194 Recommended Compensation

Sometimes occasions arise in which the RC4194 ratings must be exceeded. One example is the "brownout." During a brownout, line voltages may be reduced to as low as 75 VRMS, causing the input voltage to the RC4194 to drop below the minimum dropout voltage. When this happens, the negative output voltage can go to positive. The maximum amount of current available is approximately 5 mA.

In general this is not enough current to damage most ICs which the RC4194 might be supplying, but it is a potentially destructive condition. Fortunately, it is easy to protect against. As shown in the typical application circuit in Figure 11, a diode, D, can be connected to the negative output.

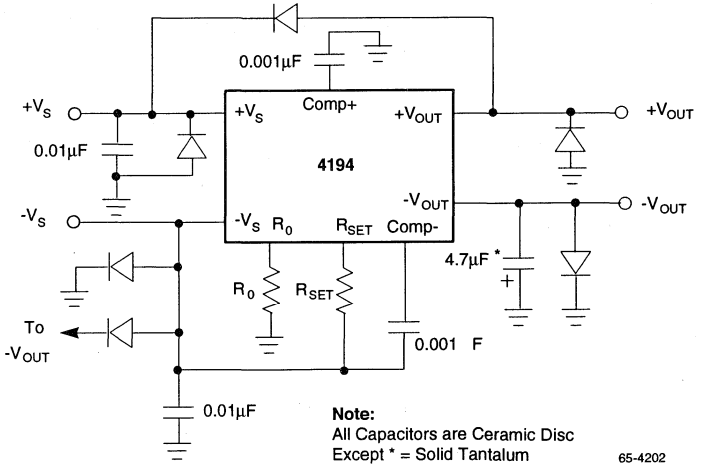


Figure 10. RC4194 Regulator Showing All Protective Diodes

If a small signal silicon diode is used, it will clamp the negative output voltage at about +0.55V. A Schottky barrier or germanium device would clamp the voltage at about +0.3V. Another cure which will keep the negative output negative at all times is the 1 mΩ resistor connected between the +15V output and the Comp- terminal. This resistor will then supply drive to the negative output transistor, causing it to saturate to -1V during the brownout.

Heatsinking

Voltage Regulators are power devices which are used in a wide range of applications.

When operating these devices near their extremes of load current, ambient temperature and input-output differential, consideration of package dissipation becomes important to avoid thermal shutdown at 175°C. The RC4194 has this feature to prevent damage to the device. It typically starts affecting load regulation approximately 2°C below 175°C. To avoid shutdown, some form of heatsinking should be used or one of the above operating conditions would need to be derated.*

The following is the basic equation for junction temperature:

$$T_J = T_A + P_D\theta_{J-A}$$

Equation 1

where

T_J = junction temperature (°C)

T_A = ambient air temperature (°C)

P_D = power dissipated by device (W)

θ_{J-A} = thermal resistance from junction to ambient air (°C/W)

The power dissipated by the voltage regulator can be detailed as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Equation 2

where

V_{IN} = input voltage

V_{OUT} = regulated output voltage

I_O = load current

I_Q = quiescent current drain

Let's look at an application where a user is trying to determine whether the RC4194 in a high temperature environment will need a heatsink.

Given:

T_J at thermal shutdown = 150°C

T_A = 125°C

θ_{J-A} = 41.6°C/W, K (TO-66) pkg.

V_{IN} = 40V

V_{OUT} = 30V

I_Q = 1 mA + 75 µA/V_{OUT} x 30V
= 3.25 mA*

$$\theta_{J-A} = \frac{T_J - T_A}{P_D}$$

$$P_D = \frac{T_J - T_A}{\theta_{J-A}}$$

$$= (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Solve for I_O,

$$I_O = \frac{T_J - T_A}{\theta_{J-A}(V_{IN} - V_{OUT})} - \frac{V_{IN} \times I_Q}{(V_{IN} - V_{OUT})}$$

$$I_O = \frac{150°C - 125°C}{41.6°C/W \times 10V} - \frac{40 \times 3.25 \times 10^{-3}}{10}$$

= 60 mA – 13 mA ~ 47 mA

If this supply current does not provide at least a 10% margin under worst case load conditions, heatsinking should be employed. If reliability is of prime importance, the multiple regulator approach should be considered.

In Equation 1, θ_{J-A} can be broken into the following components:

$$\theta_{J-A} = \theta_{J-C} + \theta_{C-S} + \theta_{S-A}$$

where

θ_{J-C} = junction-to-case thermal resistance

θ_{C-S} = case-to-heatsink thermal resistance

θ_{S-A} = heatsink-to-ambient thermal resistance

*The current drain will increase by 50µA/V_{OUT} on positive side and 100µA/V_{OUT} on negative side

In the above example, let's say that the user's load current is 200 mA and he wants to calculate the combined θ_{C-S} and θ_{S-A} he needs:

Given: $I_O = 200$ mA,

$$\theta_{J-A} = \frac{T_J - T_A}{(V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q}$$

$$= \frac{50°C - 125°C}{10V \times 200mA + 40 \times 3.25 \times 10^{-3}}$$

$$= 11.75°C/W$$

Given $\theta_{J-C} = 7.15°C/W$ for the 4194 in the K package,

$$\theta_{C-S} + \theta_{S-A} = 11.75°C/W - 7.15°C/W$$

$$= 4.6°C/W$$

When using heatsink compound with a metal-to-metal interface, a typical $\theta_{C-S} = 0.5°C/W$ for the K package. The remaining θ_{S-A} of approximately 4°C/W is a large enough thermal resistance to be easily provided by a number of heatsinks currently available. Table 1 is a brief selection guide to heatsink manufacturers.

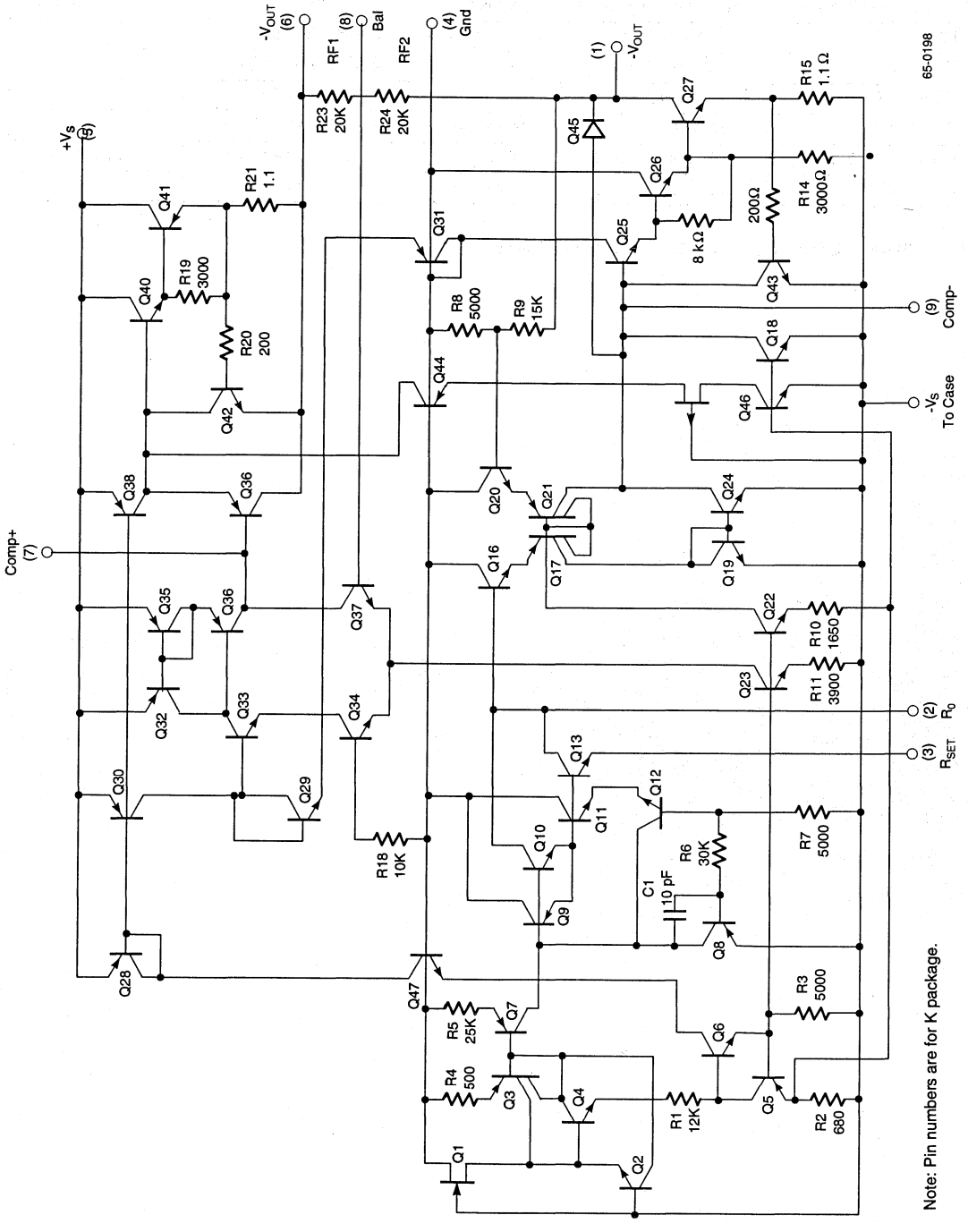
Table 1. Commercial Heatsink Selection Guide

No attempt has been made to provide a complete list of all heatsink manufacturers. This list is only representative.

θ_{S-A}[1] (°C/W)	Manufacturer/Series or Part Number
TO-66 Package	
0.31 – 1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0 – 3.0	Wakefield — 641
	Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0 – 5.0	Wakefield — 621, 623
	Thermalloy — 6606, 6129, 6141, 6303
	IERC — HP
	Staver — V3-3-2
5.0 – 7.0	Wakefield — 690
	Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301
	IERC — LB
	Staver— V3-5-2
7.0 – 10.0	Wakefield — 672
	Thermalloy — 6001, 6016, 6051, 6105, 6601
	IERC — LA, uP
	Staver — V1-3, V1-5, V3-3, V3-5, V3-7
10.0 – 25.0	Thermalloy — 6-13, 6014, 6015, 6103, 6104, 6105, 6117
Dual In-line Package	
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LI
60	Wakefield — 650, 651

Staver Co., Inc.: 41-51 N Saxon Ave., Bay Shore, NY 11706
IERC: 135 W Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W Valley View Ln., Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880
* All values are typical as given by manufacturer or as determined from characteristic curves supplied by manufacturer.

Simplified Schematic Diagram



Note: Pin numbers are for K package.

Ordering Information

Product Number	Temperature Range	Screening	Package	SMD Number
RC4194N	0° to +70°C	Commercial	14 pin Plastic DIP	
RC4194D	0° to +70°C	Commercial	14 pin Ceramic DIP	
RC4194K	0° to +70°C	Commercial	9 pin TO-66	
RM4194D	-55°C to +125°C	Commercial	14 pin Ceramic DIP	
RM4194D/883B	-55°C to +125°C	Military	14 pin Ceramic DIP	7705401CA
RM4194K	-55°C to +125°C	Commercial	9 pin TO-66	

Note:

1. /883B suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

RC4195

Fixed ±15V Dual Tracking Voltage Regulator

Features

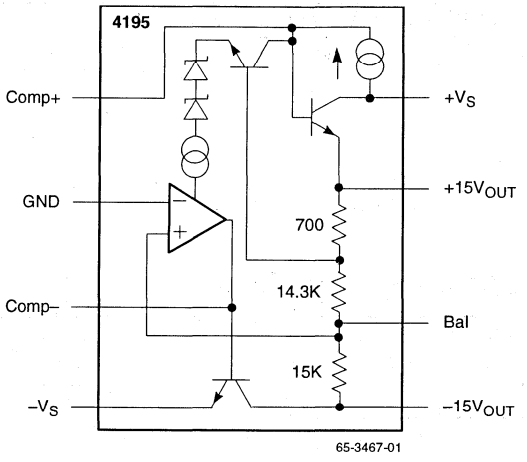
- ±15V operational amplifier power at reduced cost and component density
- Thermal shutdown at T_J = +175°C in addition to short circuit protection
- Output currents to 100 mA
- May be used as single output regulator with up to +50V output
- Available in TO-66, TO-99 and 8-lead mini-DIP

Description

The RM/RC4195 is a dual polarity tracking regulator designed to provide balanced positive and negative 15V output voltages at currents up to 100mA. This device is designed for local "on-card" regulation, eliminating distribution problems associated with single point regulation. The regulator is intended for ease of application. Only two external components are required for operation (two 10 µF bypass capacitors).

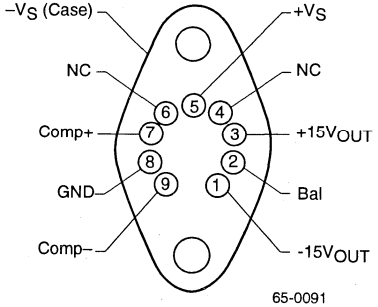
The device is available in four package types to accommodate various applications requiring economy, high power, dissipation, and reduced component density.

Block Diagram

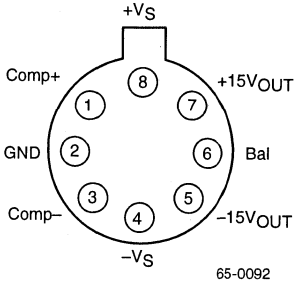


65-3467-01

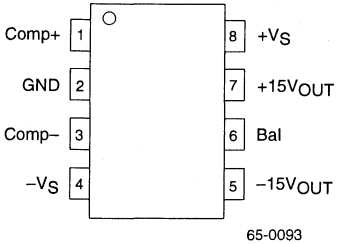
Pin Assignments



65-0091



65-0092



65-0093

Rev. 1.0.0

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage (±V_S) to Ground				±30	V
Load Current	PDIP/TO-99			150	mA
	TO-66			100	mA
$P_D T_A$ < 50°C	PDIP			468	mW
	TO-99			658	mW
	TO-66			2381	mW
Junction Temperature	PDIP			125	°C
	TO-99			175	°C
	TO-66			150	°C
Storage Temperature		-65		150	°C
Operating Temperature (T_j)	RC4195	0		70	°C
	RM4195	-55		125	°C
Lead Soldering Temperature (60 sec)				300	°C
For T_A > 50°C Derate at	PDIP		6.25		mW/°C
	TO-99		5.26		mW/°C
	TO-66		23.81		mW/°C

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	TO-99		50		°C/W
		TO-66		7		°C/W
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		TO-99		190		°C/W
		TO-66		42		°C/W

Electrical Characteristics

(I_L = ±1mA; V_S = ± 20V, C_L = 10µF; RM4195: -55°C ≤ T_j ≤ +125°C; RC4195: 0°C ≤ T_j ≤ +70°C unless otherwise specified)[1]

Parameters	Test Conditions	Min	Typ	Max	Units
Line Regulation	V_S = ±18V to ±30V		2	20	mV
Load Regulation	I_L = 1mA to 100mA		5	30	mV
Output Voltage Drift With Temperature			0.005	0.015	%/°C
Supply Current	V_S = ±30V, I_L = 0 mA		±1.5	±4.0	mA
Supply Voltage		±18		±30	V
Output Voltage	T_j = +25°C	14.5	15.0	15.5	V
Output Voltage Tracking			±50	±300	mV
Ripple Rejection	F = 120 Hz, T_A = +25°C		75		dB
Input-Output Voltage Differential	I_L = 50 mA	3.0			V
Short Circuit Current	T_j = +25°C		220		mA
Output Noise Voltage	T_j = +25°C, F = 100Hz to 120 kHz		60		μV_{RMS}
Internal Thermal Shutdown			175		°C

Note:

1. The specifications above apply for the given junction temperatures since pulse test conditions are used.

Typical Performance Characteristics

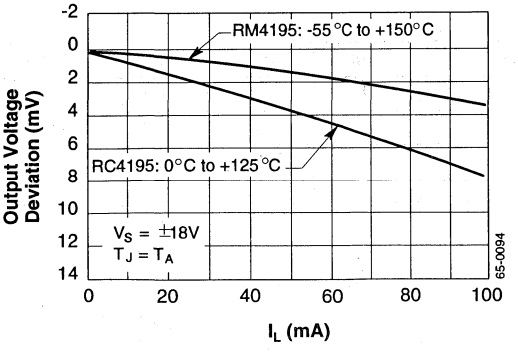


Figure 1. Output Load Regulation

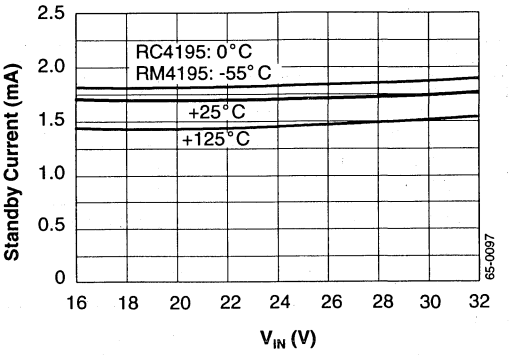


Figure 2. Standby Current Drain

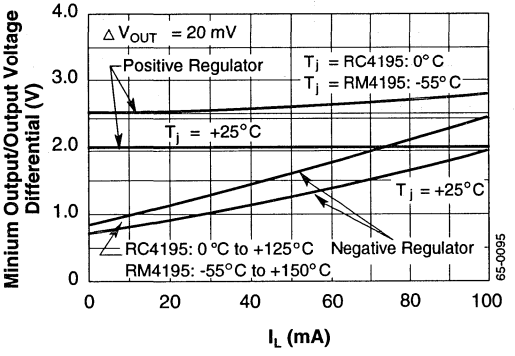


Figure 3. Regulator Dropout Voltage

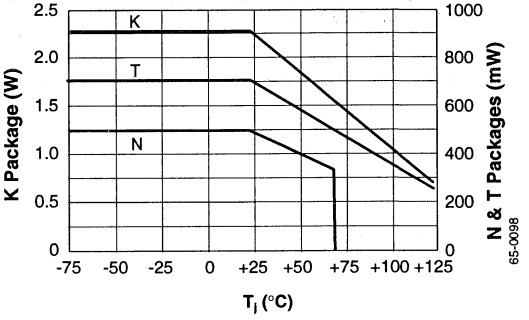


Figure 4. Power Dissipation

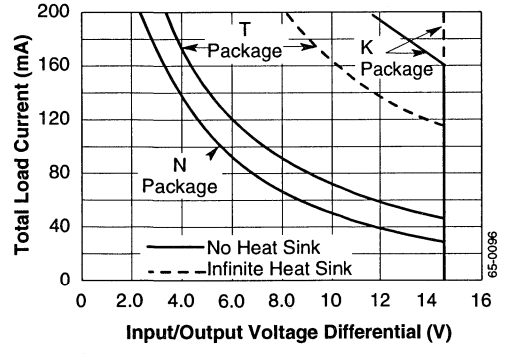


Figure 5. Maximum Current Capability

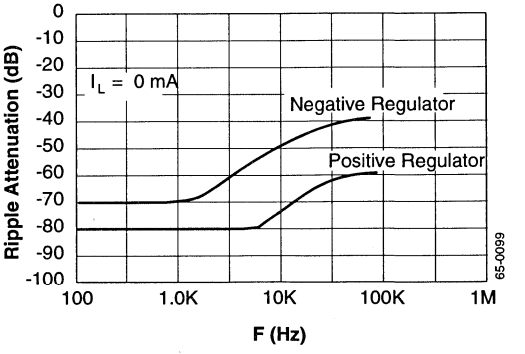


Figure 6. Ripple Rejection

Typical Applications

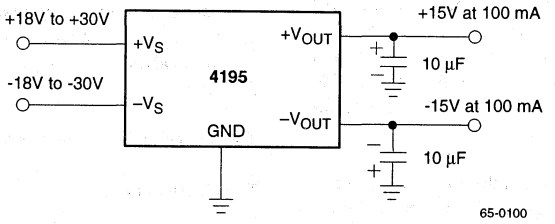


Figure 7. Balanced Output (V_{OUT} = ±15V)

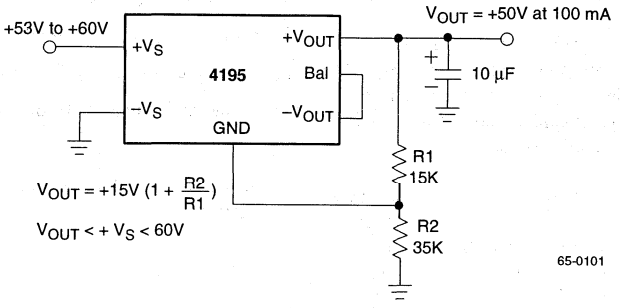


Figure 8. Positive Single Supply (+15V < V_{OUT} < +50V)

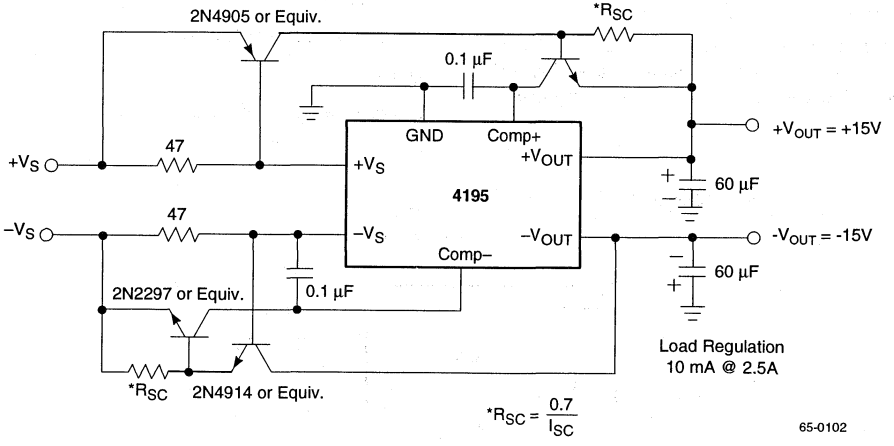


Figure 9. High Output Current

Brownout Protection

The RC4195 is one of the most easily applied and trouble-free monolithic ICs available. When used within the data sheet ratings (package power dissipation, maximum output current, minimum and maximum input voltages) it provides the most cost-effective source of regulated ±15V for powering linear ICs.

Sometimes occasions arise in which the RC4195 ratings must be exceeded. One example is the "brownout". During a brownout, line voltages may be reduced to as low as 75 V_{RMS}, causing the input voltage to the RC4195 to drop below the minimum dropout voltage. When this happens, the negative output voltage can go to positive. The maximum amount of current available is approximately 5 mA.

In general this is not enough current to damage most ICs which the RC4195 might be supplying, but it is a potentially destructive condition. Fortunately, it is easy to protect against. As shown in the typical application circuit, a diode, D, can be connected to the negative output.

If a small signal silicon diode is used, it will clamp the negative output voltage at about +0.55V. A Schottky barrier or germanium device would clamp the voltage at about +0.3V. Another cure which will keep the negative output negative all times is the 1 mΩ resistor connected between the +15V output and the Comp– terminal. this resistor will then supply drive to the negative output transistor, causing it to saturate to -1V during the brownout.

Heatsinking

When operating these devices near their extremes of load current, ambient temperature and input-output differential, consideration of package dissipation becomes important to avoid thermal shutdown at 175°C. The RC4195 has this feature to prevent damage to the device. It typically starts affecting load regulation approximately 2°C below 175°C. To avoid shutdown, some form of heatsinking should be used or one of the above operating conditions would need to be derated.*

The following is the basic equation for junction temperature:

$$T_J = T_A + P_D\theta_{J-A}$$

Equation 1

where

T_J = junction temperature (°C)

T_A = ambient air temperature (°C)

P_D = power dissipated by device (W)

θ_{J-A} = thermal resistance from junction to ambient air (°C/W)

The power dissipated by the voltage regulator can be detailed as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Equation 2

where

V_{IN} = input voltage

V_{OUT} = regulated output voltage

I_O = load current

I_Q = quiescent current drain

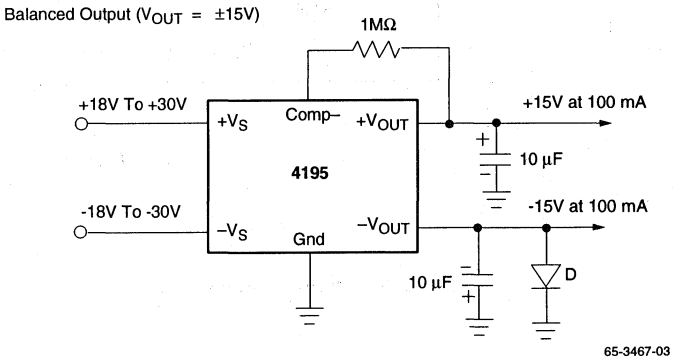


Figure 10. Typical Application Circuit

*In allowing for process deviations, the user should work with a maximum allowable function temperature of 150°C.
**The current drain will increase by 50µA/V_{OUT} on positive side and 100µA/V_{OUT} on negative side

Let's look at an application where a user is trying to determine whether the RC4195 in a high temperature environment will need a heatsink.

Given:

T_J at thermal shutdown = 150°C

T_A = 125°C

θ_{J-A} = 41.6°C/W, K (TO-66) pkg.

V_{IN} = 40V

V_{OUT} = 30V

I_Q = 1 mA + 75 µA/V_{OUT} x 30V
= 3.25 mA**

$$\theta_{J-A} = \frac{T_J - T_A}{P_D}$$

$$P_D = \frac{T_J - T_A}{\theta_{J-A}}$$

$$= (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Solve for I_O,

$$I_O = \frac{T_J - T_A}{\theta_{J-A}(V_{IN} - V_{OUT})} - \frac{V_{IN} \times I_Q}{(V_{IN} - V_{OUT})}$$

$$I_O = \frac{150°C - 125°C}{41.6°C/W \times 10V} - \frac{40 \times 3.25 \times 10^{-3}}{10}$$

= 60 mA – 13 mA ~ 47 mA

If this supply current does not provide at least a 10% margin under worst case load conditions, heatsinking should be employed. If reliability is of prime importance, the multiple regulator approach should be considered.

In Equation 1, θ_{J-A} can be broken into the following components:

$$\theta_{J-A} = \theta_{J-C} + \theta_{C-S} + \theta_{S-A}$$

where

θ_{J-C} = junction-to-case thermal resistance

θ_{C-S} = case-to-heatsink thermal resistance

θ_{S-A} = heatsink-to-ambient thermal resistance

In the above example, let's say that the user's load current is 200 mA and he wants to calculate the combined θ_{C-S} and θ_{S-A} he needs:

Given: I_O = 200 mA,

$$\theta_{J-A} = \frac{T_J - T_A}{(V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q}$$

$$= \frac{50°C - 125°C}{10V \times 200mA + 40 \times 3.25 \times 10^{-3}}$$

= 11.75°C/W

Given θ_{J-C} = 7.15°C/W for the 4194 in the K package,

$\theta_{C-S} + \theta_{S-A}$ = 11.75°C/W – 7.15°C/W

= 4.6°C/W

When using heatsink compound with a metal-to-metal interface, a typical θ_{C-S} = 0.5°C/W for the K package. The remaining θ_{S-A} of approximately 4°C/W is a large enough thermal resistance to be easily provided by a number of heatsinks currently available. Table 1 is a brief selection guide to heatsink manufacturers.

Table 1. Commercial Heatsink Selection Guide

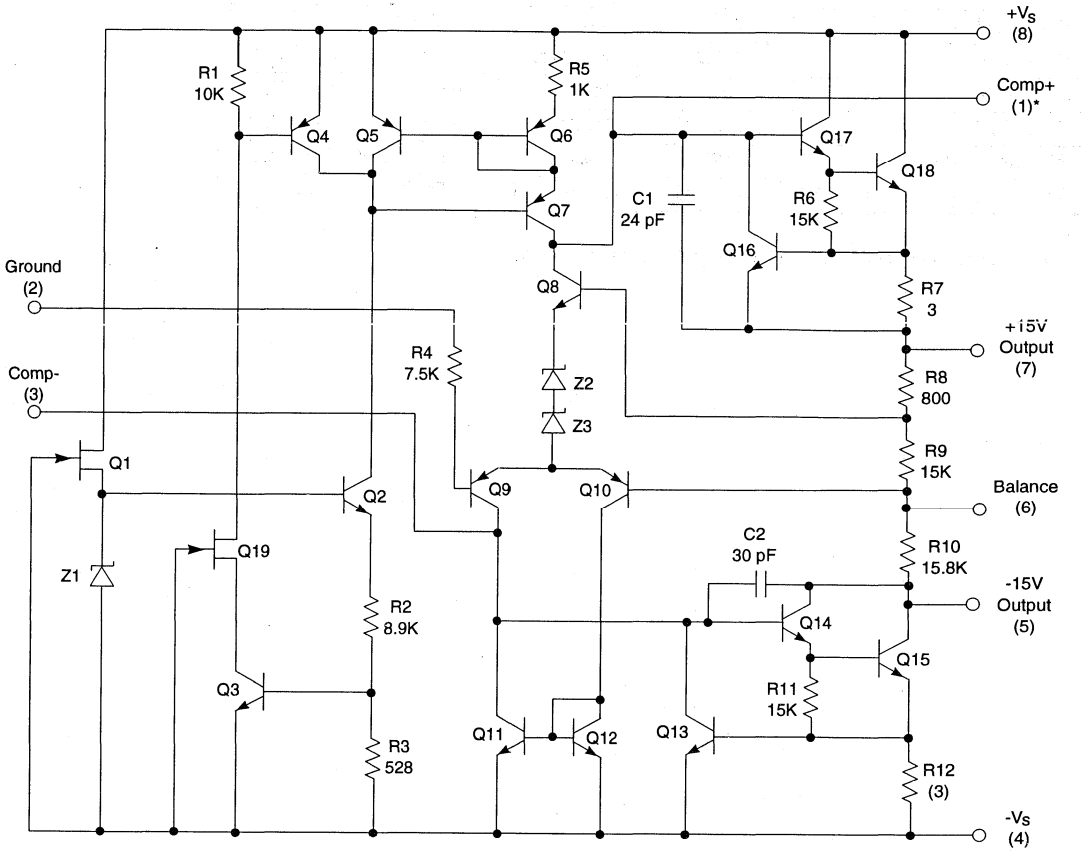
No attempt has been made to provide a complete list of all heatsink manufacturers. This list is only representative.

θ_{S-A}* (°C/W)	Manufacturer/Series or Part Number
TO-66 Package	
0.31 – 1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0 – 3.0	Wakefield — 641
	Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0 – 5.0	Wakefield — 621, 623
	Thermalloy — 6606, 6129, 6141, 6303
	IERC — HP
	Staver — V3-3-2
5.0 – 7.0	Wakefield — 690
	Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301
	IERC — LB
	Staver— V3-5-2
7.0 – 10.0	Wakefield — 672
	Thermalloy — 6001, 6016, 6051, 6105, 6601
	IERC — LA, uP
	Staver — V1-3, V1-5, V3-3, V3-5, V3-7
10.0 – 25.0	Thermalloy — 6-13, 6014, 6015, 6103, 6104, 6105, 6117
TO-99 Package	
12.0 – 20.0	Wakefield — 260
	Thermalloy — 1101, 1103
	Staver — V3A-5
20.0 – 30.0	Wakefield — 209
	Thermalloy — 1116, 1121, 1123, 1130, 1131, 1132, 2227, 3005
	IERC — LP
	Staver — F5-5
3.0 – 50.0	Wakefield — 207
	Thermalloy — 2212, 2215, 225, 2228, 2259, 2263, 2264
Dual In-line Package	
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LI
60	Wakefield — 650, 651

Staver Co., Inc.: 41-51 N Saxon Ave., Bay Shore, NY 11706
IERC: 135 W Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W Valley View Ln., Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880

* All values are typical as given by manufacturer or as determined from characteristic curves supplied by manufacturer.

Simplified Schematic Diagram



*Pin numbers are for 8-pin packages.

65-0090

Ordering Information

Product Number	Temperature Range	Screening	Package
RC4195N	0° to +70°C	Commercial	8 Pin Plastic DIP
RC4195T	0° to +70°C	Commercial	8 Pin TO-99 Metal Can
RC4195K	0° to +70°C	Commercial	9 Pin TO-66 Metal Can
RM4195T	-55°C to +125°C	Commercial	8 Pin TO-99 Metal Can
RM4195T/883B	-55°C to +125°C	Military	8 Pin TO-99 Metal Can
RM4195K	-55°C to +125°C	Commercial	9 Pin TO-66 Metal Can

Note:

1. /883B suffix denotes MIL-STD-883, Par. 1.2.1 compliant device.

RC4391

Inverting and Step-Down Switching Regulator

Features

- Versatile —
  Inverting function (+ to -)
  Step-down function
  Adjustable output voltage
  Regulates supply changes
- Micropower —
  Low quiescent current — 170 µA
  Wide supply range — 4V to 30V
- High performance —
  High switch current — 375 mA
  High efficiency — 70% typically
- Low battery detection capability
- 8-lead mini-DIP or S.O. package

Description

Raytheon's RC4391 is a monolithic switch mode power supply controller for micropower circuits. The RC4391 integrates all the active functions needed for low power switching supplies, including oscillator, switch, reference and logic, into a small package. Also, the quiescent supply current drawn by the RC4391 is extremely low; this combination of low supply current, function, and small package make it adaptable to a variety of miniature power supply applications.

The RC4391 complements another Raytheon switching regulator IC, the RC4190. The RC4190 is dedicated to step-up ($V_{OUT} > V_{IN}$) applications, while the RC4391 was designed for inverting ($V_{OUT} = -V_{IN}$) and step-down ($V_{OUT} < V_{IN}$) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the RC4190 data sheet for information on step-up applications.

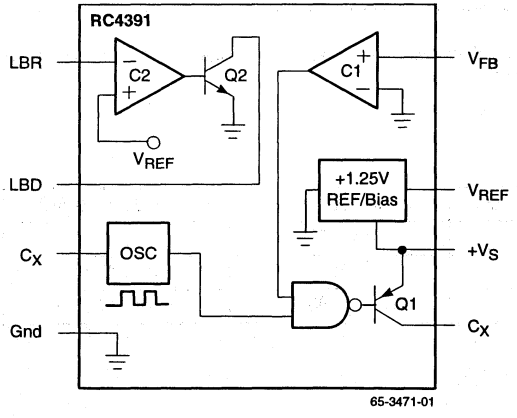
The functions provided are:

- Squarewave oscillator (adjustable externally)
- Bandgap voltage reference
- High current PNP switch transistor
- Feedback comparator
- Logic for gating the comparator
- Circuitry for detecting a discharged battery condition (in battery powered systems)

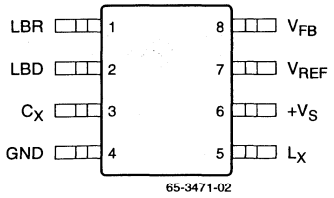
Few external components are required to build a complete DC-to-DC converter:

- Inductor
- Low value capacitor to set the oscillator frequency
- Electrolytic filter capacitor
- Steering diode
- Two resistors

Block Diagram



Pin Assignments



Pin Descriptions

Pin Number	Pin Function Description
1	Low Battery Resistor (LBR)
2	Low Battery Detector (LBD)
3	Timing Capacitor (C_X)
4	Ground
5	External Inductor (L_X)
6	+Supply Voltage ($+V_S$)
7	+1.25V Reference Voltage (V_{REF})
8	Feedback Voltage (V_{FB})

Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Unit
Internal Power Dissipation				500	mW
Supply Voltage[1]	(Pin 6 to Pin 4 or Pin 6 to Pin 5)			+30	V
Operating Temperature	RC4391	0		70	°C
	RV4391	-25		85	°C
	RM4391	-55		125	°C
Storage Temperature		-65		150	°C
Junction Temperature	PDIP, SOIC			125	°C
	CerDIP			175	°C
Switch Current (I_{MAX})	Peak			375	mA
P_D T_A <50°C	PDIP			468	mW
	CerDIP			833	mW
	SOIC			300	mW
Lead Soldering Temperature	(10 seconds)			300	°C

Note:

1. The maximum allowable supply voltage ($+V_S$) in inverting applications will be reduced by the value of the negative output voltage, unless an external power transistor is used in place of Q1.

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	Small Outline SO-8
Therm. Res θ_{JC}	—	45°C/W	—
Therm. Res. θ_{JA}	160°C/W	150°C/W	240°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	4.17 mW/°C

Electrical Characteristics

(V_S = +6.0V, over the full operating temperature range unless otherwise noted)

Symbol	Parameters	Condition	Min	Typ	Max	Units
$+V_S$	Supply Voltage	(Note 1)	4.0		30	V
I_{SY}	Supply Current	V_S = +25V		300	500	µA
V_{REF}	Reference Voltage		1.13	1.25	1.36	V
V_{OUT}	Output Voltage	V_{OUT} nom = -5.0V	-5.5	-5.0	-4.5	V
		V_{OUT} nom = -15V	-16.5	-15.0	-13.5	
LI_1	Line Regulation	V_{OUT} nom = -5.0V, C_X = 150pF V_S = +5.8V to +15V		2.0	4.0	%V_{OUT}
		V_{OUT} nom = -15V, C_X = 150pF V_S = +5.8V to +15		1.5	3.0	
LO_1	Load Regulation	V_{OUT} nom = -5.0V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.5	%V_{OUT}
		V_{OUT} nom = -15V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.3	
I_{CO}	Switch Leakage Current	Pin 5 = -20V		0.1	30	µA

Note:

1. The maximum allowable supply voltage ($+V_S$) in inverting applications will be reduced by the value of the negative output voltage, unless an external power transistor is used.

Electrical Characteristics

(V_S = +6.0V, T_A = +25°C unless otherwise noted)

Symbol	Parameters	Condition	Min	Typ	Max	Units
I_{SY}	Supply Voltage	V_S = +4.0V, No External Loads		170	250	µA
		V_S = +25V No External Loads		300	500	
V_{OUT}	Output Voltage	$V_{OUT\ nom}$ = -5.0V	-5.35	-5.0	-4.65	V
		$V_{OUT\ nom}$ = -15V	-15.85	-15.0	-14.15	
LI_1	Line Regulation	$V_{OUT\ nom}$ = -5.0V C_X = 150pF, V_S = +5.8V to +15V		1.5	3.0	%V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X = 150pF V_S = +5.8V to +15V		1.0	2.0	
LO_1	Load Regulation	$V_{OUT\ nom}$ = -5.0V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.4	%V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.07	0.14	
V_{REF}	Reference Voltage		1.18	1.25	1.32	V
I_{SW}	Switch Current	Pin 5 = 5.5V	75	100		mA
I_{CO}	Switch Leakage Current	Pin 5 = -24V		0.01	5.0	µA
I_{CX}	Cap. Charging Current	Pin 3 = 0V	6.0	10	14	µA
I_{LBDL}	LBD Leakage Current	Pin 1 = 1.5V, Pin 2 = 6.0V		0.01	5.0	µA
I_{LBD0}	LBD On Current	Pin 1 = 1.1V, Pin 2 = 0.4V	210	600		µA
I_{LBRB}	LBR Bias Current	Pin 1 = 1.5V		0.7		µA

Typical Performance Characteristics

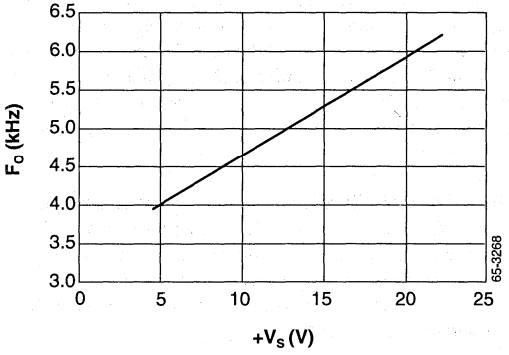


Figure 1. Oscillator Frequency vs. Supply Voltage

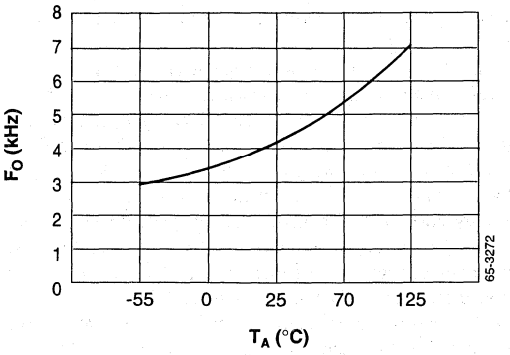


Figure 2. Oscillator Frequency vs. Temperature

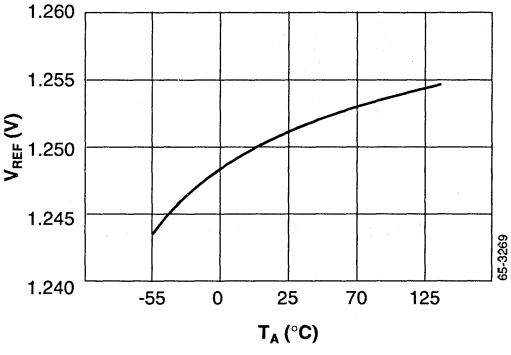


Figure 3. Reference Voltage vs. Temperature

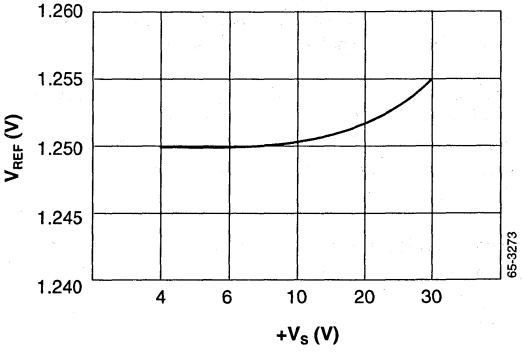


Figure 4. Reference Voltage vs. Supply Voltage

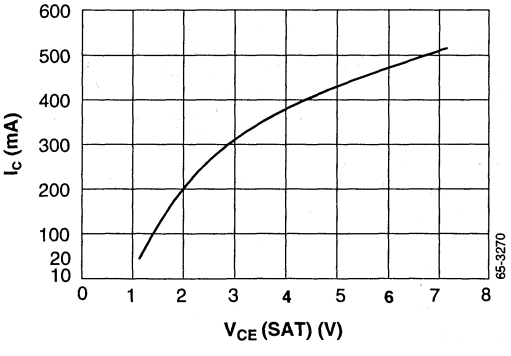


Figure 5. Collector Current vs. Q1 Saturation Voltage

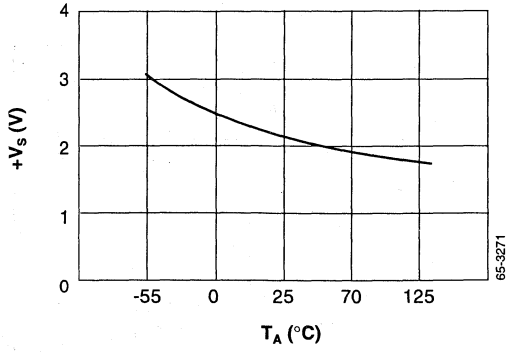


Figure 6. Minimum Supply Voltage vs. Temperature

Principles of Operation

The basic switching inverter circuit is the building block on which the complete inverting application is based.

A simplified diagram of the voltage inverter circuit with ideal components and no feedback circuitry is shown in Figure 7. When the switch S is closed, charging current from the battery flows through the inductor L, which builds up a magnetic field, increasing as the switch is held closed. When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a current which flows through the inductor in the same direction as the changing current. Because there is no path for this current to flow through the switch, the current must flow through the diode to charge the capacitor C. The key to the inversion is the ability of the inductor to become a source when the charging current is removed.

The equation V = L (di/dt) gives the maximum possible voltage across the inductor; in the actual application, feedback circuitry and the output capacitor will decrease the output voltage to a regulated fixed value.

A complete schematic for the standard inverting application is shown in Figure 8. The ideal switch in the simplified diagram is replaced by the PNP transistor switch between pins 5 and 6. C_F functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the ground sensing comparator (pin 8) compares the output voltage to the +1.25V voltage reference. Because C_F is initially discharged a positive voltage is applied to the comparator, and the output of the comparator gates the squarewave oscillator. This gated squarewave signal turns on, then off, the PNP output transistor. This turning on and off of the output transistor performs the same function as opening and closing the ideal switch in the simplified diagram; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

The comparator will continue to allow the oscillator to turn the switch transistor on and off until enough energy has been stored in the output capacitor to make the comparator input voltage decrease to less than 0V. The voltage applied to the comparator is set by the output voltage, the reference voltage, and the ratio of R1 to R2.

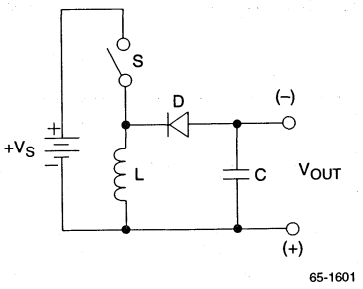
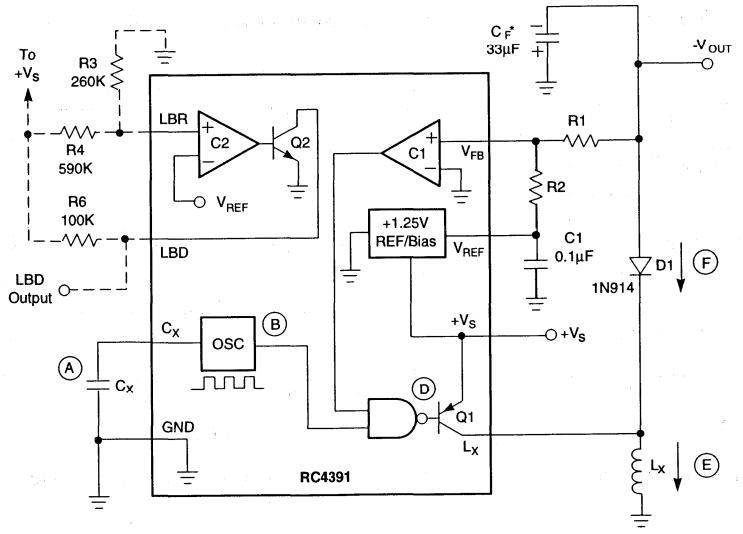


Figure 7. Simple Inverting Regulator



Parts List	-5.0V Output	-15V Output
R1 =	300 kΩ	900 kΩ
R2 =	75 kΩ	75 kΩ
C_X =	150 pF	150 pF
L_X =	1.0 mH Dale TE3 Q4 TA	

– – – – – – = Optional

$-V_{OUT} = (1.25V)\left(\frac{R1}{R2}\right)$

65-1602

*Caution: Use current limiting protection circuit for high values of C_F (Figure 13)

Figure 8. Inverting Regulator – Standard Circuit

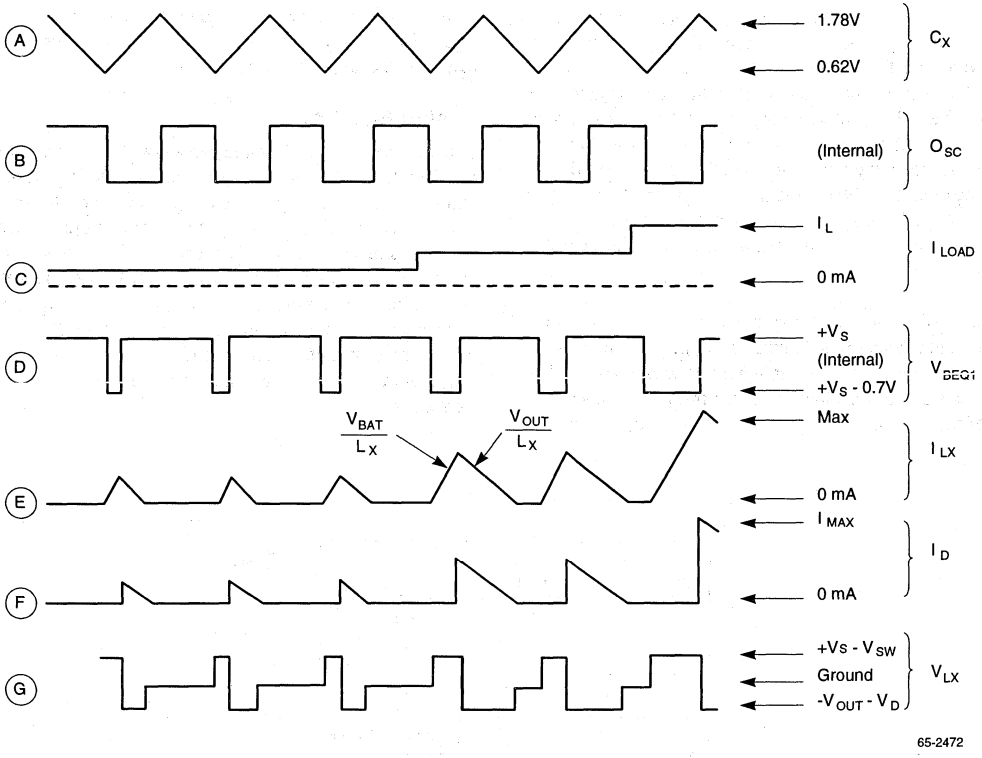


Figure 9. Inverting Regulator Waveforms

This feedback system will vary the duration of the on time in response to changes in load current or battery voltage (see Figure 9). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle, (waveform B) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and line.

Step-Down Regulator

The step-down circuit function is similar to inversion; it uses the same components (switch, inductor, diode, filter capacitor), and charges and discharges the inductor by closing and opening the switch. The great difference is that the inductor is in series with the load; therefore, both the charging current and the discharge current flow into the load. In the inverting circuit only the discharge current flows into the load. Refer to Figure 10.

When the switch S is closed, current flows from the battery, through the inductor, and through the load resistor to ground. After the switch is opened, stored energy in the inductor causes current to keep flowing through the load, the circuit being completed by the catch diode D. Since current flows to the load during charge and discharge, the average load current will be greater than in an inverting circuit. The significance of that is that for equal load currents the step-down circuit will require less peak inductor current than an inverting circuit. Therefore, the inductor will not require as large of a core, and the switch transistor will not be stressed as heavily for equal load currents.

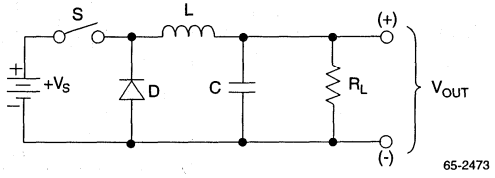


Figure 10. Simple Step-Down Regulator

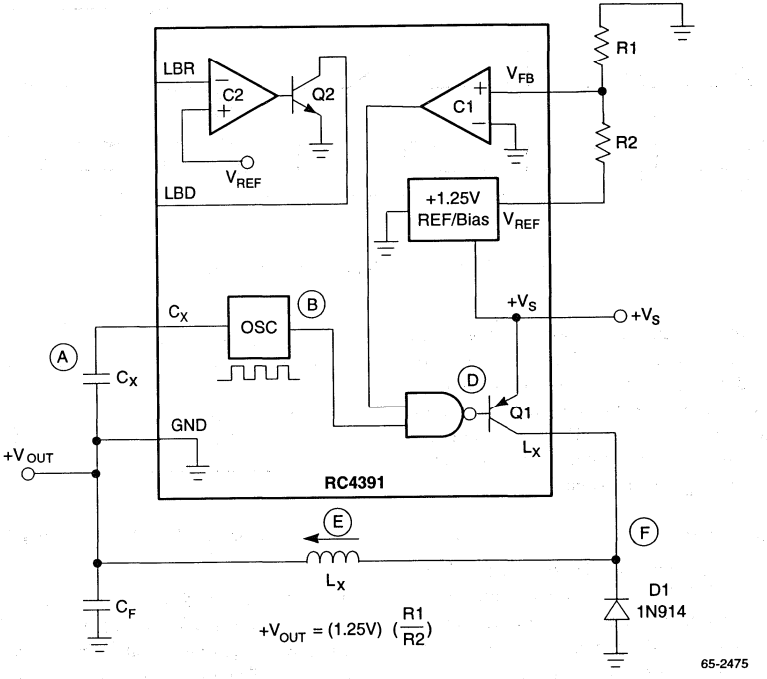
Figure 11 depicts a complete schematic for a step-down circuit using the RC4391. Observe that the ground lead of the 4391 is **not** connected to circuit ground; instead, it is tied to the output voltage. It is by this rearrangement that the feedback system, which senses voltages more negative than the ground lead, can be used to regulate a non-negative output voltage.

When power is first applied, the output filter capacitor is discharged so the ground lead potential starts at 0V. The reference voltage is forced to +1.25V above the ground lead and pulls the feedback input (pin 8) more positive than the ground lead. This positive voltage forces the control network to begin pulsing the switch transistor. As the switching action pumps up the output voltage, the ground lead rises with the output until the voltage on the ground lead is equal to the feedback voltage. At that point, the control network reduces the time on time of the switch to maintain a constant output.

This control network will vary the on time of the switch in response to changes in load current or battery voltage (see Figure 12). If the load current increases (waveform C), then the transistor will remain on (waveformD) for a longer portion of the oscillator cycle, (waveform B), thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and line.

Design Equations

The inductor value and timing capacitor (CX) value must be carefully tailored to the input voltage, input voltage range, output voltage, and load current requirements of the application. The key to the problem is to select the correct inductor value for a given oscillator frequency, such that the inductor current rises to a high enough peak value (IMAX) to meet the average load current drain. The selection of this inductor value must take into account the variation of oscillator frequency from unit to unit and the drift of frequency over temperature. Use ±30% as a maximum variation of oscillator frequency.



Important Note: This circuit must have a minimum load ≥ 1 mA always connected.

Figure 11. Step-Down Regulator – Standard Circuit

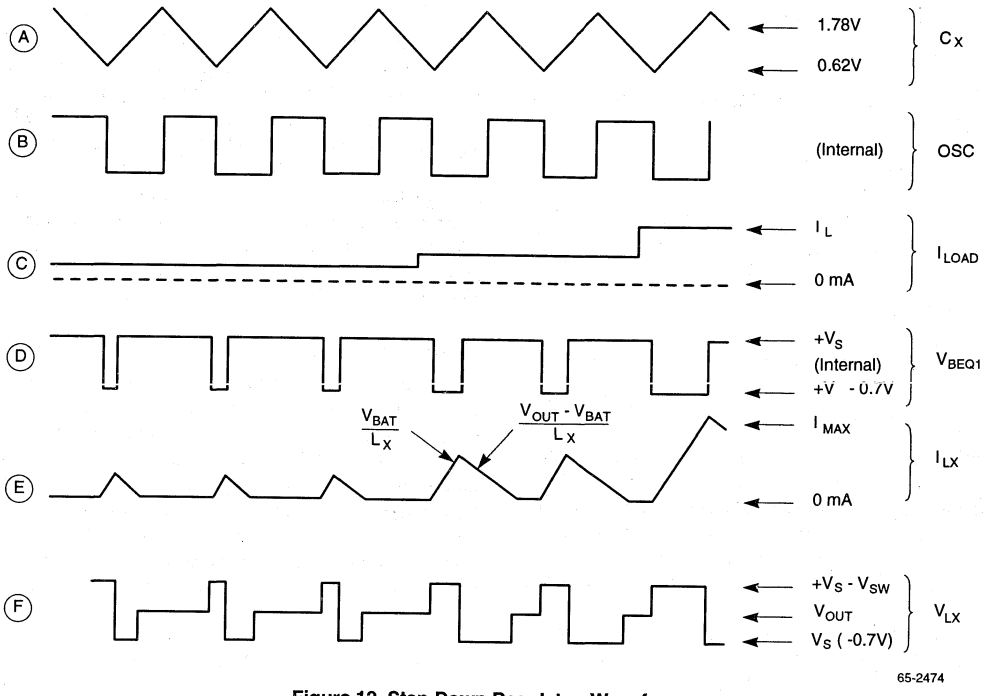


Figure 12. Step-Down Regulator Waveforms

The oscillator creates a squarewave using a method similar to the 555 timer IC, with a current steering flip-flop controlled by two voltage sensing comparators. The oscillator frequency is set by the timing capacitor (C_X) according to the following equation.

$$F_O\,(Hz) = \frac{4.1 \times 10^{-6}}{C_x\,(pF)}$$

The squarewave output of the oscillator is internal and cannot be directly measured, but is equal in frequency to the triangle waveform measurable at pin 3. The switch transistor is normally on when the triangle waveform is ramping up and off when ramping down. Capacitor selection depends on the application; higher operating frequencies will reduce the output voltage ripple and will allow the use of an inductor with a physically smaller inductor core, but excessively high frequencies will reduce load driving capability and efficiency.

Inverting Design Procedure

1. Select an operating frequency and timing capacitor value as shown above (frequencies from 10kHz to 50kHz are typical).
2. Find the maximum on time T_{ON} (add 3µS for the turn off base recombination delay of Q1):

$$T_{ON} = \frac{1}{2F_O} + 3\mu S$$

3. Calculate the peak inductor current IMAX (if this value is greater than 375mA then an external power transistor must be used in place of Q1):

$$I_{MAX} = \frac{(V_{OUT} + V_D)\,2I_L}{(F_O)\,(T_{ON})\,(V_S - V_{SW})}$$

Where:

V_S = Supply Voltage
V_{SW} = Saturation Voltage of Q1 (typically 0.5V)
V_D = Diode Forward Voltage (typically 0.7V)
I_L = DC Load Current

4. Find an inductance value for LX:

$$L_X\,(Henries) = \left(\frac{V_S - V_{SW}}{I_{MAX}}\right)(T_{ON})$$

The inductor chosen must exhibit this value of inductance and have a current rating equal to I_{MAX}.

Step-Down Design Procedure

1. Select an operating frequency.
2. Determine the maximum on time T_{ON} as in the inverting design procedure.
3. Calculate I_{MAX}:

$$I_{MAX} = \frac{2I_L}{(F_O)(T_{ON})\left[\frac{(V_S - V_{OUT})}{(V_{OUT} - V_D)} + 1\right]}$$

4. Calculate L_X:

$$L_X(\text{Henries}) = \left(\frac{V_S - V_{SW}}{I_{MAX}}\right)(T_{ON})$$

Alternate Design Procedure

The design equations above will not work for certain input/output voltage ratios, and for these circuits another method of defining component values must be used. If the slope of the current discharge waveform is much less than the slope of the current charging waveform, then the inductor current will become continuous (never discharging completely), and the equations will become extremely complex. So, if the voltage applied across the inductor during the charge time is greater than during the discharge time, use the design procedure below. For example, a step-down circuit with 20V input and 5V output will have approximately 15V across the inductor when charging, and approximately 5V when discharging. So in this example the inductor current will be continuous and the alternate procedure will be necessary. The alternate procedure may also be used for discontinuous circuits.

1. Select an operating frequency based on efficiency and component size requirements (a value between 10kHz and 50kHz is typical).
2. Build the circuit and apply the worst case conditions to it, i.e., the lowest battery voltage and the highest load current at the desired output voltage.
3. Adjust the inductor value down until the desired output voltage is achieved, then decrease its value by 30% to cover manufacturing tolerances.
4. Check the output voltage with an oscilloscope for ripple, at high supply voltages, at voltages as high as are expected. Also check for efficiency by monitoring supply and output voltages and currents:

$$\left(\text{eff} = \frac{(V_{OUT})(I_{OUT})}{(+V_S)(I_{SY}) \times 100}\right)$$

5. If the efficiency is poor, go back to Step 1 and start over. If the ripple is excessive, then increase the output filter capacitor value or start over.

Compensation

When large values (> 50 kΩ) are used for the voltage setting resistors (R1 and R2 of Figure 8) stray capacitance at the V_{FB} input can add lag to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This can often be avoided by minimizing the stray capacitance at the V_{FB} node. It can also be remedied by adding a lead compensation capacitor of 100 pF to 10 nF. In inverting applications, the capacitor connects between $-V_{OUT}$ and V_{FB}; for step-down circuits it connects between ground and V_{FB}. Most applications do not require this capacitor.

Inductors

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite pot core is recommended; the wind-yourself type with an air gap adjustable by washers or spacers is very useful for bread-boarding prototypes. Care must be taken to choose a core with enough permeability to handle the magnetic flux produced at I_{MAX}. If the core saturates, then efficiency and output current capability are severely degraded and excessive current will flow through the switch transistor. A pot core inductor design section is provided later in this datasheet.

An isolated AC current probe for an oscilloscope (example: Tektronix P6042) is an excellent tool for saturation problems; with it the inductor current can be monitored for nonlinearity at the peaks (a sign of saturation).

Low Battery Detector

An open collector signal transistor Q2 with comparator C2 provides the designer with a method of signaling a display or computer whenever the battery voltage falls below a programmed level (see Figure 13). This level is determined by the +1.25V reference level and by the selection of two external resistors according to the equation:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

When the battery drops below this threshold Q2 will turn on and sink typically 600µA. The low battery detection circuit can also be used for other less conventional applications such as the voltage dependent oscillator circuit of Figure 18.

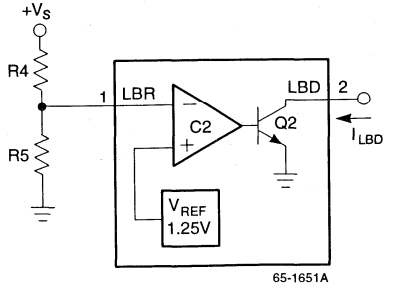


Figure 13. Low Battery Detector

Device Shutdown

The entire device may be shut down to an extremely low current non-operating condition by disconnecting the ground (pin 4). This can be easily done by putting an NPN transistor in series with ground pin and switching it with an external signal. This switch will not affect the efficiency of operation, but will add to and increase the reference voltage by an amount equal to the saturation voltage of the transistor used. A mechanical switch can also be used in series between circuit ground and pin 4, without introducing any reference offset.

Power Transistor Interfaces

The most important consideration in selecting an external power transistor is the saturation voltage at $I_C = I_{MAX}$. The lower the saturation voltage is, the better the efficiency will be. Also, a higher beta transistor requires less base drive and therefore less power will be.

Also, a higher beta transistor requires less base drive and therefore less power will be consumed in driving it, improving efficiency losses in the interface. The part numbers given in the following applications are recommended, but other types may be more appropriate depending on voltage and power levels.

When troubleshooting external power transistor circuits, ensure that clean, sharp-edged waveforms are driving the interface and power transistors. Monitor these waveforms with an oscilloscop—disconnect the inductor, and tie the V_{FB} input (pin 8) high through a 10K resistor. This will cause the regulator to pulse at maximum duty cycle without drawing excessive inductor currents. Check for expected on time and off time, and look for slow rise times that might cause the power transistor to enter its linear operating region.

The following external power transistor circuits may demand some adjustment to resistor values to satisfy various power levels and input/output voltages. C_X and L_X values must be selected according to the design equations (pages 2-213 and 2-214).

Inverting Medium Power Application

Figure 8 is a schematic of an inverting medium power supply (250mW to 1W) using an external PNP switch transistor. Supply voltage is applied to the IC via R3: when the internal switch transistor is turned on current through R4 is also drawn through R3; creating a voltage drop from base to emitter of the external switch transistor. This drop turns on the external transistor.

Voltage pulses on the supply lead (pin 6) do not affect circuit operation because the internal reference and bias circuitry have good supply rejection capabilities. A power Schottky diode is used for higher efficiency.

Inverting High Power Application

For higher power applications (500mW to 5W), refer to Figure 9. This circuit uses an extra external transistor to provide well controlled drive current in the correct phase to the power switch transistor. The value of R3 sets the drive current to the switch by making the interface transistor act as a current source. R4 and R5 must be selected such that the RC time constant of R4 and the base capacitance of Q2 do not slow the response time (and affect duty cycle), but not so low in value that excess power is consumed and efficiency suffers. The resistor values chosen should be proportional to the supply voltage (values shown are for +5V).

Step-Down Power Applications

Figures 16 and 17 show medium and high power interfaces modified to perform step-down functioning. The design

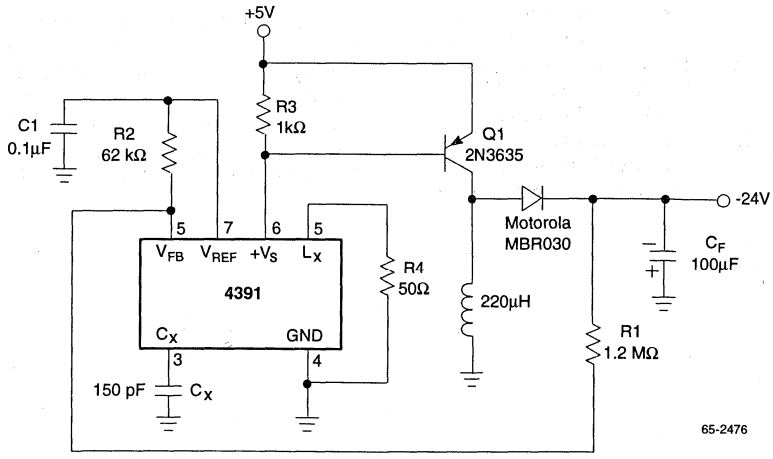


Figure 14. Inverting Medium Power Application

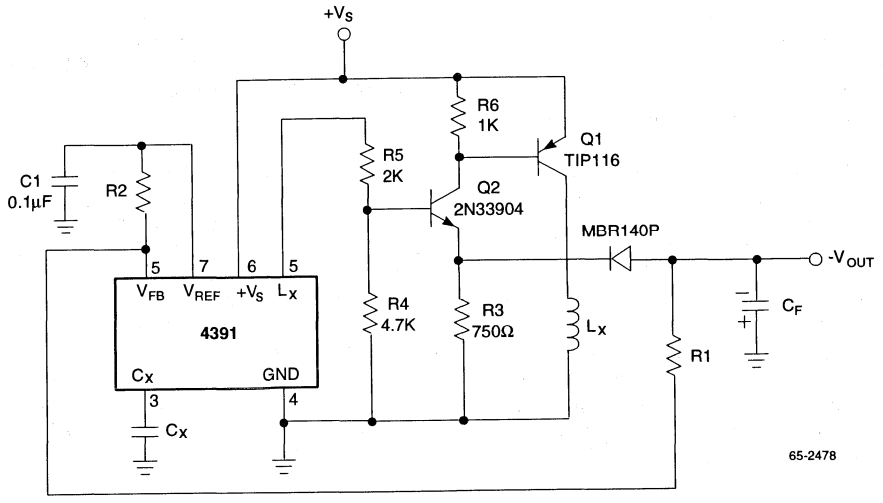


Figure 9. Inverting High Power Application

equations and suggestions for the circuits of Figures 14 and 15 also apply to these circuits. For a certain range of load power, the RC4193 can be used for step-sown applications. A load range from 400mW to 2W can be sustained with fewer components (especially when stepping down greater than 30V) than the comparable RC4391 circuit. Refer to Raytheon's RC4191/4192/4193 data sheet for a schematic of this medium power step-down application.

Voltage Dependent Oscillator

The RC4391's ability to supply load current at low battery voltages depends on the inductor value and the oscillator frequency. Low values of inductance or a low oscillator frequency will cause a higher peak inductor current and therefore increase the load current capability. A large inductor current is not necessarily best , however, because the large amount of energy delivered with each cycle will cause a large voltage ripple at the output, especially at high input voltages. This trade-off between load current capability and output ripple can be improved with the circuit connection shown in Figure 18. This circuit uses the low battery detector to sense for a low battery voltage condition and will decrease the oscillator frequency after a pre- programmed threshold is reached.

The threshold is programmed exactly as the normal low battery detector connection:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

When the battery voltage reaches this threshold the comparator will turn on the open collector transistor at pin 2, effectively pulling C_Y in parallel with C_X. This added capacitance will reduce the oscillator frequency, according to the following equation:

$$F_O(Hz) = \frac{4.1 \times 10^{-6}}{C_X(pF) + C_Y(pF)}$$

Current Limiting

The oscillator (C_X) pin can be used to add short circuit protection and to protect against over current at start-up (when using large values for the output filter capacitor —greater than 100 µF). A transistor V_{BE} is used as a current sensing comparator which resets the oscillator upon sensing an over current condition, thus providing cycle-by-cycle current limiting. Figure 19 shows how this is applied.

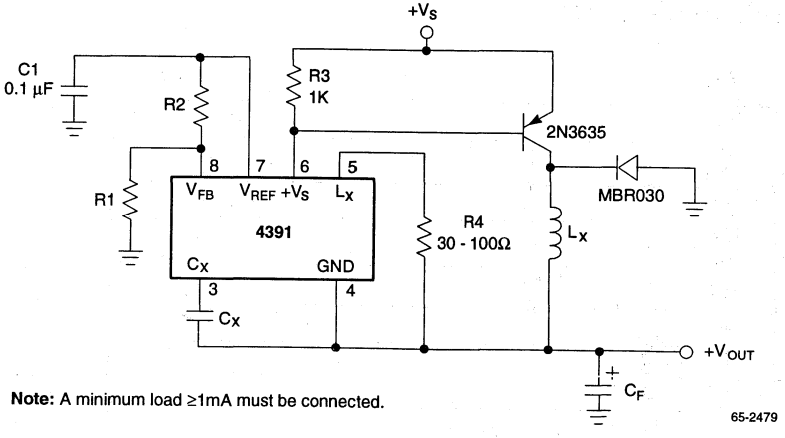


Figure 16. Step-Down Medium Power Application

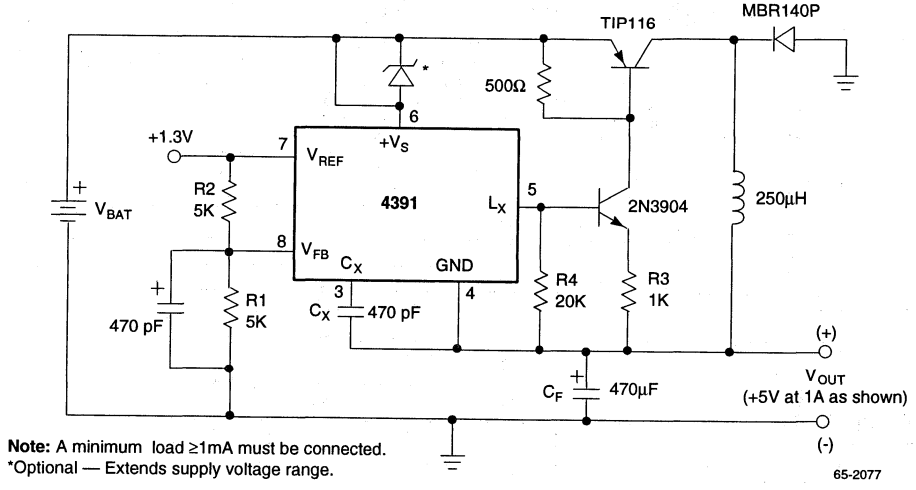


Figure 17. Step-Down High Power Application

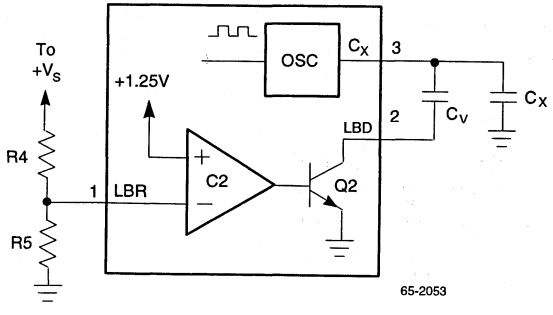


Figure 18. Voltage Dependent Oscillator

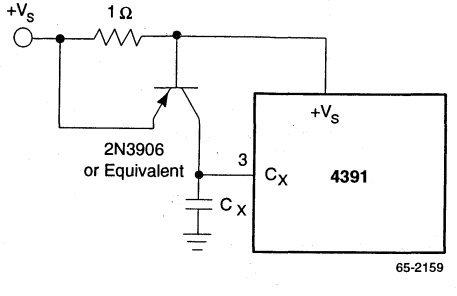
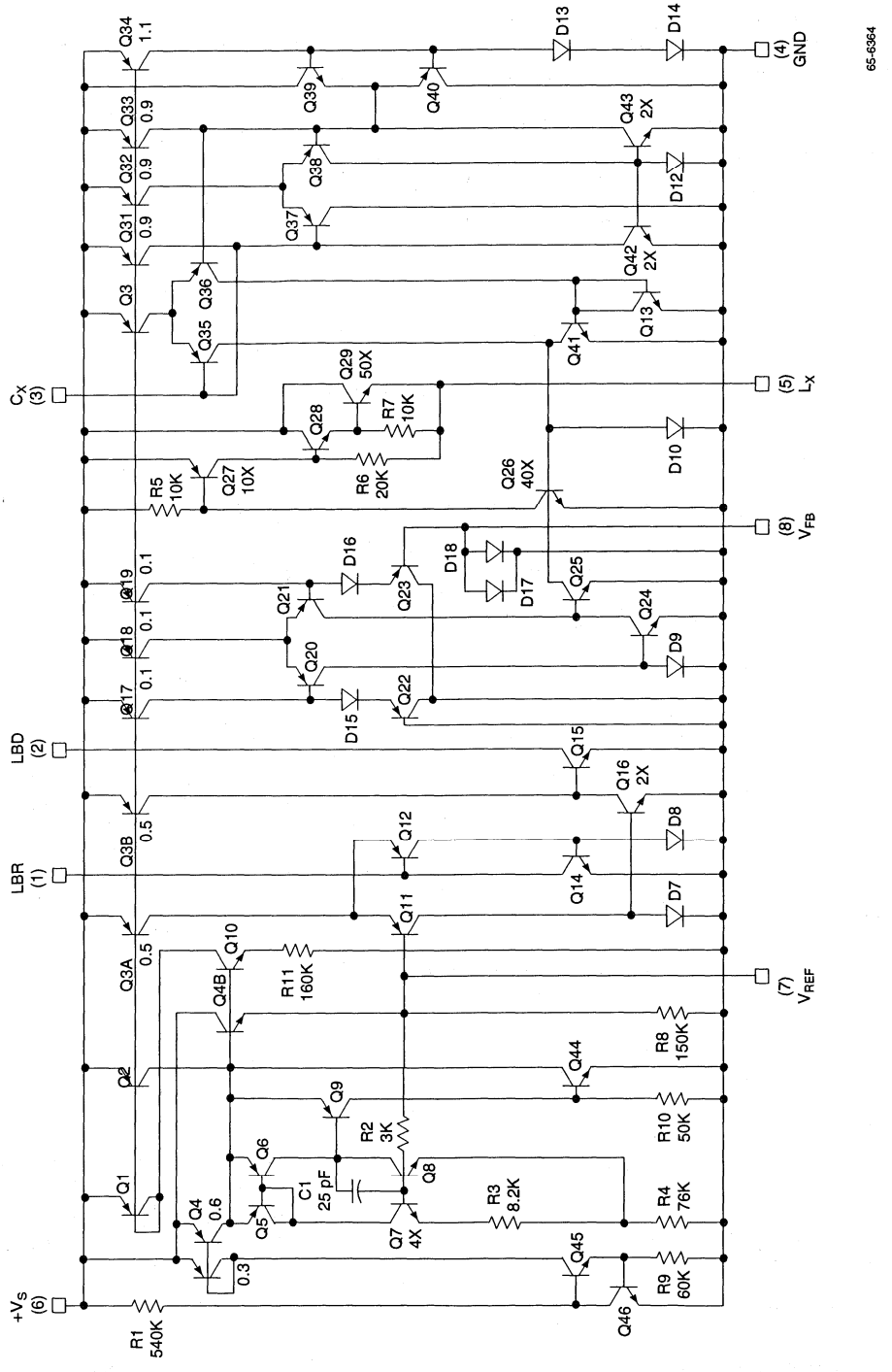
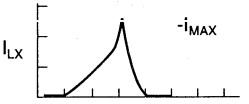
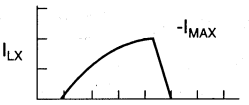
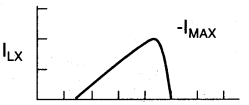


Figure 18. Current Limiting

Simplified Schematic Diagram



Troubleshooting Chart

Symptom	Possible Problems
Draws excessive supply current on star-up.	Inductance value too low. Output frequency (F_O) too low. Combination of low resistance inductor and high value filter capacitor — needs current limiting circuit (Figure 13).
Output voltage is low.	Inductance value too high for F_O or core saturating.
Inductor "sings" with audible hum.	Not potted well or bolted loosely.
L_X pin appears noisy — scope will not synchronize.	Normal operating condition.
 Inductor current shows nonlinear waveform.	Inductor is saturating: 1. Core too small. 2. Core too hot. 3. Operating frequency too low.
 Inductor current shows nonlinear waveform.	Waveform has resistive component: 1. Wire size too small. 2. Power transistor lacks base drive. 3. Components not rated high enough. 4. Battery has high series resistance.
 Inductor current is linear until high current is reached.	External transistor lacks base drive or beta is too low.
Poor efficiency.	Core saturating. Diode or transistor: 1. Not fast enough. 2. Not rated for current level (high $V_{CE}SAT$). High series resistance. Operating frequency too high.
Motorboating (erratic current pulses).	Loop stability problem — needs feedback from V_{OUT} to V_{FB} (pin 8), 100pF to 1000pF

Pot Core Inductor Design

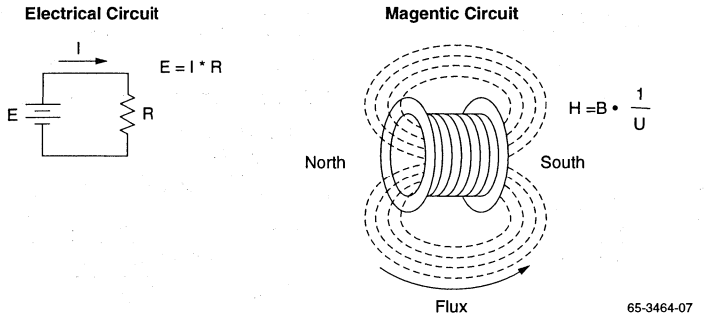


Figure 20. Electricity vs. Magnetism

Electricity Versus Magnetism

Electrically the inductor must meet just one requirement, but that requirement can be hard to satisfy. The inductor must exhibit the correct value of inductance (L, in Henrys) as the inductor current rises to its highest operating value (I_{MAX}). This requirement can be met most simply by choosing a very large core and winding it until it reaches the correct inductance value, but that brute force technique wastes size, weight and money. A more efficient design technique must be used.

Question: What happens if too small a core is used?

First, one must understand how the inductor's magnetic field works. The magnetic circuit in the inductor is very similar to a simple resistive electrical circuit. There is a magnetizing force (H, in oersteds), a flow of magnetism, or flux density (B, in Gauss), and a resistance to the flux, called permeability (U, in Gauss per oersted). H is equivalent to voltage in the electrical model, flux density is like current flow, and permeability is like resistance (except for two important differences discussed to the right).

First Difference: Permeability instead of being analogous to resistance, is actually more like conductance (1/R). As permeability increases, flux increases.

Second Difference: Resistance is a linear function. As voltage increases, current increases proportionally, and the resistance value stays the same. In a magnetic circuit the value of permeability varies as the applied magnetic force varies. This nonlinear characteristic is usually shown in graph form in ferrite core manufacturer's data sheet.

As the applied magnetizing force increases, at some point the permeability will start decreasing, and therefore the amount of magnetic flux will not increase any further, even as the magnetizing force increases. The physical reality is that, at the point where the permeability decreases, the magnetic field has realigned all of the magnetic domains in the core material. Once all of the domains have been aligned the core will then carry no more flux than just air, it becomes as if there were no core at all. This phenomenon is called saturation. Because the inductance value, L, is dependent on the amount of flux, core saturation will cause the value of L to decrease dramatically, in turn causing excessive and possibly destructive inductor current.

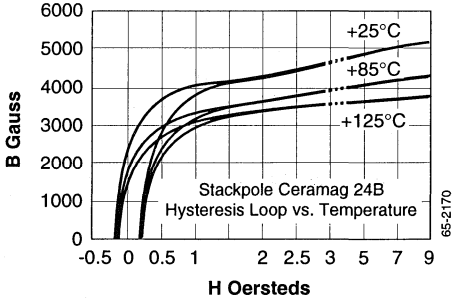


Figure 21. Typical Manufacturer's Curve Showing Saturation Effects

Pot Cores for RC4391

Pot core inductors are best suited for the RC4391 switching regulator for several reasons:

1. **They are available in a wide range of sizes.** RC4391 applications are usually low power with relatively low peak currents (less than 500mA). A small inexpensive pot core can be chosen to meet the circuit requirements.

2. **Pot cores are easily mounted.** They can be bolted directly to the PC card adjacent to the regulator IC.

3. **Pot cores can be easily air-gapped.** The length of the gap is simply adjusted using different washer thicknesses. cores are also available with predetermined air gaps.

4. **Electromagnetic interference (EMI) is kept to a minimum.** the completely enclosed design of a pot core reduces stray electromagnetic radiation—an important consideration if the regulator circuit is built on a PC card with other circuitry.

Not quite. Core size is dependent on the amount of energy stored, not on load power. Raising the operating frequency allows smaller cores and windings. Reduction of the size of the magnetics is the main reason switching regulator design tends toward higher operating frequency. Designs with the RC4391 should use 75 kHz as a maximum running frequency, because the turn off delay of the power transistor and stray capacitive coupling begin to interfere. Most applications are in the 10 to 50 kHz range, for efficiency and EMI reasons.

The peak inductor current (I_{MAX}) must reach a high enough value to meet the load current and simultaneously the inductor value is decreased, then the core can be made smaller. For a given core size and winding, an increase in air gap spacing (an air gap is a break in the material in the magnetic path, like a section broken off a doughnut) will cause the inductance to decrease and I_{MAX} (the usable peak current before saturation)to increase.

The curves shown are typical of the ferrite manufacturer's power HF material, such as Siemens N27 or Stackpole 24B, which are usually offered in standard millimeter sizes including the sizes shown.

Use of the Design Aid Graph

1. From the application requirement, determine the inductor value (L) and the required peak current (I_{MAX}).

2. Observe the curves of the design aid graph and determine the smallest core that meets both the L and I requirements.

3. Note the approximate air gap at IMAX for the selected core, and order the core with the gap. (If the gapping is done by the user, remember that a washer lspacer results in an air gap of twice the washer thickness, because two gaps will be created, one at the center post and one at the rim, like taking two bites from a doughnut.)

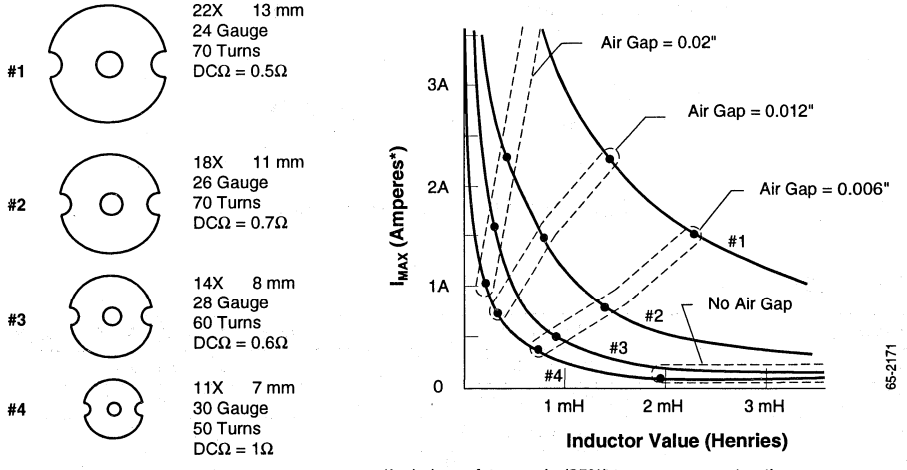
4. If the required inductance is equal to the indicated value on the graph, then wind the core with the number of turns shown in the table of sizes. The turns given are the maximum number for that gauge of wire that can be easily wound in cores winding area.

5. If the required inductance is less than the value indicated on the graph, a simple calculation must be done to find the adjusted number of turns. Find A_L (inductance index) for a specific air gap.

$$\frac{L\,(\text{indicated})}{\text{Turns}^2} = A_L\left(\frac{\text{inHenries}}{\text{Turn}^2}\right)$$

Then divide the required inductance value by A_L to give the actual turns squared, and take the square root to find the actual turns needed.

$$\text{ActualTurns} = \frac{L\,(\text{required})}{A_L}$$



*Includes safety margin (25%) to ensure nonsaturation

Figure 22. Inductor Design Aid

If the actual number of turns is significantly less than the number from the table then the wire size can be increased to use up the leftover winding area and reduce resistive losses.

6. Wind and gap the core as per calculations, and measure the value with an inductance meter. Some adjustment of the number of turns may be necessary.

The saturation characteristics may be checked with the inductor wired into the switching regulator application circuit. To do so, build and power up the circuit. Then clamp an oscilloscope current probe (recommend Tektronix P6042 or equivalent) around the inductor lead and monitor the current in the inductor. Draw the maximum load current from the application circuit so that the regulator is running at close to full duty cycle. Compare the waveform you see to those pictured.

Check for saturation at the highest expected ambient temperature.

7. After the operation in circuit has been checked, reassemble and pot the core using a potting compound recommended by the manufacturer.

   If the core material differs greatly in magnetic characteristics from the standard power material shown in Figure 16, then the following general equation can be used to help in winding and gapping. This equation can be used for any core geometry, such as an E-E core.

$$L_X = \frac{(1.26)\ (N^2)\ (Ae)\ (10^8)}{g = (le/ue)}$$

Where:

N = number of turns
Ae = core area from data sheet (in cm2)
le = magnetic path length from data sheet (in cm)
ue =permeability of core from manufacturer's graph
g = center post air gap (in cm)

Manufacturers

Below is a list of several pot core manufacturers:

Ferroxcube Company
5083 Kings Highway
Saugerties, NY 12477

Indiana General Electronics
Keasley, NJ 08832

Siemens Company
186 Wood Avenue South
Iselin, NJ 08830

Stackpole Company
201 Stackpole Street
St. Mary, PA 15857

TDK Electronics
13-1, 1-Chrome
Nihonbaski, Chuo-ku, Tokyo

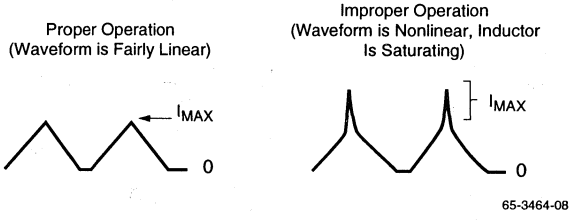


Figure 23. Inductor Current Waveforms

Ordering Information

Part Number	Package	Operating Temperature Range
RC4391N	8 Lead Plastic DIP	0°C to +70°C
RC4391M	8 Lead Plastic SOIC	0°C to +70°C
RV4391N	8 Lead Plastic DIP	-25° C to +85°C
RM4391D	8 Lead Ceramic DIP	-55°C to +125°C

RC2211
FSK Demodulator/Tone Decoder

Features

- Wide frequency range – 0.01 Hz to 300 kHz
- Wide supply voltage range – 4.5V to 20V
- DTL/TTL/ECL logic compatibility
- FSK demodulation with carrier-detector
- Wide dynamic range – 2 mV to 3 V_{RMS}
- Adjustable tracking range – ±1% to ±80%
- Excellent temperature stability – 20 ppm/°C typical

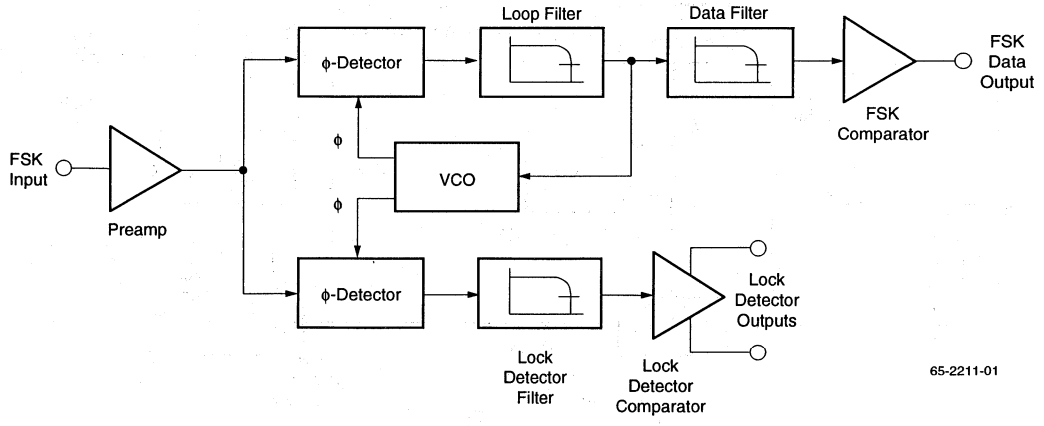
Applications

- FSK demodulation
- Data synchronization
- Tone decoding
- FM detection
- Carrier detection

Description

The RC2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well-suited for FSK modem applications, and operates over a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth and output delay.

Block Diagram



Description of Circuit Controls

Signal Input (Pin 2)

The input signal is AC coupled to this terminal. The internal impedance at pin 2 is 20 kΩ. Recommended input signal level is in the range of 10 mV_{RMS} to 3 V_{RMS}.

Quadrature Phase Detector Output, Q (Pin 3)

This is the high impedance output of the quadrature phase detector, and is internally connected to the input of lock detector voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 1) to eliminate chatter at the lock detector outputs. If this tone detector section is not used, pin 3 can be left open circuited.

Lock Detector Output, Q (Pin 5)

The output at pin 5 is at a "high" state when the PLL is out of lock and goes to a "low" or conducting state when the PLL is locked. It is an open collector output and requires a pull-up resistor, R_L, to $+V_S$ for proper operation. In the "low" state it can sink up to 5 mA of load current.

Lock Detector Complement, $\overline{Q}$ (Pin 6)

The output at pin 6 is the logic complement of the lock detector output at pin 5. This output is also an open collector type stage which can sink 5 mA of load current in the low or "on" state.

FSK Data Output (Pin 7)

This output is an open collector stage which requires a pull-up resistor, R_L, to $+V_S$ for proper operation. It can sink 5 mA of load current. When decoding FSK signals the FSK data output will switch to a "high" or off state for low input frequency, and will switch to a "low" or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

FSK Comparator Input (Pin 8)

This is the high impedance input to the FSK voltage comparator. Normally, an FSK post detection or data filter is connected between this terminal and the PLL phase detector output (pin 11). This data filter is formed by R_F and C_F of Figure 1. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at pin 10.

Reference Bypass (Pin 9)

This pin can have an optional 0.1, µF capacitor connected to the ground.

Reference Voltage, V_R (Pin 10)

This pin is internally biased at the reference voltage level, V_R; $V_R = +V_S/2 - 650$ mV. The DC voltage level at this pin forms an internal reference for the voltage levels at pin 3, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1 µF capacitor.

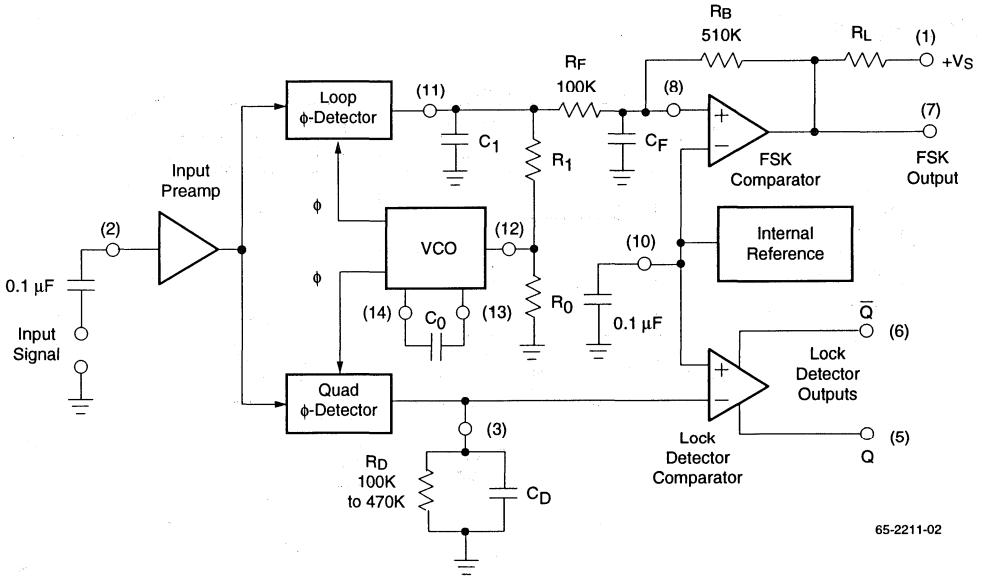


Figure 1. Generalized Circuit Connection for FSK and Tone Detection

Loop Phase Detector Output (Pin 11)

This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R1 and C1 connected to pin 11 (see Figure 1). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

VCO Control Input (Pin 12)

VCO free running frequency is determined by external timing resistor, R0, connected from this terminal to ground. The VCO free running frequency, F_0 is given by:

$$F_0\,(Hz) = \frac{1}{R_0 C_0}$$

where C_0 is the timing capacitor across pins 13 and 14. For optimum temperature stability R_0 must be in the range of 10 kΩ to 100 kΩ (see Typical Performance Characteristics).

This terminal is a low impedance point, and is internally biased at a DC level equal to V_R. The maximum timing current drawn from pin 12 must be limited to ≤3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14)

VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals. C_0 must be non-polarized, and in the range of 200 pF to 10 µF.

VCO Frequency Adjustment

VCO can be fine tuned by connecting a potentiometer, Rx, in series with R_0 at pin 12 (see Figure 2).

VCO Free-Running Frequency, F_0

The RC2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. However, for set-up or adjustment purposes, the VCO freerunning frequency can be measured at pin 3 (with C_D disconnected) with no input and with pin 2 shorted to pin 10.

Design Equations

See Figure 1 for Definitions of Components.

1. VCO Center Frequency, F_0:

$$F_0\,(Hz) = \frac{1}{R_0 C_0}$$

2. Internal Reference Voltage, V_R (measured at pin 10)

$$V_R = \left(\frac{+V_S}{2}\right) - 650\ mV$$

3. Loop Lowpass Filter Time Constant, τ

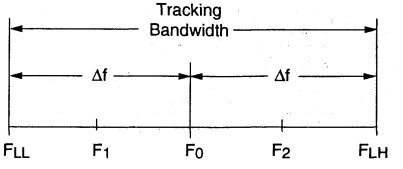
$$\tau = R_1 C_1$$

4. Loop Dampening, ζ:

$$\zeta = \left(\sqrt{\frac{C_0}{C_1}}\right)\left(\frac{1}{4}\right)$$

5. Loop Tracking Bandwidth, $\pm\Delta F/F_0$:

$\Delta f/F_O = R0/R1$



65-2211-03

6. FSK Data Filter Time Constant, τ_F:

$$\tau_F = R_F C_F$$

7. Loop Phase Detector Conversion Gain, $K\phi$ ($K\phi$ is the differential DC voltage across pins 10 and 11, per unit of phase error at phase-detector input):

$$k\phi\,(\text{in volts per radian}) = \frac{(-2)\,(V_R)}{\pi}$$

8. VCO Conversion Gain, K_0 is the amount of change in VCO frequency per unit of DC voltage change at pin 11:

$$K0\,(\text{in Hertz per volt}) = \frac{-1}{C_0 R_1 V_R}$$

9. Total Loop Gain, K_T:

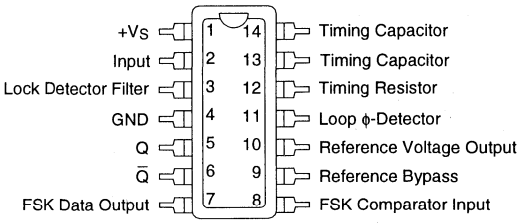
$$K_T\,(\text{in radians per second per volt}) = 2\,\pi K\phi K0$$

$$= \frac{4}{C_0 R_1}$$

10. Peak Phase Detector Current, I_A:

$$I_A\,(mA) = \frac{V_R}{25}$$

Pin Assignments



65-2211-04

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage		-20	+20	V
Input Signal Level			3	V_{RMS}
Storage Temperature Range		-65	+150	°C
Operating Temperature Range	RM2211D	-55	+125	°C
	RV2211N	-25	+85	°C
	RC2211N	-0	+70	°C
Junction Temperature	PDIP		+125	°C
	CerDIP		+175	°C
Lead Soldering Temperature (60 sec.)			+300	°C
Max. P_D T_A<50°C	PDIP		468	mW
	CerDIP		1042	mW

Thermal Characteristics

Parameter	14 Lead Plastic DIP	14 Lead Ceramic DIP
Therm. Res θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For T_A > 50°C Derate at	6.5 mW/°C	8.33 mW/°C

Electrical Characteristics

(Test Conditions $+V_S$ = +12V, T_A +25°C, R0 = 30 kΩ, C0 = 0.033 µF. See Figure 1 for component designations.)

Parameters	Test Conditions	RV/RM2211			RC2211			Units
		Min	Typ	Max	Min	Typ	Max	
General								
Supply Voltage[2]		4.5		20	4.5		20	V
Supply Current	$R_0 \geq 10$ kΩ		4.0	9.0		5.0	11	mA
Oscillator								
Frequency Accuracy	Deviation from $f_0 = 1/R_0C_0$		±1.0	±3.0		±1.0		%
Frequency Stability[1]								
Temperature Coefficient	$R_1 = \infty$		±20	±50		±20		ppm/°C
Power Supply Rejection	$+V_S$ = 12 ±1V		0.05	0.5		0.05		%/V
	$+V_S$ = 5 ±0.5V		0.2		0.2			%/V
Upper Frequency Limit	R_0 = 8.2 kΩ, C_0 = 400 pF	100	300			300		kHz
Lowest Practical Operating Frequency[1]	R_0 = 2 MΩ, C_0 = 50 µF			0.01		0.01		Hz
Timing Resistor, R_0								
Operating Range		5.0		2000	5.0		2000	kΩ
Recommended Range		15		100	15		100	kΩ
Loop Phase Detector								
Peak Output Current	Measured at pin 11	±150	±200	±300	±100	±200	±300	µA
Output Offset Current			±1.0			±2.0		µA
Output Impedance			1.0			1.0		MΩ
Maximum Swing	Ref. to pin 10	±4.0	±5.0		±4.0	±5.0		V
Quadrature Phase Detector								
Peak Output Current[3]	Measured at pin 3	100	150			150		µA
Output Impedance			1.0			1.0		MΩ
Maximum Swing			11			11		V_{P-P}
Input Preamp								
Input Impedance	Measured at pin 2		20			20		kΩ
Input Signal Voltage Required to Cause Limiting[3]			2.0	10		2.0		mV_{RMS}
Voltage Comparator								
Input Impedance	Measured at pins 3 & 8		2.0			2.0		MΩ
Input Bias Current			100			100		nA
Voltage Gain[1]	R_L = 5.1 kΩ	55	70		55	70		dB
Output Voltage Low	I_C = 3mA		300			300		mV
Output Leakage Current	V_0 = 12V		0.01			0.01		µA
Internal Reference								
Voltage Level	Measured at pin 10	4.9	5.3	5.7	4.75	5.3	5.85	V
Output Impedance			100			100		Ω

Notes:

1. Guaranteed by design.
2. Individual applications may need special circuitry to function at <12V.
3. Sample tested.

Applications

FSK Decoding

Figure 2 shows the basic circuit connection for FSK decoding. With reference to Figures 1 and 2, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one pole post-detection filter for the FSK data output. The resistor R_B (510 kΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bauds are given in Table 1.

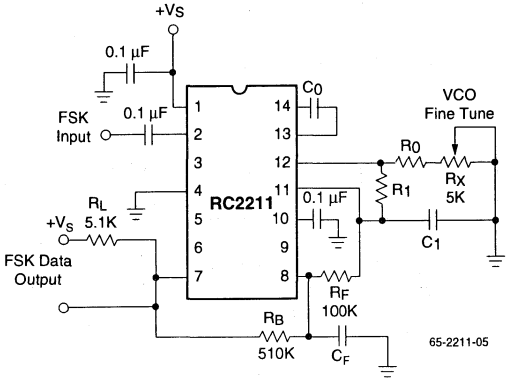


Figure 2. Circuit Connectbn for FSK Decoding

Table 1. Recommended Component Values for Commonly Used FSK Bands

(see Circuit of Figure 2)

FSK Band	Component Values
300 Baud	C_0 = 0.039 µF, C_F = 0.005 µF
F_1 = 1070 Hz	C_1 = 0.01 µF, R_0 = 18 kΩ
F_2 = 1270 Hz	R_1 = 100 kΩ
300 Baud	C_0 = 0.022 µF, C_F = 0.005 µF
F_1 = 2025 Hz	C_1 = 0.0047 µF, R_0 = 18 kΩ
F_2 = 2225 Hz	R_1 = 200 kΩ
1200 Baud	C_0 = 0.027 µF, C_F = 0.0022 µF
F_1 = 1200 Hz	C_1 = 0.01 µF, R_0 = 18 kΩ
F_2 = 2200 Hz	R_1 = 30 kΩ

Design Instructions

The circuit of Figure 2 can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, F_1 and F_2, these parameters can be calculated as follows:

1. Calculate PLL center frequency, F_0

$$F_0 = \frac{F_1 + F_2}{2}$$

2. Choose a value of timing resistor R_0 to be in the range of 10 kΩ to 100 kΩ. This choice is arbitrary. The recommended value is R_0 = 20 kΩ. The final value of R_0 ios normally finetuned with the series potentiometer, R_X.

3. Calculate value of C_0 from Design Equation No. 1 or from Typical Performance Characteristics:

$$C_0 = 1/R_0F_0$$

4. Calculate R_1 to give a Δf equal to the markspace deviation:

$$R_1 = R_0 [F_0/(F_1 - F_2)]$$

5. Calculate C_1 to set loop damping. (See Design Equation No. 4)

Normally, $\zeta \approx 1/2$ is recommended
Then: $C_1 = C_0/4$ for $\zeta = 1/2$

6. Calculate Data Filter Capacitance, C_F:
For R_F = 100 kΩ, R_B = 510 kΩ, the recommended value of C_F is:

$$C_F \text{ (in µF)} = \frac{3}{\text{Baud Rate}}$$

Note: All calculated component values except RO can be rounded off to the nearest standard value, and R0 can be varied to fine-tune center frequency through a series potentiometer, R_X (see Figure 2).

Design Example

75 Baud FSK demodulator with mark space frequencies of 1110/1170 Hz:

Step 1: Calculate F_0:
F_0=(1110+1170)(1/2)= 1140Hz

Step 2: Choose R_0 = 20 kΩ (18 kΩ fixed resistor in series with 5 kΩ potentiometer)

Step 3: Calculate C_0 from VCO Frequency vs. Timing Capacitor: C_9 = 0.044µF

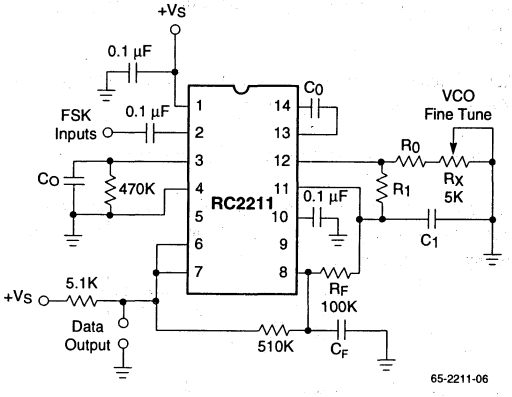
Step 4: Calculate R_1: $R_1 = R_0$ (1140/60) = 380 kΩ

Step 5: Calculate C_1: $C_1 = C_0/4$ = 0.011 µF

Note: All values except R_0 can be rounded off to nearest standard value.

FSK Decoding with Carrier Detector

The lock detector section of the RC2211 can be used as a carrier detector option for FSK decoding. The recommended circuit connection for this application is shown in Figure 3. The open-collector lock detector output, pin 6, is shorted to the data output (pin 7). Thus, the data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the pin 6 output goes "high" to enable the data output.



Note: Data output is "low" when no carrier is present.

Figure 3. External Connections for FSK Demodulation with Carrier Detector Capability

The minimum value of the lock detector filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_C$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta F_C < \Delta F/2$. For R_D = 470 kΩ, the approximate minimum value of C_D can be determined by:

$$C_D(\mu F) \geq 16/\text{capture range in Hz}$$

With values of C_D that are too small, chatter can be observed on the lock detector output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detector output.

Tone Detection

Figure 4 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs becomes reversed to the duration of the input tone. Each logic output can sink 5 mA of load current.

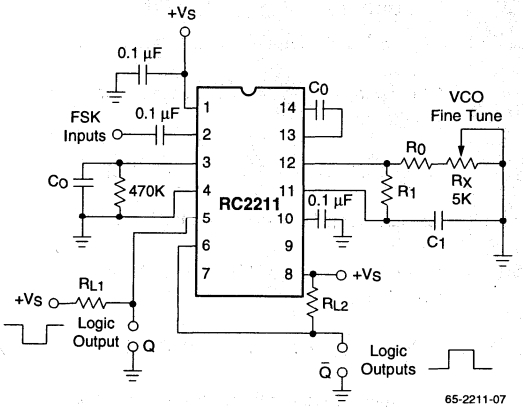


Figure 4. Circuit Connection for Tone Detection

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2} as shown in Figure 4.

With reference to Figures 1 and 4, the function of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency, R_1 sets the detection bandwidth, C_1 sets the lowpass-loop filter time constant and the loop dampening factor, and R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

Design Instructions

The circuit of Figure 4 can be optimized for any tone-detection application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input tone frequency, F_S, these parameters are calculated as follows:

1. Choose R_0 to be in the range of 15 kΩ to 100 kΩ. This choice is arbitrary.
2. Calculate C_0 to set center frequency, f_0 equal to F_S: $C_0 = 1/R_0F_S$.
3. Calculate R_1 to set bandwidth $\pm\Delta F$ (see Design Equation No. 5): $R_1 = R_0(F_0/\Delta F)$. Note: The total detection bandwidth covers the frequency range of $F_0 \pm \Delta F$.
4. Calculate value of C_1 for a given loop damping factor:

   $C_1 = C_0/16\zeta^2$

   Normally ζ = 1/2 is optimum for most tone detector applications, giving C_1 = 0.25 C_0.

   Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.
5. Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470Ω, C_D must be:

   $C_D(\mu F) \geq (16/\text{capture range in Hz})$

   Increasing C_D slows the logic output response time.

Design Examples

Tone detector with a detection band of 1 kHz ±20 Hz:

Step 1: Choose R_0 = 20 kΩ (18 kΩ in series with 5 kΩ potentiometer) .

Step 2: Choose C_0 for F_0 = 1 kHz: C_0 = 0.05 µF.

Step 3: Calculate R_1: $R_1 = (R_0)\ (1000/20)$ = 1 MΩ.

Step 4: Calculate C_1: for $\zeta = 1/2$, C_1 = 0.25 µF, C_0 = 0.013 µF.

Step 5: Calculate C_D: $C_D = 16/38$ = 0.42 µF.

Step 6: Fine tune the center frequency with the 5 kΩ potentiometer. R_X.

Linear FM Detection

The RC2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown in Figure 5. The demodulated output is taken from the loop phase detector output (pin 11), through a post detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 5.

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{OUT} = R_1\ V_R/100\ R_0 \text{ Volts/\% deviation}$$

where V_R is the internal reference voltage. For the choice of external components R_1, R_0, C_0, C_1 and C_F, see the section on Design Instructions.

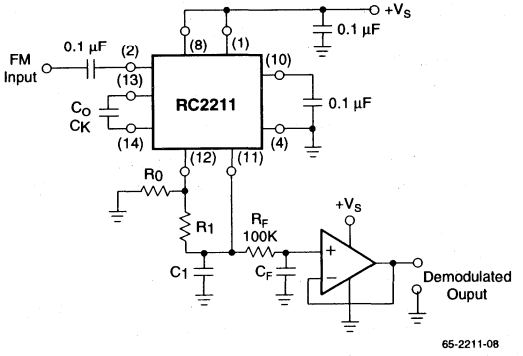


Figure 5. Linear FM Detector Using RC2211 and an External Op Amp

Typical Performance Characteristics

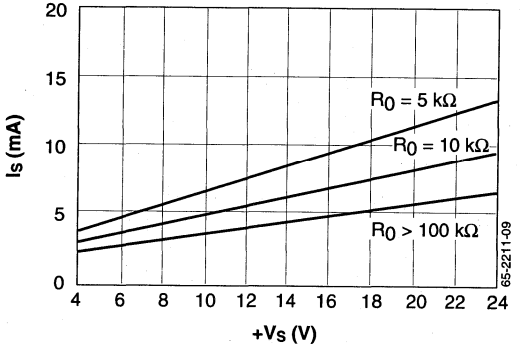


Figure 6. Supply Current vs. Supply Voltage (Logic Outputs Open Circuited)

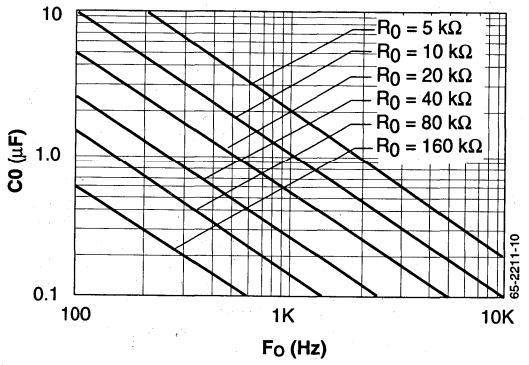


Figure 7. Timing Resistor with Timing Capacitor vs. VCO Frequency

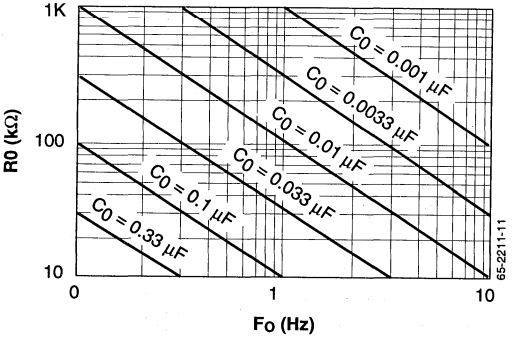


Figure 8. Timing Capacitor with Timing Resistor vs. VCO Frequency

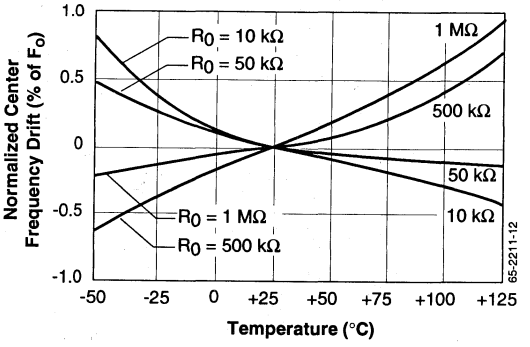
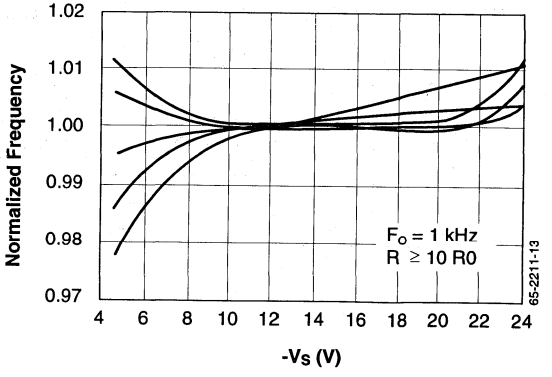


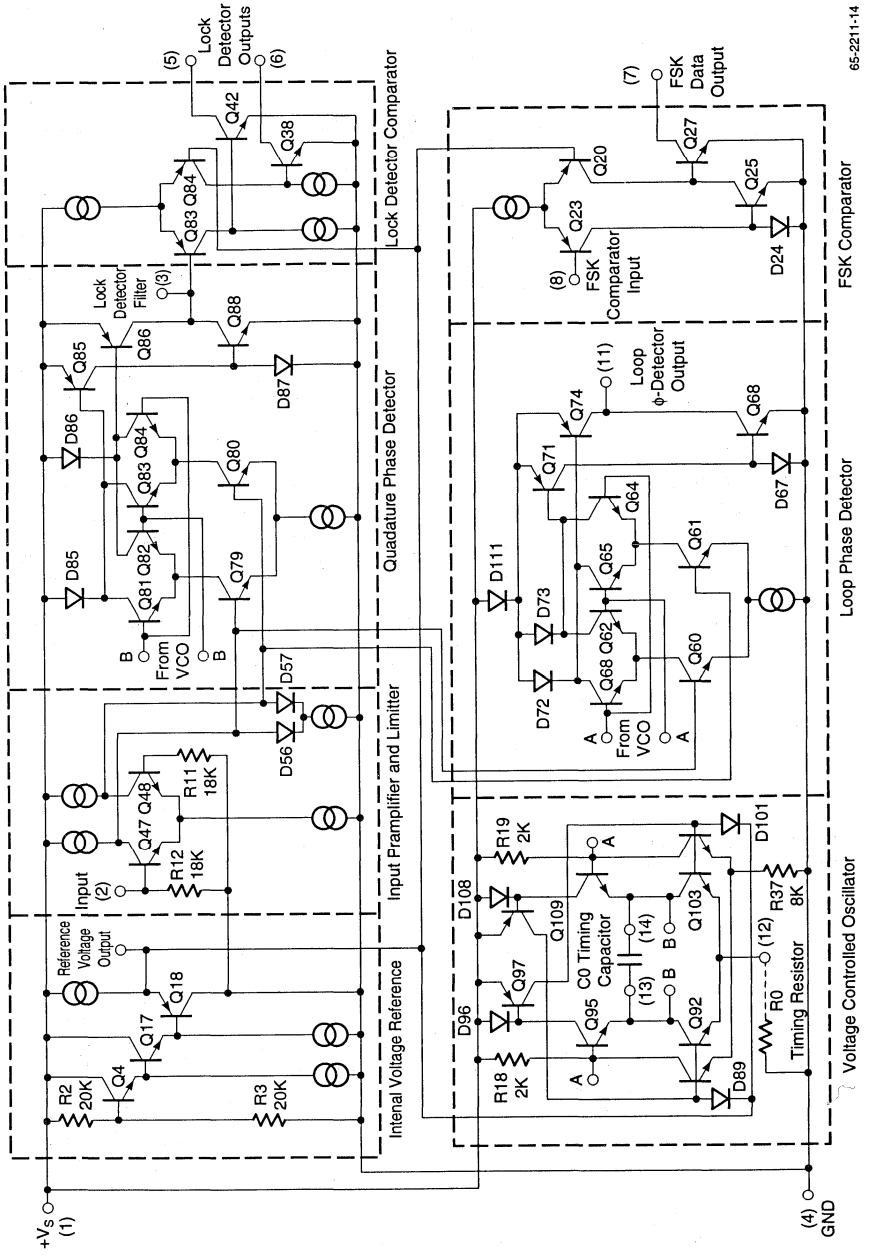
Figure 9. Center Frequency Drift vs. Temperature



Curve	R0
1	5K
2	10K
3	30K
4	100K
5	300K

Figure 10. VCO Frequency vs. Supply Voltage

Schematic Diagram



Ordering Information

Part Number	Package	Operating Temperature Range
RC2211N	N	0°C to +70°C
RV2211N	N	-25°C to +85°C
RM2211D	D	-55°C to +125°C
RM2211D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Par 1.2.1 Compliant Devices
N = 14-Lead Plastic DIP
D = 14-Lead Ceramic DIP

THIS PAGE INTENTIONALLY LEFT BLANK

RC4200
Analog Multiplier

Features

- High accuracy
- Nonlinearity – 0.1%
  Temperature coefficient – 0.005%/°C
- Multiple functions
- Multiply, divide, square, square root, RMS-to-DC conversion, AGC and modulate/demodulate
- Wide bandwidth – 4 MHz
- Signal-to-noise ratio – 94 dB

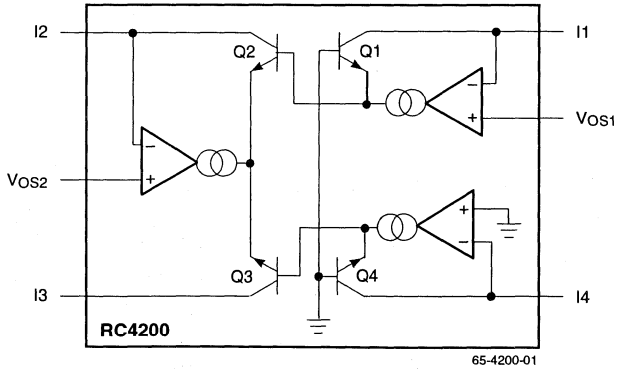
Description

The RC4200 analog multiplier has complete compensation for nonlinearity, the primary source of error and distortion. This multiplier also has three onboard operational amplifiers designed specifically for use in multiplier logging circuits. These amplifiers are frequency compensated for optimum AC response in a logging circuit, the heart of a multiplier, and can therefore provide superior AC response.

The RC4200 can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, two-quadrant division, square rooting, squaring and RMS conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well-designed monolithic chip provides a very high accuracy and a low temperature coefficient.

The RC4200 is ideal for use in low distortion audio modulation circuits, voltage-controlled active filters, and precision oscillators.

Block Diagram



Functional Description

The RC4200 multiplier is designed to multiply two input currents (I_1 and I_2) and to divide by a third input current (I_4). The output is also in the form of a current (I_3). A simplified circuit diagram is shown in the Block Diagram. The nominal relationship between the three inputs and the output is:

$$I_3 = \frac{I_1 I_2}{I_4} \quad (1)$$

The three input currents must be positive and restricted to a range of 1 µA to 1 mA. These currents go into the multiplier chip at op amp summing junctions which are nominally at zero volts. Therefore, an input voltage can be easily converted to an input current by a series resistor. Any number of currents may be summed at the inputs. Depending on the application, the output current can be converted to a voltage by an external op amp or used directly. This capabilty of combining input currents and voltages in various combinations provides great versatility in application.

Inside the multiplier chip, the three op amps make the collector currents of transistors Q1, Q2 and Q4 equal to their respective input currents (I_1, I_2, and I_4). These op amps are designed with current source outputs and are phase-compensated for optimum frequency response as a multiplier. Power drain of the op amps was minimized to prevent the introduction of undesired thermal gradients on the chip. The three op amps operate on a single supply voltage (nominally -15V) and total quiescent current drain is less than 4 mA. These special op amps provide significantly improved performance in comparison to 741-type op amps.

The actual multiplication is done within the log-antilog configuration of the Q1-Q4 transistor array. These four transistors, with associated proprietary circuitry, were specially designed to precisely implement the relationship.

$$V_{BEN} = \frac{kT}{Q} \ln \frac{I_{CN}}{I_{SN}} \quad (2)$$

Previous multiplier designs have suffered from an additional undesired linear term in the above equation; the collector current times the emitter resistance. The I_{CR_E} term introduces a parabolic nonlinearity even with matched transistors. Raytheon has developed a unique and proprietary means of inherently compensating for this undesired I_{CR_E} term. Furthermore, this Raytheon developed circuit technique compensates linearity error over temperature changes. The nonlinearity versus temperature is significantly improved over earlier designs.

From equation (2) and by assuming equal transistor junction temperatures, summing base-to-emitter voltage drops around the transistor array yields:

$$\frac{KT}{q}\left[\ln\frac{I_1}{I_{S1}} = \ln\frac{I_2}{I_{S2}} - \ln\frac{I_3}{I_{S3}} - \ln\frac{I_4}{I_{S4}}\right] = 0 \quad (3)$$

This equation reduces to:

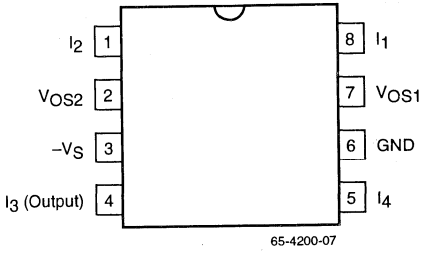
$$\frac{I_1 I_2}{I_3 I_4} = \frac{I_{S1} I_{S2}}{I_{S3} I_{S4}} \quad (4)$$

The rate of reverse saturation current $I_{S1}I_{S2}/I_{S3}I_{S4}$, depends on the transistor matching. In a monolithic multiplier this matching is easily achieved and the rate is very close to unity, typically 1.0±1%. The final result is the desired relationship:

$$I_3 = \frac{I_1 I_2}{I_4} \quad (5)$$

The inherent linearity and gain stability combined with low cost and versatility makes this new circuit ideal for a wide range of nonlinear functions.

Pin Assignments



65-4200-07

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage[1]			-22	V
Input Current			-5	mA
Storage Temperature Range	RM4200/4200A	-65	+150	°C
	RC4200/4200A	-55	+125	°C
Operating Temperature Range	RM4200/4200A	-55	+125	°C
	RC4200/4200A	0	+70	°C

Notes:
1. For a supply voltage greater than -22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

(Still air, soldered into PC board)

	8-Lead Plastic DIP	8-Lead Ceramic DIP
Max. Junction Temp.	+125°C	+175°C
Max. P_D T_A<50°C	468 mW	833 mW
Therm. Res θ_{JC}	—	45°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W
For T_A > 50°C Derate at	6.25 mW/°C	8.33 mW/°C

Electrical Characteristics

(Over operating temperature range, V_S = -15V unless otherwise noted)

		4200A			4200			
Parameters	**Test Conditions**	**Min**	**Typ**	**Max.**	**Min**	**Typ**	**Max**	**Units**
Total Error as Multiplier	TA = +25°C							
Untrimmed	Note 1			±2.0			±3.0	%
With External Trim			±0.2			±0.2		%
Versus Temperature			±0.005			±0.005		%/°C
Versus Supply (-9 to -18V)			±0.1			±0.1		%/V
Nonlinearity	50μA ≤ $I_{1,2,4}$ ≤ 250 μA, T_A = +25°C (Note 2)			±0.1			±0.3	%
Input Current Range (I_1,I_2 and I_4)		1.0		1000	1.0		1000	μA
Input Offset Voltage	$I_1 = I_2 = I_4$ = 150 μA T_A = +25°C			±5.0			±10	mV
Input Bias Current	$I_1 = I_2 = I_4$ = 150 μA T_A = +25°C			300			500	nA
Average Input Offset Voltage Drift	$I_1 = I_2 = I_4$ = 150 μA			±50			±100	μV/°C
Output Current Range (I_3)	Note 3	1.0		1000	1.0		1000	μA

Electrical Characteristics (continued)

(Over operating temperature range, V_S = -15V unless otherwise noted)

Parameters	Test Conditions	4200A			4200			Units
		Min	Typ	Max.	Min	Typ	Max	
Frequency Response, -3dB point			4.0			4.0		MHz
Supply Voltage		-18	-15	-9.0	-18	-15	-9.0	V
Supply Current	$I_1 = I_2 = I_4 = 150\ \mu A$ $T_A = +25°C$			4.0			4.0	mA

Notes:

1. Refer to Figure 6 for example.
2. The input circuits tend to become unstable at I_1, I_2, I_4 < 50 µA and linearity decreases when I_1, I_2, I_4 > 250 µA (eq. @ $I_1 = I_2$ = 500 µA, nonlinearity error ≈ 0.5%).
3. These specifications apply with output (I_3) connected to an op amp summing junction. If desired, the output (I_3) at pin (4) can be used to drive a resistive load directly. The resistive load should be less than 700Ω and must be pulled up to a positive supply such that the voltage on pin (4) stays within a range of 0 to +5V.

Basic Circuits

Current Multiplier/ Divider

The basic design criteria for all circuit configurations using the 4200 multiplier is contained in equation (1): i.e.,

$$I_3 = \frac{I_1 I_2}{I_4}$$

The current-product-balance equation restates this as:

$$I_1 I_2 = I_3 I_4 \quad (6)$$

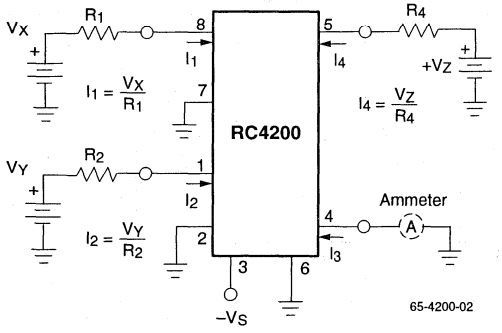


Figure 1.

Dynamic Range and Stability

The precision dynamic range for the 4200 is from +50 µA to +250 µA inputs for I_1, I_2 and I_4. Stability and accuracy degrade if this range is exceeded.

To improve the stability for input currents less than 50 µA, filter circuits ($R_S C_S$) are added to each input (see Figure 2).

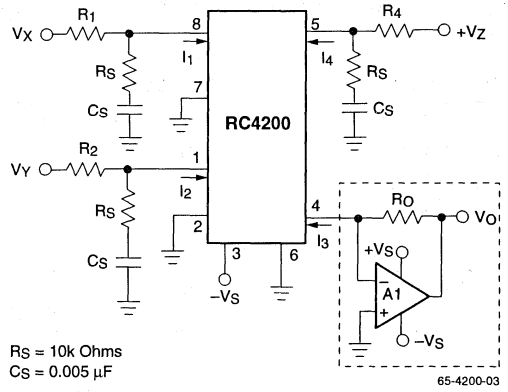
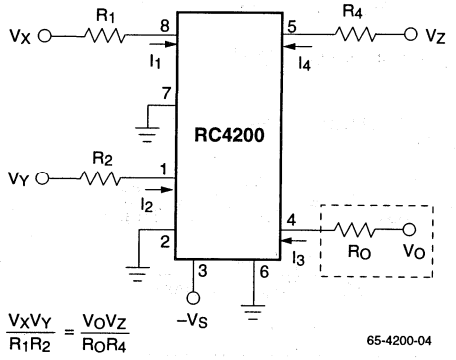


Figure 2.

Amplifier A1 is used to convert the I_3 current to an output voltage.

Multiplier: Vz = constant ≠ 0
Divider: Vy = constant ≠ 0

Voltage Multiplier/Divider



$$\frac{V_X V_Y}{R_1 R_2} = \frac{V_O V_Z}{R_O R_4}$$

Figure 3.

Solving for $V_0 = \dfrac{V_X V_Y}{V_Z} \dfrac{R_0 R_4}{R_1 R_2}$

For a multiplier circuit $V_Z = V_R$ = constant

Therefore: $V_0 = V_X V_Y K$ where $K = \dfrac{R_0 R_4}{V_R R_1 R_2}$

For a divider circuit $V_Y = V_R$ = constant

Therefore: $V_0 = \dfrac{V_X}{V_Z} K$ where $K = \dfrac{V_R R_0 R_4}{R_1 R_2}$

Extended Range

The input and output voltage ranges can be extended to include 0 and negative voltage signals by adding bias currents. The RSCS filter circuits are eliminated when the input and biasing resistors are selected to limit the respective currents to 50 µA min. and 250 µA max.

Extended Range Multiplier

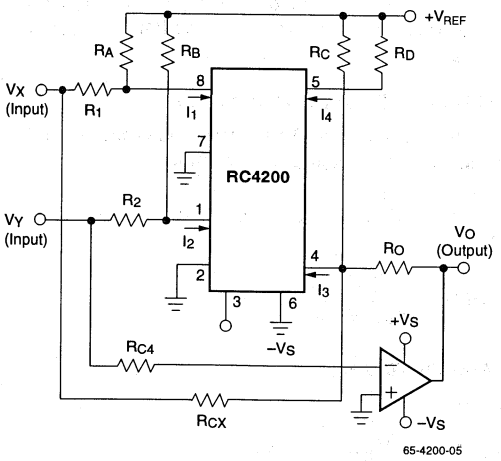


Figure 4.

Resistors R_a and R_b extend the range of the V_X and V_Y inputs by picking values such that:

$$I_1(\text{min.}) = \frac{V_X(\text{min.})}{R_1} + \frac{V_{REF}}{R_a} = 50\ \mu A,$$

$$\text{and } I_1(\text{max.}) = \frac{V_X(\text{max.})}{R_1} + \frac{V_{REF}}{R_a} = 250\ \mu A,$$

$$\text{also } I_2(\text{min.}) = \frac{V_Y(\text{min.})}{R_2} + \frac{V_{REF}}{R_b} = 50\ \mu A,$$

$$\text{and } I_2(\text{max.}) = \frac{V_Y(\text{max.})}{R_2} + \frac{V_{REF}}{R_b} = 250\ \mu A.$$

Resistor R_C supplies bias current for I_3 which allows the output to go negative.

Resistors R_{CX} and R_{CY} permit equation (6) to balance, ie.:

$$\left(\frac{V_X}{R_1} + \frac{V_{REF}}{R_a}\right)\left(\frac{V_Y}{R_2} + \frac{V_{REF}}{R_b}\right) = \left(\frac{V_0}{R_0} + \frac{V_{REF}}{R_C} + \frac{V_X}{R_{CX}} + \frac{V_Y}{R_{CY}}\right)\left(\frac{V_{REF}}{R_D}\right)$$

$$\frac{V_Y V_X}{R_1 R_2} + \frac{V_X V_{REF}}{R_1 R_b} + \frac{V_Y V_{REF}}{R_2 R_a} + \frac{V_{REF}}{R_a R_b} =$$

$$\frac{V_0 V_{REF}}{R_0 R_d} + \frac{V_X V_{REF}}{R_{cx} R_d} + \frac{V_Y V_{REF}}{R_{CY} R_d} + \frac{V_{REF}^2}{R_c R_d}$$

Cross-Product Cancellation

Cross-products are a result of ths $V_X V_R$ and $V_Y V_R$ terms. To the extend that $R_1 R_b = R_{CX} R_D$, and $R_2 R_a = R_{CY} R_d$ cross-product cancellation will occur.

Arithmetic Offset Cancellation

The offset caused by the V_{REF}^2 term will cancel to the extent that $R_a R_b = R_0 R_d$, and the result is:

$$\frac{V_Y V_X}{R_1 R_2} = \frac{V_0 V_{REF}}{R_0 R_d} \text{ or } V_0 = V_X V_Y K$$

$$\text{where } K = \frac{R_0 R_d}{V_{REF} R_1 R_2}$$

Resistor Values

Inputs:

$$V_X(\text{min.}) \le V_X \le V_X(\text{max.})$$

$$\Delta V_X = V_X(\text{max.}) - V_X(\text{min.})$$

$$V_Y(\text{min.}) \le V_Y \le V_Y(\text{max.})$$

$$\Delta V_Y = V_Y(\text{max.}) = V_Y(\text{min.})$$

$$V_{REF} = \text{Constant (+7V to +18V)}$$

$$K = \frac{V_0}{V_X V_Y} \text{ (Design Requirements)}$$

$$R_1 = \frac{\Delta V_X}{200\mu A}, R_2 = \frac{\Delta V_Y}{200\mu A}, R_d = \frac{V_{REF}}{250\mu A}$$

$$R_a = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_X - 200\mu A\ V_X(\text{max.})}$$

$$R_b = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_Y - 200\mu A\ V_Y(\text{max.})}$$

$$R_c = \frac{R_a R_b}{R_d}, R_{CX} = \frac{R_1 R_b}{R_d}, R_{cy} = \frac{R_2 R_a}{R_d}$$

$$R_0 = \frac{\Delta V_X \Delta V_Y K}{160\mu A}$$

Multiplying Circuit Offset Adjust

$10K \leq R_5 = R_9 = R_{16} \leq 50K$

$R_7 = R_{11} = R_{14}, = 100\Omega$

$R_6 = R_{10} = 100\Omega\ (V_S/0.05)$

$R_{15} = 100\Omega\ (V_S/0.10)$

$R_8 = R_1 \,||\, R_a$

$R_{12} = R_2 \,||\, R_b$

$R_{13} = R_0 \,||\, R_C \,||\, R_{CX} \,||\, R_{CY}$

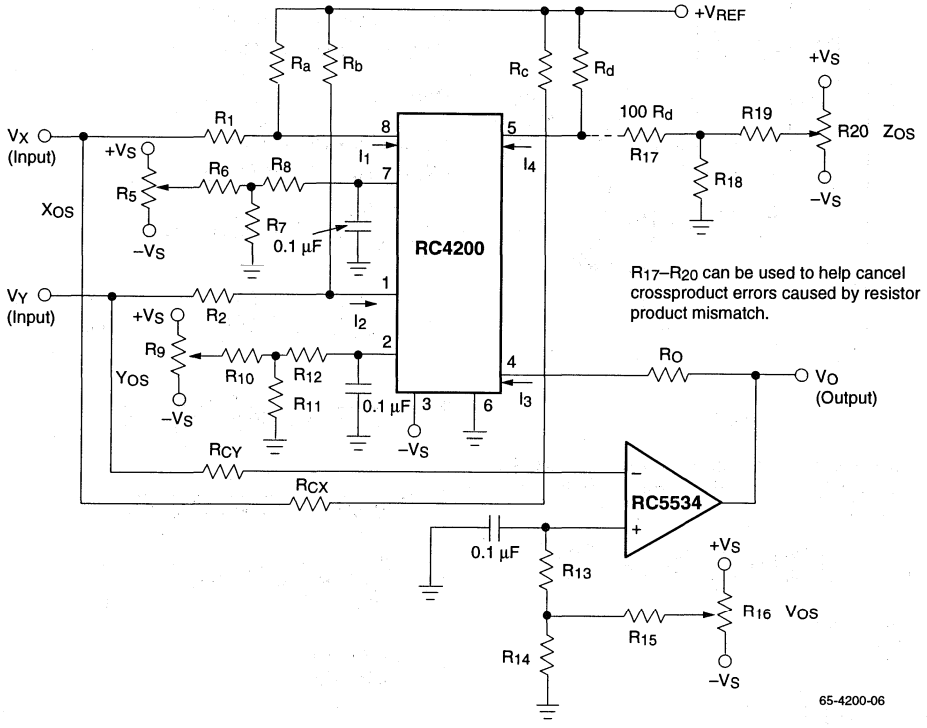


Figure 5.

Procedure

1. Set all trimmer pots to 0V on the wiper.

2. Connect V_X input to ground. Put in a full scale square wave on V_Y input. Adjust $X_{OS}(R_5)$ for no square wave on V_0 output (adjust for 0 feedthrough).

3. Connect V_Y input to ground. Put in a full scale square wave on V_X input. Adjust $Y_{OS}(R_9)$ for no square wave on V_0 output (adjust for 0 feedthrough).

4. Connect V_X and V_Y to ground. Adjust $V_{OS}(R_{16})$ for 0V on V_0 output.

Extended Range Divider

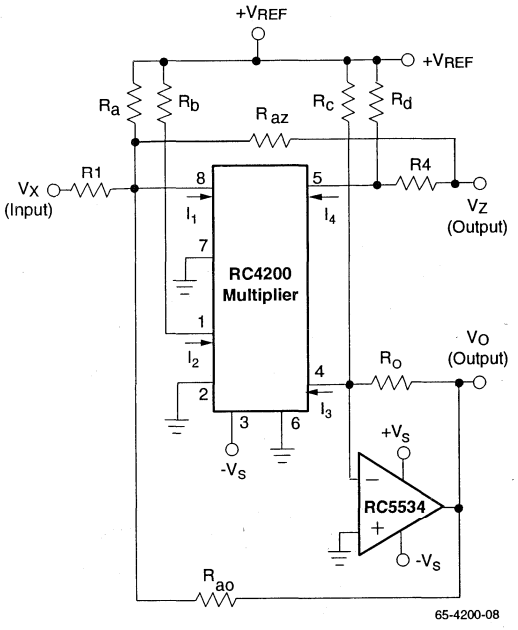


Figure 6.

As with the extended range multiplier, resistors R_{az} and R_{ao} are added to cancel the cross-product error caused by the biasing resistors, i.e.

$$\left(\frac{V_X}{R_1}+\frac{V_0}{R_{ao}}+\frac{V_Z}{R_{az}}+\frac{V_{REF}}{R_a}\right)\left(\frac{V_{REF}}{R_b}\right)=\left(\frac{V_0}{R_0}+\frac{V_{REF}}{R_C}\right)\left(\frac{V_Z}{R_4}+\frac{V_{REF}}{R_D}\right)$$

$$\frac{V_XV_{REF}}{R_1R_b}+\frac{V_0V_{REF}}{R_{ao}R_b}+\frac{V_ZV_{REF}}{R_{az}R_b}+\frac{V_{REF}^2}{R_aR_b}=$$

$$\frac{V_0V_Z}{R_0R_4}+\frac{V_0V_{REF}}{R_0R_d}+\frac{V_ZV_{REF}}{R_4R_c}+\frac{V_{REF}^2}{R_cR_d}$$

To cancel cross-product and arithmetic offset:

$R_{ao}R_b = R_0R_d$, $R_{az}R_b = R_4R_c$ and $R_aR_b = R_cR_d$

and the result is:

$$\frac{V_XV_{REF}}{R_1R_b}=\frac{V_0V_Z}{R_0R_4} \quad \text{or} \quad V_0=\frac{V_X}{V_ZK}$$

where $K=\dfrac{V_{REF}R_0R_4}{R_1R_b}$

Note: It is necessary to match the above resistor cross-products to within the amount of error tolerable in the output offset, i.e., with a 10V F.S. output, 0.1% resistor cross-product match will give 0.1% x 10V. untrimmable output offset voltage.

Resistor Values

Inputs:

$V_X(\text{min.}) \le V_X \le V_X(\text{max.})$

$\Delta V_X = V_X(\text{max.}) = V_X(\text{min.})$

$V_Z(\text{min.}) \le V_Z \le V_Z(\text{max.})$

$\Delta V_Z = V_Z(\text{max.}) = V_Z(\text{min.})$

V_{REF} = Constant (+7V to +18V)

Outputs:

$V_0(\text{min.}) \le V_0 \le V_0(\text{max.})$

$\Delta V_0 = V_0(\text{max.}) = V_0(\text{min.})$

$$K=\frac{V_0V_Z}{V_X}\text{(Design Requirement)}$$

$$R_0=\frac{\Delta V_0}{750\mu A},\ R_b=\frac{\Delta V_{REF}}{250\mu A},\ R_4=\frac{\Delta V_Z}{200\mu A}$$

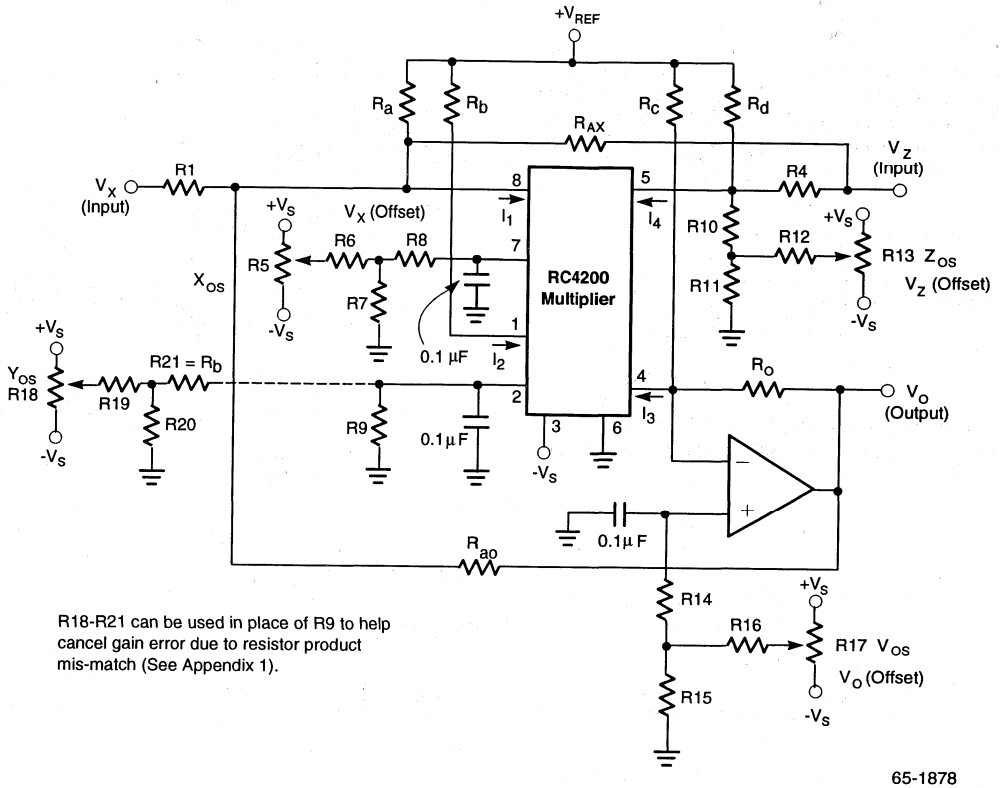
$$R_c=\frac{\Delta V_0V_{REF}}{750\mu A\Delta V_0-700\mu A\ V_0(\text{max.})}$$

$$R_d=\frac{\Delta V_XV_{REF}}{250\mu A\Delta V_Z-200\mu A\ V_Z(\text{max.})}$$

$$R_a=\frac{R_cR_d}{R_b},\ R_{az}=\frac{R_cR_4}{R_b},\ R_{ao}=\frac{R_0R_d}{R_b}$$

$$R_1=\frac{\Delta V_0\Delta V_Z}{600\mu AK}$$

Divider Circuit with Offset Adjustment



R18-R21 can be used in place of R9 to help cancel gain error due to resistor product mis-match (See Appendix 1).

65-1878

General

$10K \le R_5 = R_{13} = R_{17} \le 50K$
$R_7 + R_8 \approx R_1 \,||\, R_a \,||\, R_{az} \,||\, R_{ao}$
$R_6 \approx R_7 (V_S/0.05)$
$R_9 = R_b$
$R_{10} \approx 100 \times R_4$
$R_{11} = 20K$
$R_{12} = 100K$
$R_{14} + R_{15} \approx R_0 \,||\, R_c$
$R_{16} \approx R_{15} (V_S/0.10)$

Example: Two-Quad Divider

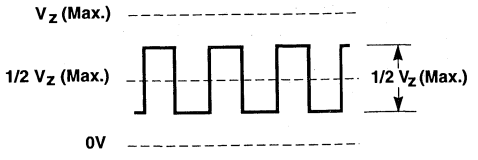
$V_0 = K(V_X/V_Z)$, K = k, $V_{REF} = +V_S = +15V$
$-10 \le V_X \le +10$, therefore $\Delta V_X = 20$
$0 \le V_Z \le +10$, therefore $\Delta V_Z = 20$
$-10 \le V_0 \le +10$, therefore $\Delta V_0 = 20$

$R_0 = 26.7K$	$R_1 = 333K$
$R_b = 60K$	$R_5, R_{13}, R_{17} = 10K$
$R_4 = 50K$	$R_7, R_{15} = 1K$
$R_c = 37.5K$	$R_8, R_{11} = 20K$
$R_d = 300K$	$R_6, R_9, R_{16} = 300K$
$R_a = 187.5K$	$R_{10} = 4.7M$
$R_{az} = 31.25$	$R_{12} = 100K$
$R_{ao} = 133K$	

Figure 7.

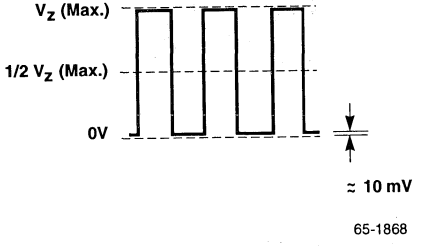
Divider Circuit Offset Adjustment Procedure

1. Set each trimmer pot to 0V on the wiper.
2. Connect V_X (input) to ground. Put a DC voltage of approximatey 1/2 V_Z (max.) DC on the V_Z (input) with an AC (squarewave is easiest) voltage of 1/2 V_Z (max.) peak-to-peak superimposed on it. Adjust X_{OS} (R5) for zero feedthrough. (No AC at V_0)



3. Connect V_X (input) to V_Z (input) and put in the 1/2 V_Z(max.) DC with an AC of approximately 20 mV less than V_Z(max.).

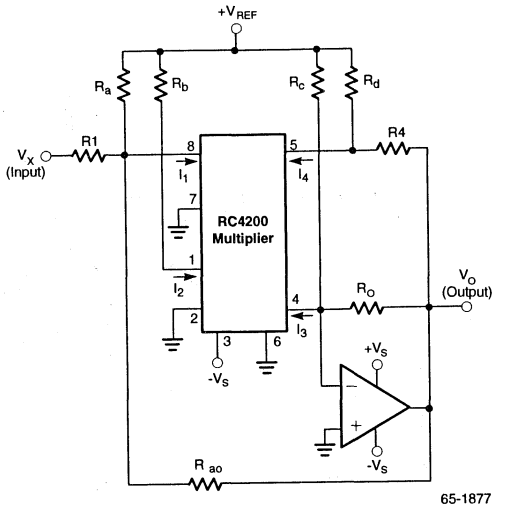
   Adjust Z_{OS} (R_{13}) for zero feedthrough.



4. Return V_X (Input) to ground and connect V_Z(max.) DC on V_Z(input). Adjust output V_{OS}(R17) for V_O = 0V_O
5. Connect V_X (input) to V_Z (input) and and in V_Z (max.) DC. (The output will equal K.) Decrease the input slowly until the output (V_0 - K) deviates beyond the desired accuracy. Adjust Z_{OS} to bring it back into tolerance and return to Step 4. Continue steps 4 and 5 until V_Z reduces to the lowest value desired.

Note: As the input to V_X and V_Z gets closer to zero (an illegal state) the system noise will predominate so much that an integrating voltmeter will be very helpful.

Square Root CFrcult $V_0 = N\sqrt{V_X}$



$$\frac{V_X V_{REF}}{R_1 R_b} + \frac{V_{REF}^2}{R_a R_b} + \frac{V_0 V_{REF}}{R_{ao} R_b} = \frac{V_0^2}{R_0 R_4} + \frac{V_0 V_{REF}}{R_c R_4} + \frac{V_0 V_{REF}}{R_0 R_d} + \frac{V_{REF}^2}{R_c R_d}$$

If $R_a R_b = R_c R_d$ and $R_{ao} R_b R_0 R_d + R_{ao} R_b R_c R_4 = R_c R_d R_0 R_4$

Then $\frac{V_0^2}{R_0 R_4} = \frac{V_X V_{REF}}{R_1 R_b}$ or $V_0^2 = V_X K$ where $K = \frac{V_{REF} R_0 R_4}{R_1 R_b}$

and $V_0 = N\sqrt{V_X}$ where $N = \sqrt{K}$

$0 \le V_X \le V_X$ (max.) and V_0 (max.) $= N\sqrt{V_X \text{ (max.)}}$

$N = \frac{V_0}{\sqrt{V_X}}$ (Design Requirements)

$R_1 = \frac{V_0 (\text{max.})^2}{74\mu A\, N^2}$

$R_a = R_d = \frac{V_{REF}}{50\mu A}$

$R_b = R_c = \frac{V_{REF}}{150\mu A}$

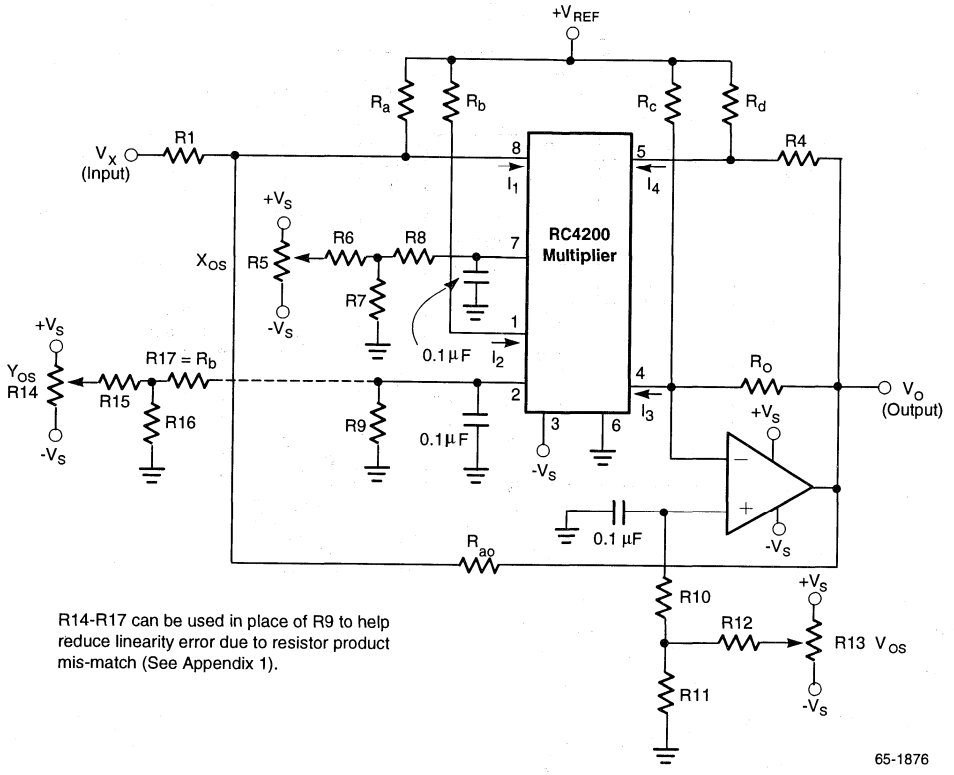
$R_4 = \frac{V_0 (\text{max.})}{50\mu A}$

$R_{ao} = \frac{V_0 (\text{max.})}{125\mu A}$

$R_0 = \frac{V_0 (\text{max.})}{225\mu A}$

Figure 8.

Square Root Circuit Offset Adjust



R14-R17 can be used in place of R9 to help reduce linearity error due to resistor product mis-match (See Appendix 1).

$10K \leq R_5 = R_{13} \leq 50K$

$R_7 = 100\Omega$

$R_6 = R_7 \frac{V_S}{0.05}$

$R_8 = R_1 \| R_a \| R_{ao}$

$R_9 = R_b$

$R_{10} = R_0 \| R_C$

$R_{11} = 100\Omega$

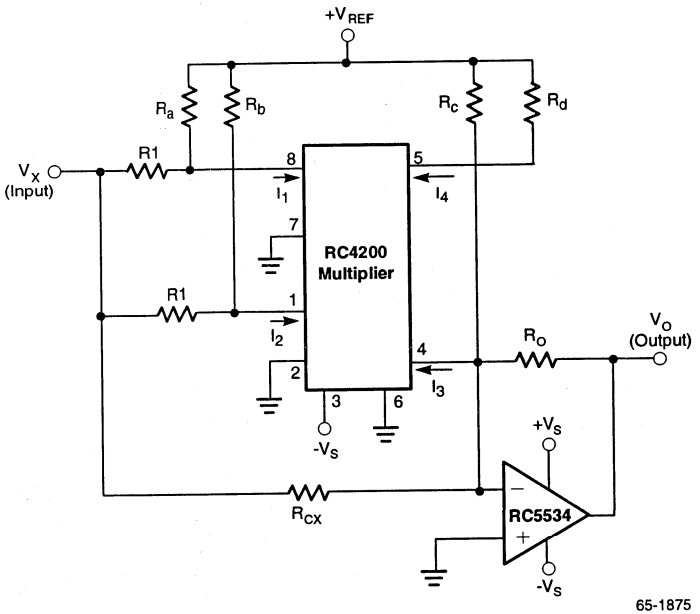
$R_{12} = R_{11} \frac{V_S}{0.1}$

Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale (0 to V_X(max.) squarewave on V_X input. Adjust X_{OS}(R5) for proper peak-to-peak amplitude on V_0 output. (Scaling adjust)
3. Connect V_X input to ground. Adjust V_{OS}(R13) for 0V on V_0 output.

Figure 9.

Squaring Circuits $V_0 = K V_X^2$



65-1875

$$\frac{V_X^2}{R_1^2} + \frac{2V_X V_{REF}}{R_1 R_a} + \frac{V_{REF}^2}{R_a^2} = \frac{V_0 V_{REF}}{R_0 R_d} + \frac{V_{REF}^2}{R_c R_d} + \frac{V_X V_{REF}}{R_c R_d}$$

if $R_a^2 = R_c R_d$ and $R_1 R_a = 2R_{CX} R_D$

then $\frac{V_0 V_{REF}}{R_0 R_d} = \frac{V_X^2}{R_1^2}$ or $V_0 = K V_X^2$ where $K = \frac{R_0 R_d}{V_{REF} R_1^2}$

$V_X(\text{min.}) \le V_X \le V_X(\text{max.})$ $\quad \Delta V_X = V_X(\text{max.}) - V_X(\text{min.})$

$$K = \frac{V_0}{V_X^2} \text{ (Design Requirement)}$$

$$R_1 = \frac{\Delta V_X}{200\mu A}$$

$$R_a = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_X - 200\mu A\ V_X(\text{max.})}$$

$$R_d = \frac{V_{REF}}{250\mu A}$$

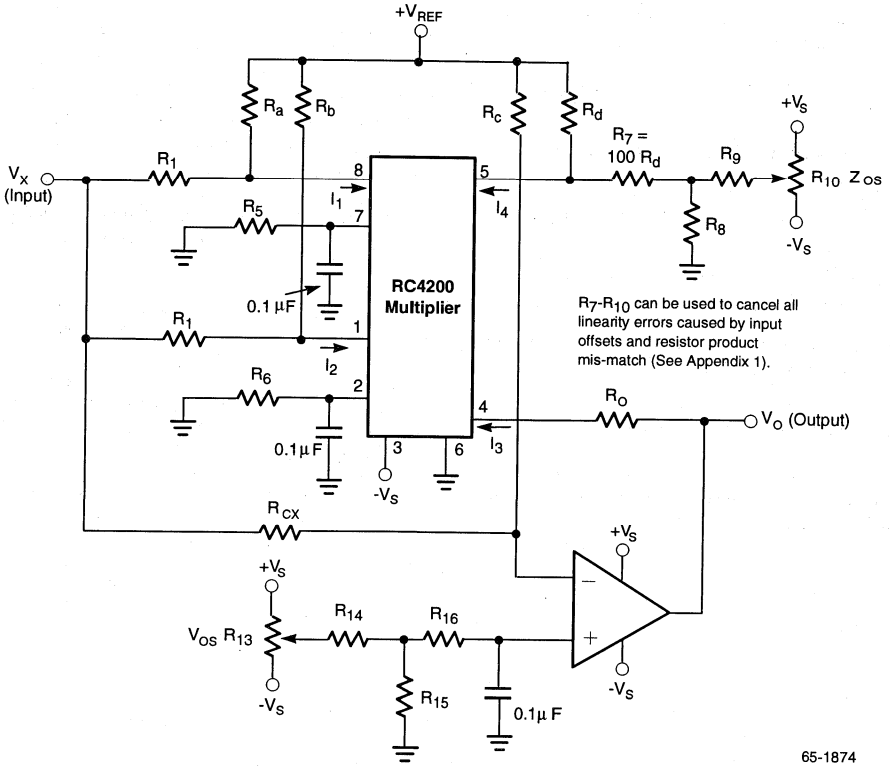
$$R_c = \frac{R_a^2}{R_d}$$

$$R_{cx} = \frac{R_1 R_a}{2R_d}$$

$$R_0 = \frac{\Delta V_X^2 K}{160\mu A}$$

Figure 10.

Squaring Circuits Offset Adjust



65-1874

$10K \leq R_{10} = R_{11} \leq 50K$

$R_8,\ R_{15} = 100\Omega$

$R_9,\ R_{14} = 100\Omega \frac{V_S}{0.1}$

$R_5,\ R_6 = R_1 \parallel R_a$

$R_{16} = R_0 \parallel R_c \parallel R_a$

Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale (±VX) squarewave on VX input. Adjust ZOS(R10) for uniform output.
3. Connect VX input to ground. Adjust VOS(R11) for 0V on V0 outputs.

Figure 11.

Appendix 1—System Errors

There are four types of accuracy errors which affect overall system performance. They are:

1. Nonimearity—Incremental deviation from absolute accuracy. (1)
2. Scaling Error—Linear deviation from absolute accuracy.
3. Output Offset—Constant deviation from absolute accuracy.
4. Feedthrough(2)—Cross-product errors caused by input offsets and external circuit limitations.

This nonlinearity error in the transfer function of the 4200 is ±0.1% max. (±0.03 max. for 4200A).

$$\text{i.e., } I_3 = \frac{I_1 I_2}{I_4} \pm 0.1\%\ \text{F.S.}^{(4)}$$

The other system errors are caused by voltage offsets on the inputs of the 4200 and can be as high as ±3.0% (±2.0% for 4200A).

$$\text{i.e., } V_0 = \frac{V_X V_Y}{V_Z}\frac{R_0 R_4}{R_1 R_2} \pm 3.0\%\ \text{F.S.}^{(3)\ (4)}$$

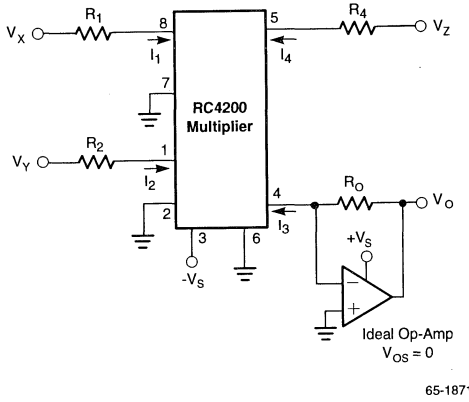


Figure 12.

Notes:

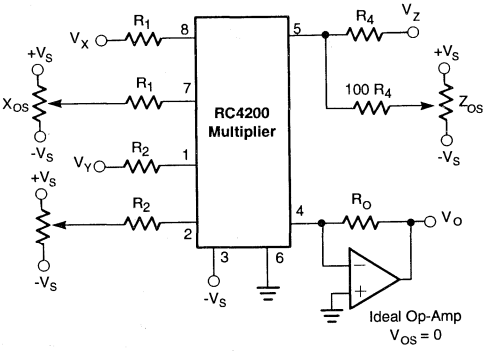
1. The input circuits tend to become unstable at I_1, I_2, $I_4 < 50$ µA and linearity decreases when I_1, I_2, $I_4 > 250$ µA (e.g., @ $I_1 = I_2 = 500$µA nonlinearity error ≈ 0.5%).
2. This section will not deal with feedthrough which is proportional to frequency of operation and caused by stray capacitance and/or bandwidth limitations. (refer to Figure 21.)
3. Not including resistor tolerance or output offset on the op amp.
4. For 50 µA ≤ I_1, I_2, I_4 ≤ 250 µA.

Errors Caused by Input Offsets

$$V_0 = \frac{R_0 R_4}{R_0 R_4}\left[\frac{V_X V_Y}{V_Z} \pm \frac{1}{V_Z}\underbrace{V_Y V_{OSX}} \pm \underbrace{V_X V_{OSY}} \pm \underbrace{V_0 V_{OSZ}} \pm \underbrace{V_{OSX} V_{OSY}}\right]$$

V_Y Feedthrough
V_X Feedthrough
Scaling Error
Output Offset Error

System errors can be greatly reduced by externally trimming the input offset voltages of the 4200. (±3.0% F.S. for 4200 and ±0.1% for 4200A.)



If $X_{OS} = X_{OSX}$, $Y_{OS} = Y_{OSY}$, $Z_{OS} = -V_{OSZ}$,

$$\text{then } V_O \frac{V_X V_Y}{V_Z}\frac{R_0 R_4}{R_1 R_2} \pm 0.3\%\ \text{F.S.}^{(3)}$$

Figure 13. RC4200 with Input Offset Adjustment

Extended Range Circuit Errors

The extended range configurations have a disadvantage in that additional accuracy errors may be introduced by resistor product mismatching.

Multiplier (Figure 6)

An error in resistor product matching will cause an equivalent feedthrough or output offset error:

1. $R_1R_b = R_CX R_d \pm \alpha$, V_X feedthrough ($V_Y = 0$) = $I\alpha V_X$
2. $R_2R_a = R_CY R_d \pm \beta$, V_Y feedthrough ($V_X = 0$) = $\pm\beta V_Y$
3. $R_aR_b = R_CR_d \pm \gamma$, V_0 offset ($V_X = V_Y = 0$) = $\pm\gamma V_{REF}$*

*Output offset errors can always be trimmed out with the output op amp offset adjust, VOS (R16).

Reducing Mismatch Errors (Figure 4)

You need not use .01% resistors to reduce resistor product mismatch errors. Here are a couple of ways to squeeze maximum accuracy out of the extended range multiplier (see Figure 4) using 1% resistors.

Method #1

V_X feedthrough, for example, occurs when $V_Y = 0$ and $V_{OSY} \neq 0$. This V_X feedthrough will equal $\pm V_X V_{OSY}$. Also, if $V_{OSZ} \neq 0$, there is a V_X feedthrough equal to $V_X V_{OSZ}$. A resistor-product error of α will cause a V_X feedthrough of $\pm\alpha V_X$. Likewise, V_Y feedthrough errors are: $\pm V_Y V_{OSX}$, $\pm V_Y V_{OSZ}$ and $\pm\beta V_Y$

Total feedthrough:
$\pm V_X V_{OSY} \pm V_Y V_{OSX} \pm\alpha V_X \pm\beta V_Y \pm(V_X + V_Y) V_{OSZ}$

By carefully abusing $X_{OS}(R_5)$, $Y_{OS}(R_9)$ and $Z_{OS}(R_{20})$ this equation can be made to very nearly equal zero and the feedthrough error will practically disappear.

A residual of set will probably remain which can be trimmed outwith $V_{OS}(R_{16})$ at the output of amp.

Method #2

Notice that the ratios of R_1R_b:$R_{CX}R_d$ and R_2R_a:$R_{CY}R_d$ are both dependent of R_d also that R_1, R_2, R_a and R_b are all functions of the maximum input requirements. By designing a multiplier for the same input ranges on both V_X and V_Y then $R_1 = R_2$, $R_{CX} = R_{CY}$ and $R_a = R_b$. (Note: it is acceptable to design a four quadrant multiplier and use only two quadrants of it.)

Select R_d to be 1% or 2% below (or above) the calculated value. This will cause α and β to both be positive (or negative) by nearly the same amount. Now the effective value of R_d can be trimmed with an offset adjustment $Z_{OS}(R_{20})$ on pin 5.

This technique will cause: 1) a slight gain error which can be compensated for with the R_0 value, and 2) an output of offset error that can be trimmed out with $V_{OS}(R_{16})$ on the output op amp.

Extended Range Divider (Figure 6)

The only cross-product error of interest is the V_Z feedthrough ($V_X = 0$ and $V_{OSX} \neq 0$) which is easily adjusted with $X_{OS}(R_5)$.

Resistor product mismatch will cause scaling errors (gain) that could be a problem for very low values of V_Z. Adjustments to $Y_{OS}(R_{18})$ can be made to improve the high gain accuracy.

Square Root and Squaring (Figures 9 and 11)

These circuits are functions of single variables so feedthrough, as such, is not a consideration. Cross product errors will effect incremental accuracy that can be corrected $Y_{OS}(R_{14})$ or $Z_{OS}(R_{10})$.

Appendix 2—Applications

Design Considerations for RMS-to-DC Circuits

Average Value

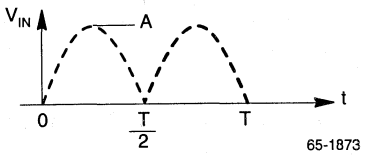
Consider $V_{in} = A\sin\omega\tau$. By definition,

$$V_{AG} = \int_0^{\frac{T}{2}} V_{IN}\,dt$$

Where T = Period

$\omega = 2\pi f$

$$= \frac{2\pi}{T}$$



65-1873

$$V_{AG} = \frac{2}{T}\int_0^{\frac{T}{2}} A\sin\omega t\,dt$$

$$= \frac{2A}{T}\left[-\frac{1}{\omega}\cos\omega t\right]_0^{\frac{T}{2}}$$

$$= \frac{2A}{2\pi}\left[-\cos(\pi) + \cos(0)\right]$$

Average Value of $A\sin\omega t$ is $\frac{2}{\pi}A$

RMS Value

Again, consider $V_{IN} = A\sin\omega t$

$$V_{rms} = \sqrt{V_{AVG}} = \sqrt{\frac{1}{T}\int_0^T [V_{IN}]^2 dt}$$

V_{rms} for $A\sin\omega t dt$:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T A^2\sin^2\omega t\,dt}$$

$$V_{rms} = \sqrt{\frac{A^2}{T}\int_0^T \left[\frac{1}{2} - \frac{1}{2}\cos 2\cos 2\,\omega t\right]dt}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}\left[\frac{T}{2} - \frac{1}{4\omega}\sin 2\,\omega t\right]_0^T}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}\left[\frac{T}{2}\right]}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}}$$

therefore, the rms value of $A\sin\omega t$ becomes:

$$V_{rms} = \frac{A}{\sqrt{2}}$$

RMS Value for Rectified Sine Waves

Consider $V_{in} = |A \sin \omega t|$, a rectified wave. To solve, integrate of each half cycle.

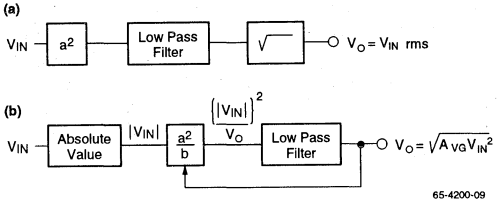
i.e. $\frac{1}{T}\int_0^T V_{in}^2\,dt =$

$$\frac{1}{T}\left[\int_0^{\frac{T}{2}} A^2\sin^2\omega t\,dt + \int_{\frac{T}{2}}^T (-A\sin\omega t)^2 dt\right]$$

This is the same as $\frac{1}{1}\int_0^T A^2\sin^2\omega t\,dt$

so, $|A\sin\omega t|_{rms} = A\sin\omega t_{rms}$

Practical Consideration: $|A\sin\omega t|$ has high-order harmonics; $A\sin\omega t$ does not. Therefore, non-ideal integrators may cause different errors for two approaches.



65-4200-09

$$\text{Avg}\left[\frac{V_{IN}^2}{V_0}\right] = V_0$$

implies $V_0 = \sqrt{\text{Avg}(|V_{IN}^2|)}$

$$V_0 = \sqrt{\text{Avg}\ V_{IN}^2}$$

Figure 14.

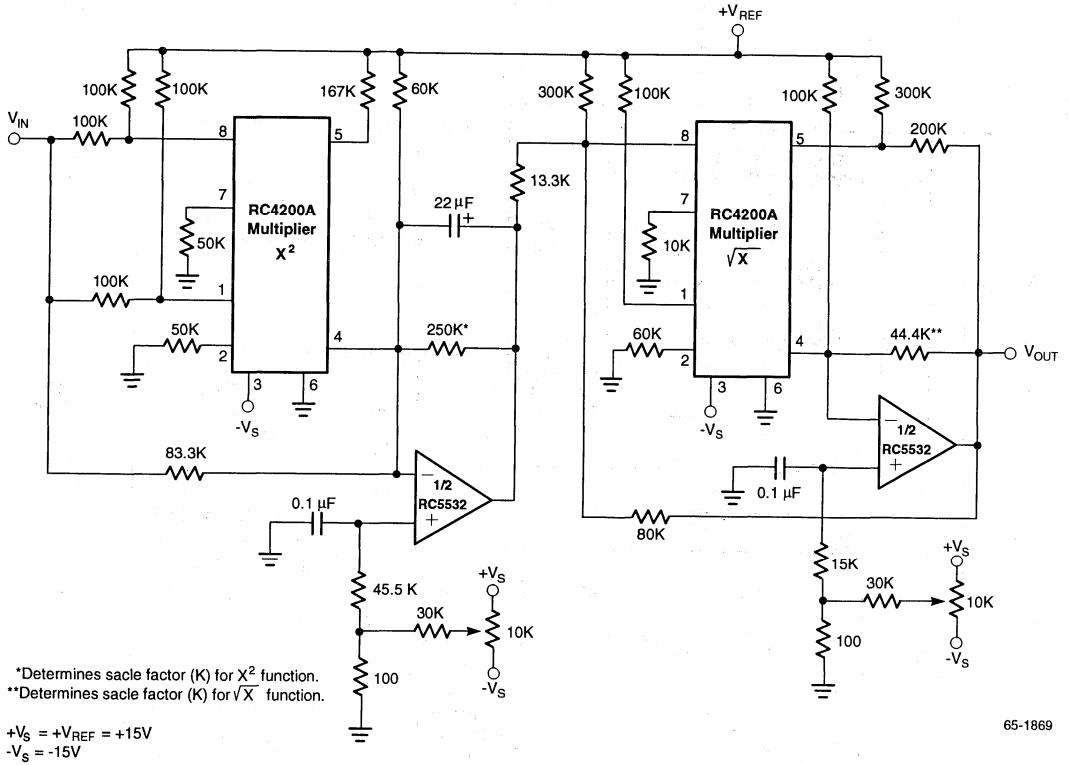


Figure 15. RMS to DC Converter $V_{OUT}=\sqrt{V_{IN}^2}$

Amplitude Modulator with A.G.C. (Figure 16)

In many AC modulator applications, unwanted output modulation is caused by variations in carrier input amplitude. The versatility of the RC4200 multiplier can be utilizes to eliminate this undesired fluctuation. The extended range multiplier circuit (Figure 4) shows an output amplitude inversely proportional to the reference voltage V_{REF}.

$$\text{i.e., } V_0 = \frac{V_X V_Y}{V_{REF}} \frac{R_0 R_d}{R_1 R_2}$$

By making V_{REF} proportional to V_Y (where V_Y is the carrier input) such that:

$$V_{REF} = V_H = \int (|V_Y|)$$

Then the denominator becomes a variable value that automatically provides constant gain, such that the modulating input (V_X) modulates the carrier (V_Y) with a fixed scale factor even though the carrier varies in amplitude.

If V_H is made proportional to the average value of Asinωt (i.e., 2A/π) and scaled by a value of π/2 then:

$V_H=A$

and if: V_X = Modulating input (V_M)

and: V_Y Carrier input (Asinωt)

Then: $V_0 = K V_M \sin\omega t$ where $K = \frac{R_0 R_d}{R_1 R_2}$

The resistor scaling is determined by the dynamic range of the carrier variation and modulating input.

The resistor values are solved, as with the other extended range circuits, in terms of the input voltages.

Input voltages:

Modulation voltage (V_M): $0 \le V_M \le V_X$(max.)

Carrier (V_Y): $V_Y = A\sin\omega t$

Carrier amplitude fluctuation (ΔA):

$A(\text{min.}) \sin t \le V_Y \le A(\text{max.}) \sin\Omega\omega t$

Dynamic Range (N): A(max.)/A(min.),

A(max.) = V_H(max.) and A(min.) = V_H(min.)

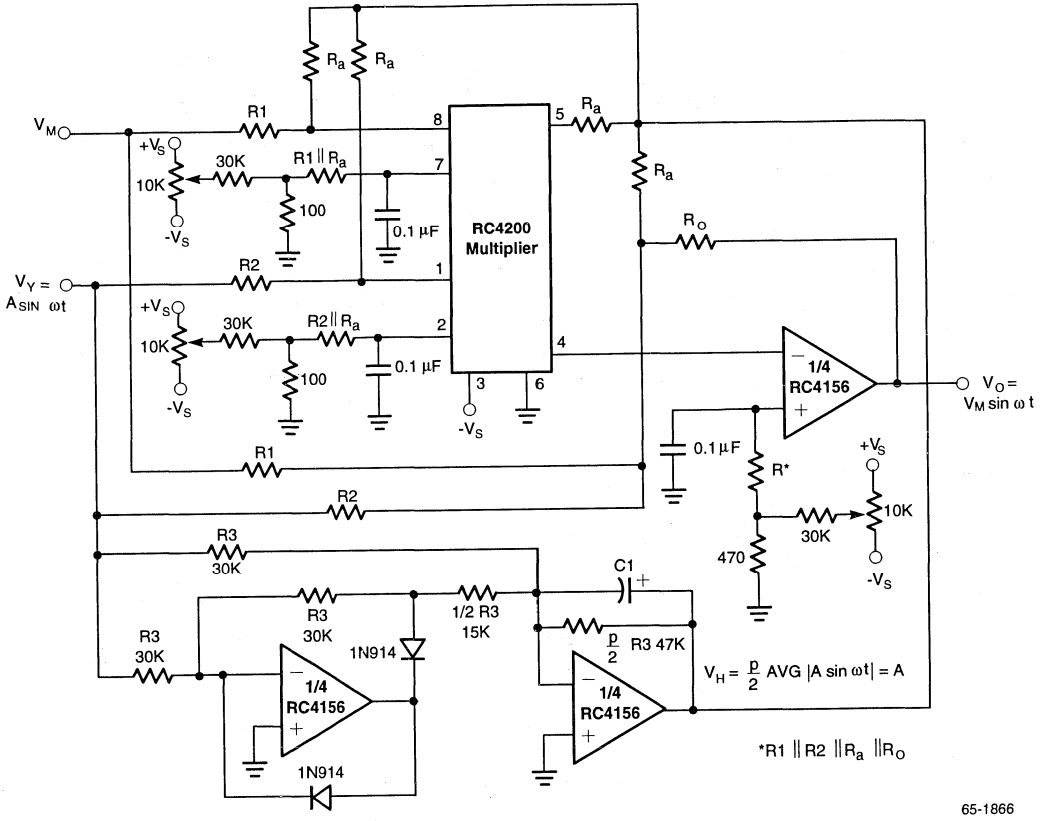


Figure 16. Amplitude Modulator with A.G.C.

The maximum and minimum values for I_1 and I_2 lead to:

$$I_1(\text{max.}) = \frac{V_X(\text{max.})}{R_1} + \frac{V_H(\text{max.})}{R_a} = 250\mu A$$

$$I_1(\text{min.}) = \frac{V_H(\text{min.})}{R_a} = 50\mu A \; V_M(\text{min.}) = 0$$

$$I_2(\text{max.}) = \frac{A(\text{max.})}{R_2} + \frac{V_H(\text{max.})}{R_a} = 250\mu A$$

$$I_2(\text{min.}) = \frac{V_H(\text{min.})}{R_a} = 50\mu A$$

For a dynamic range of N, where

$$N = \frac{A(\text{max.})}{A(\text{min.})} < 5,$$

These equations combine to yield:

$$R_1 = \frac{V_X(\text{max.})}{(5-N)\,50\mu A}, \; R2\frac{A(\text{max.})}{(5-N)\,50\mu A},$$

$$R_a = \frac{A(\text{min.})}{50\mu A} \text{ and } R_O = K\frac{R_1 R_2}{R_a},$$

Example #1

$V_Y = A\sin\omega t$ $2.5V \le A \le 10V$, therefore N = 4
$0V \le V_M \le 10V$, therefore $V_X(\text{max.}) = 10V$
K = 1, therefore $V_O = V_M \sin\omega t$

$$R_1 = \frac{V_X(\text{max.})}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

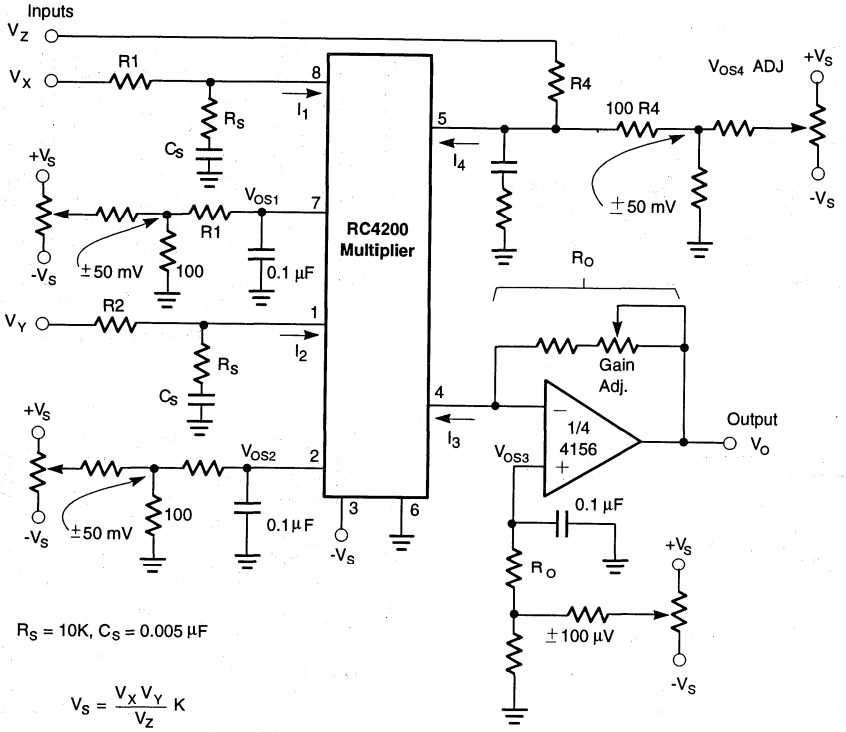
$$R_1 = \frac{A(\text{max.})}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

$$R_a = \frac{A(\text{min.})}{50\mu A} = \frac{2.5V}{50\mu A} = 50K$$

$$R_O = K\frac{R_1 R_2}{R_a} = 1\frac{200K \times 200K}{50K} = 800K$$

Example #2

$V_Y = A\sin\omega t$ $3 \le A \le 6$, therefore N = 2
$0V \le V_M \le 8V$, therefore $V_X(\text{max.}) = 8V$
K = .2, therefore $V_O = .2\, V_M \sin wt$
so:
$R_1 = 53.3K$, $R_2 = 40K$
$R_a = 60K$ and $R_O = 7.11K$



R_S = 10K, C_S = 0.005 µF

$$V_S = \frac{V_X V_Y}{V_Z} K$$

Where $K = \frac{R_O R4}{R1 R2}$

65-1867

Limited Range, First Quadrant Applications

The following circuit has the advantage that cross-product errors are due only to input offsets and nonlinearity error is sightly error is slightly less for lower input currents.

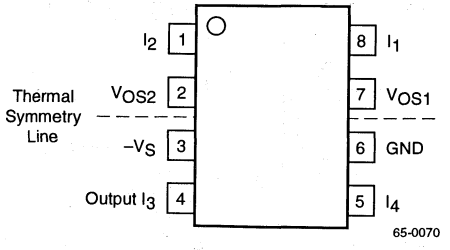
The circuit also has no standby current to add to the noise content, although the signal-to-noise ratio worsens at very low input currents (1-5 µA) due to the noise current of the input stages.

The R_SC_S filter circuits are added to each input to improve the stability for input currents below 50 µA.

Caution

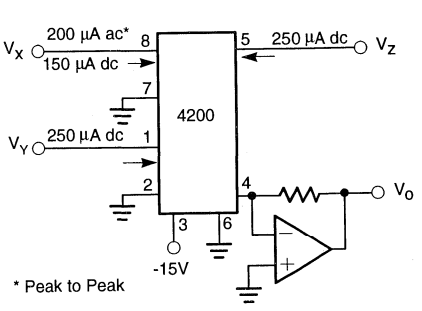
The bandpass drops off significantly for lower currents (<50 µA) and non-symmetrical rise and fall times can cause second harmonic distortion.

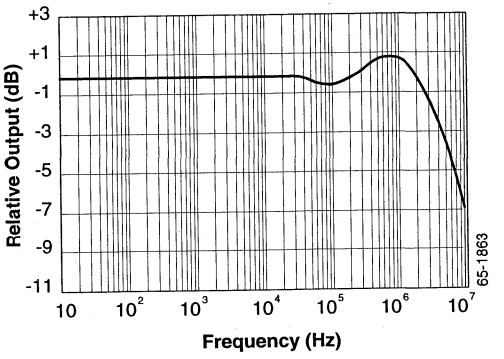
Thermal Symmetry

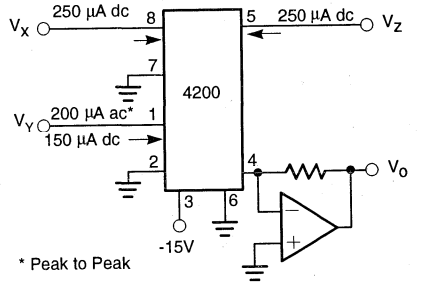


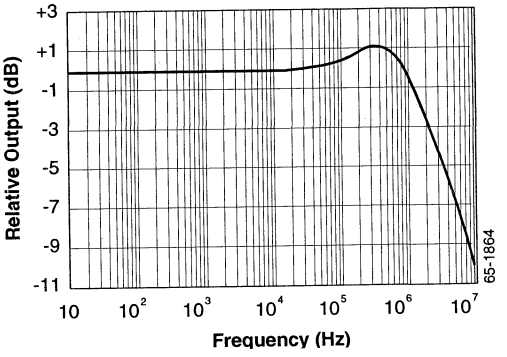
65-0070

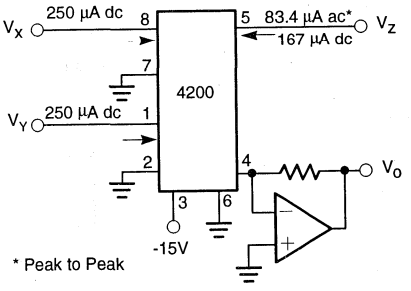
The scale factor is sensitive to temperature gradients across the chip in the lateral direction. Where possible, the package should be oriented such that forces generating temperature gradients are located physically on the line of thermal symmetry. This will minimize scale-factor error due to thermal gradients.


200 µA ac*
150 µA dc
V_X
8
5
250 µA dc
V_Z
7
4200
V_Y
250 µA dc
1
2
4
V_O
3
6
-15V
* Peak to Peak


+3
+1
-1
-3
-5
-7
-9
-11
Relative Output (dB)
10
10^2
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)
65-1863


250 µA dc
V_X
8
5
250 µA dc
V_Z
7
4200
V_Y
200 µA ac*
150 µA dc
1
2
4
V_O
3
6
-15V
* Peak to Peak


+3
+1
-1
-3
-5
-7
-9
-11
Relative Output (dB)
10
10^2
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)
65-1864


250 µA dc
V_X
8
5
83.4 µA ac*
167 µA dc
V_Z
7
4200
V_Y
250 µA dc
1
2
4
V_O
3
6
-15V
* Peak to Peak

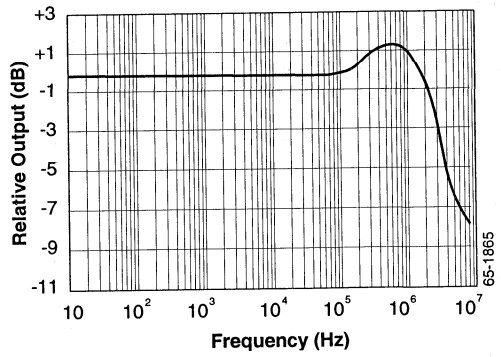

+3
+1
-1
-3
-5
-7
-9
-11
Relative Output (dB)
10
10^2
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)
65-1865

Figure 18.

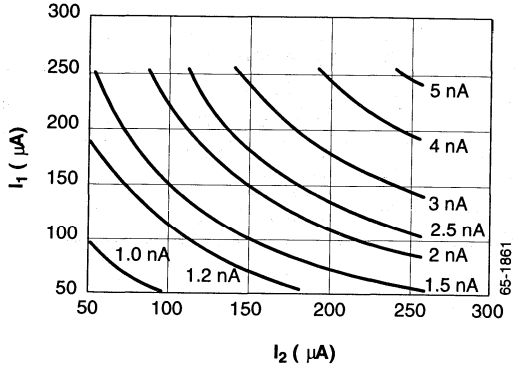


Figure 19a. Output Noise Current (I_3) vs. Input Currents (I_1, I_2) for I_4 = 250μA

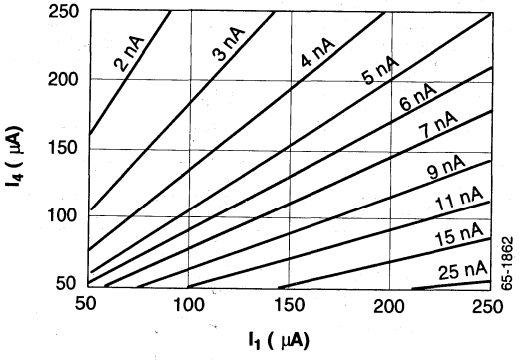


Figure 19b. Output Noise Current (I_3) vs. Input Currents (I_4, I_1) for I_2 = 250μA

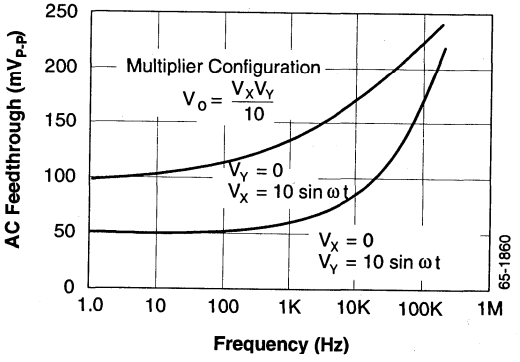


Figure 20. AC Feedthrough vs. Frequency

Ordering Information

Part Number	Package	Operating Temperature Range
RC4200N	N	0°C to +70°C
RC4200AN	N	0°C to +70°C
RM4200D	D	-55°C to +125°C
RM4200AD	D	-55°C to +125°C
RM4200AD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
N = 8-Lead Plastic DIP
D = 8-Lead Ceramic DIP

Section 2 – Broadcast Video

Digital Video Input

Digital Video Output

Video Signal Processing

A/D Converters

D/A Converters

TMC22071

Genlocking Video Digitizer

Features

- Fully integrated acquisition
- 3-channel video input multiplexer
- Two-stage video clamp
- Automatic gain adjustment
- Sync detection and separation
- Pixel and subpixel adjustment of HSYNC-to-Video timing
- Genlock to NTSC or PAL inputs
- Clock generation
- 8-bit video A/D converter
- Microprocessor interface
- Line-locked pixel rates
  - 12.27 MHz NTSC
  - 13.5 MHz NTSC or PAL
  - 14.75 MHz and 15.0 MHz PAL
- Direct interface to TMC22x9x encoders
- Built-in circuitry for crystal oscillator
- No tuning or external voltage reference required
- 68 lead PLCC package

Applications

- Frame grabber
- Digital VCR/VTR
- Desktop video

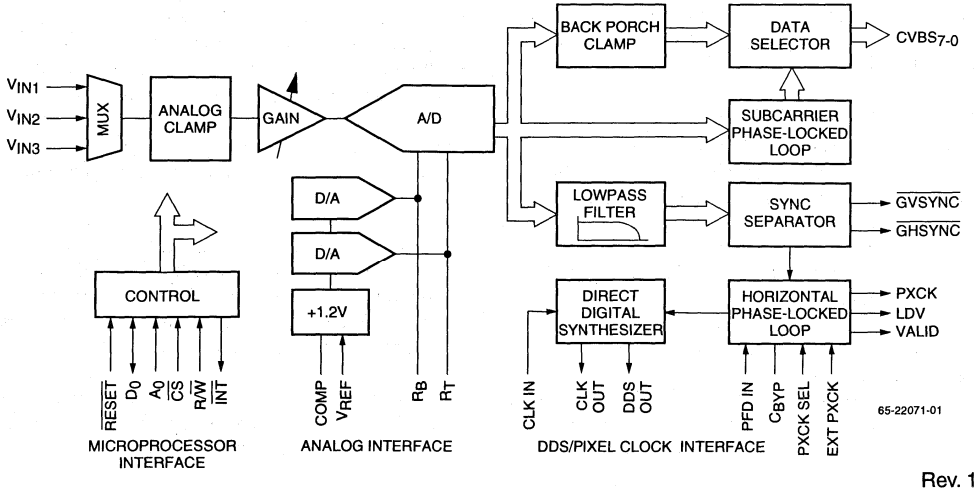
Description

The TMC22071 Genlocking Video Digitizer converts standard baseband composite NTSC or PAL video into 8-bit digital composite video data. It extracts horizontal and vertical sync signals and generates a pixel clock for the on-board 8-bit A/D converter and a 2x clock for the transfer of data to subsequent video processing or encoding with the TMC22x9x Digital Video Encoder family. It also measures the color subcarrier phase and frequency, and provides this data to the Encoder (for genlocked color NTSC or PAL encoding), or a frame buffer (for frame capture) over the digital composite video port.

The TMC22071 includes a three-channel video input multiplexer, analog clamp, variable gain amplifier, and digital back porch clamp. The on-board oscillator circuitry generates the clock from a 20 MHz crystal or the clock source may be an external oscillator. It is programmable over a microprocessor interface for NTSC or PAL operation. No external component changes and no production tuning or service adjustments are ever required.

The TMC22071 is fabricated in an advanced CMOS process, and is packaged in a 68-lead PLCC. Its performance is guaranteed from 0°C to 70°C.

Block Diagram



Rev. 1.1.1

Functional Description

The TMC22071 is a fully-integrated genlocking video A/D converter which digitizes NTSC or PAL baseband composite video under program control. It accepts video on three selectable input channels, adjusts gain, clamps to the back porch, and digitizes the video at a multiple of the horizontal line frequency. It extracts horizontal and vertical sync, measures the subcarrier frequency and phase (relative to the sampling clock), and provides this data along with digital composite video data over an 8-bit digital video port. Two sync outputs ($\overline{\text{GHSYNC}}$ and $\overline{\text{GVSYNC}}$) are also provided. It generates 1x (LDV) and 2x (PXCK) pixel clocks (PXCK) for data transfer. PXCK also serves as a master clock for the companion TMC22x9x Encoders.

Operating parameters are set up via a standard microprocessor port. Provisions have been made for internal or external voltage reference operation.

Timing

The TMC22071 operates from an internally-synthesized clock, PXCK, which runs at twice the pixel data rate. The nominal pixel rates may be set to 12.27 Mpps for NTSC, 13.5 Mpps for NTSC and PAL, and 14.75 Mpps or 15.0 Mpps for PAL operation.

Video Input

Three high-impedance video inputs are selected by an internal multiplexer under host processor control. The device accepts industry-standard video levels of 1.23 Volts (sync tip to peak color). Good channel-to-channel isolation allows active video on all three inputs simultaneously. Antialiasing filtering (if used) and line termination resistors must be provided externally. The input selection is controlled by two bits in the Control Register.

Analog Clamp

The front-end analog clamp ensures that the input video falls within the active range of the A/D converter. The digitized composite video output is clamped to the back porch by a secondary digital clamp.

Automatic Gain Adjustment

Since video signals may vary substantially from nominal levels, the TMC22071 performs an automatic level setting routine to establish correct signal amplitudes for digitizing.

The TMC22071 relies upon the presence of the sync tip-to-back porch voltage to determine the gain required for the input video signal.

Sync tip compression or clipping is often affected by APL (Average Picture Level) variation. Rather than tracking minor variations in sync tip amplitude and constantly adjusting video gain, the TMC22071 establishes proper signal amplitudes during initial genlock acquisition, and then (optionally) holds the gain constant. This results in a stable picture under variable signal conditions.

Improper termination of video cables (usually double termination) is handled in the TMC22071 by a selectable gain of +1.0 or +1.5. The higher gain is used to amplify a doubly-terminated signal which is reduced in amplitude by 2/3.

If the input signal levels are well controlled, the automatic gain adjustment can be disabled and the gain held at its nominal value (unity or 1.5X).

Analog-to-Digital Converter

The TMC22071 contains a high-performance 8-bit A/D converter. Its gain and offset are automatically set as a part of the automatic gain adjustment process during initial signal acquisition, and require no user attention.

The reference voltages to the A/D converter are set up by internal D/A converters under automatic control during genlock acquisition. These voltages determine the gain and offset of the A/D converter with respect to the video level presented at its input.

Low-Pass Filter

The digitized composite video stream is digitally low-pass filtered to remove chrominance components from the sync separator. Filtering provides robust operation by optimizing the signal-to-noise ratio of the synchronizing/blanking portion of the video, improving the accuracy of the back porch blanking level detector.

A digital sync separator provides the output sync signals, $\overline{\text{GHSYNC}}$ and $\overline{\text{GVSYNC}}$, and times internal operations.

Horizontal Phase-Locked Loop

A phase-locked loop generates PXCK, at twice the pixel rate. The reference signal for the horizontal phase-locked loop is generated by the Direct Digital Synthesizer (DDS). The DDS output is constructed with an internal D/A converter and is output from the TMC22071 via the DDS OUT pin. This signal is passed through an external LC filter and input to the horizontal phase-locked loop.

The phase of the DDS output is proportional to the phase difference between PXCK and the horizontal sync of the incoming signal.

A 20 MHz clock is required to drive the DDS. This may be input to the TMC22071 via CMOS levels on the CLK IN pin. Alternately, a 20 MHz crystal may be directly connected between CLK IN and $\overline{\text{CLK}}$ OUT with tuning capacitors to activate the internal crystal oscillator circuitry.

If incoming video is lost or disconnected after the TMC22071 has acquired and locked, PXCK, $\overline{\text{GHSYNC}}$, $\overline{\text{GVSYNC}}$ and GRS data will continue. The GRS data will

be the initial subcarrier frequency and phase values selected by the Format select bits of the Control Register. The TMC22071 will acquire and lock to incoming video within two frames after video is restored.

Subcarrier Phase-Locked Loop

A fully-digital phase-locked loop is used to extract the phase and frequency of the incoming color burst. These frequency and phase values are output over the CVBS bus during the horizontal sync period.

Back Porch Digital Clamp

A digital back-porch clamp is employed to ensure a constant blanking level. It digitally offsets the data from the A/D converter to set the back porch level to precisely $3C_h$ for NTSC and 40_h for PAL. When the digital clamp is enabled, the CVBS video output data is determined from the A/D conversion result minus the back porch level + $3C_h$ (40_h for PAL).

Digitized Video Output

The digitized 8-bit video output is provided over an 8-bit wide CVBS data port, synchronous with PXCK and LDV.

Subcarrier frequency, subcarrier phase, and Field ID data (GRS) are transmitted in 4-bit nibbles over $CVBS_{3-0}$ during the horizontal sync tip period at the PXCK rate.

Microprocessor Interface

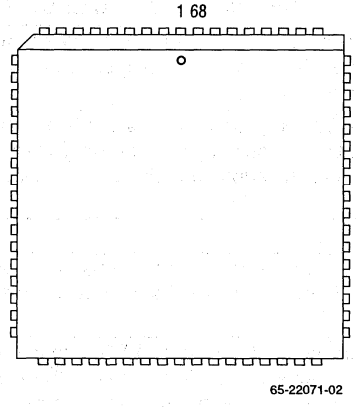
Since microprocessor buses are notoriously noisy from a wide-band analog point of view, the microprocessor interface bus is only one bit wide, rather than the more customary eight. The operation of this bus is similar to other bus-controlled devices except that the TMC22071 internal Control Register is accessed one bit at a time.

A sequence of 47 bits is written to or read from the LSB of a standard microprocessor port. Writing to or reading from the secondary address results in the transfer of data to or from the internal shift register.

The $\overline{\text{RESET}}$ input, when LOW, sets all internal state machines to their initialized conditions. Returning the $\overline{\text{RESET}}$ pin HIGH starts the signal acquisition sequence which lasts until locking with the gain-adjusted and clamped video signal is achieved.

BROADCAST VIDEO

Pin Assignments



65-22071-02

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	18	V_{DD}	35	A_{GND}	52	V_{DD}
2	$CVBS_0$	19	PXCK	36	R_T	53	$\overline{\text{CLK}}$ OUT
3	$CVBS_1$	20	D_{GND}	37	A_{GND}	54	EXT PXCK
4	$CVBS_2$	21	D_{GND}	38	V_{REF}	55	D_{GND}
5	$CVBS_3$	22	V_{DD}	39	A_{GND}	56	D_{GND}
6	$CVBS_4$	23	V_{DDA}	40	V_{DDA}	57	D_{GND}
7	V_{DD}	24	A_{GND}	41	A_{GND}	58	V_{DD}
8	D_{GND}	25	V_{DDA}	42	C_{BYP}	59	V_{DD}
9	$CVBS_5$	26	V_{DDA}	43	PFD IN	60	A_0
10	$CVBS_6$	27	A_{GND}	44	A_{GND}	61	R/$\overline{\text{W}}$
11	$CVBS_7$	28	R_B	45	DDS OUT	62	$\overline{\text{CS}}$
12	$\overline{\text{GHSYNC}}$	29	V_{IN3}	46	PXCK SEL	63	V_{DD}
13	$\overline{\text{GVSYNC}}$	30	V_{DDA}	47	V_{DDA}	64	$\overline{\text{RESET}}$
14	VALID	31	V_{IN2}	48	COMP	65	D_{GND}
15	D_{GND}	32	A_{GND}	49	A_{GND}	66	D_0
16	D_{GND}	33	V_{DDA}	50	D_{GND}	67	$\overline{\text{INT}}$
17	LDV	34	V_{IN2}	51	CLK IN	68	D_{GND}

Pin Definitions

Pin Name	Pin Number	Pin Type	Function
Video Input			
V_{IN1-3}	34, 31, 29	1.23Vp-p	**Composite Video Input.** Video inputs,1.25 Volts peak-to-peak, sync tip to peak color
Clocks			
CLK IN	51	CMOS	**20 MHz DDS clock input.** 20 MHz CMOS clock input to DDS. This pin may also be used along with $\overline{CLK}$ OUT for directly connecting crystals.
$\overline{CLK}$ OUT	53	CMOS	**Inverted clock output.** Inverted DDS clock output. This pin may also be used along with CLK IN for directly connecting a crystal.
PXCK	19	CMOS	**2x Pixel clock output.** 2x oversampled line-locked clock output.
LDV	17	CMOS	**Pixel clock output.** Delayed pixel clock output. LDV runs at 1/2 the rate of PXCK and its rising edge is useful for transferring CVBS digital video from the TMC22071 to the TMC22x9x Digital Video Encoders.
EXT PXCK	54	CMOS	**External PXCK input.** Input for external PXCK clock source.
PXCK SEL	46	CMOS	**PXCK source select.** Select input for internal or external PXCK. When HIGH, the internally generated line-locked PXCK is selected. When LOW, the external PXCK source is enabled.
Digital Video			
$\overline{GHSYNC}$	12	CMOS	**Horizontal sync output.** When the TMC22071 is locked to incoming video, the $\overline{GHSYNC}$ pin provides a negative-going pulse after the falling edge of the horizontal sync pulse. There is a fixed number of PXCK clock cycles between adjacent falling edges of $\overline{GHSYNC}$.
$\overline{GVSYNC}$	13	CMOS	**Vertical sync output.** When the TMC22071 is locked to incoming video, the $\overline{GVSYNC}$ pin provides a negative-going edge after the start of a vertical sync pulse.
$CVBS_{7-0}$	11-9, 6-2	CMOS	**Composite output bus.** 8-bit composite video data is output on this bus at 1/2 the PXCK rate. During the horizontal blanking interval, field ID, subcarrier frequency, and subcarrier phase are available on this bus.
µP I/O			
D_0	66	TTL	**Data I/O port.** Microprocessor data port. All control parameters are loaded into and read back from the Control Register over this 1-bit bus.
A_0	60	TTL	**µP port control.** Microprocessor address bus. A LOW on this input loads the I/O Port Shift Register with data from D_0 and $\overline{CS}$. A HIGH transfers the I/O Port Shift Register contents into the Control Register on the last falling edge of $\overline{CS}$.
$\overline{CS}$	62	TTL	**Chip select.** When $\overline{CS}$ is HIGH, D_0 is in a high-impedance state and ignored. When $\overline{CS}$ is LOW, the microprocessor can read or write D_0 data into the Control Register.
$\overline{RESET}$	64	TTL	**Master reset input.** Bringing $\overline{RESET}$ LOW forces the internal state machines to their starting states, loads the Control Register with default values, and disables outputs. Bringing $\overline{RESET}$ HIGH restarts the TMC22071.
R/$\overline{W}$	61	TTL	**Bus read/write control.** When R/$\overline{W}$ and A_0 are LOW, the microprocessor can write to the Control Register over D_0. When R/$\overline{W}$ is HIGH and A_0 is LOW, the contents of the Control Register are read over D_0.

Pin Definitions (continued)

Pin Name	Pin Number	Pin Type	Function
$\overline{INT}$	67	TTL	**Interrupt output.** This output is LOW if the internal horizontal phase lock loop is unlocked with respect to incoming video for 128 or more lines per field. After lock is established, $\overline{INT}$goes HIGH.
VALID	14	TTL	**HSYNC locked flag.** This output, when HIGH indicates that incoming horizontal sync has been detected and is within the ±16 pixel window in time established by previous sync pulses. When LOW, it indicates that incoming horizontal sync has not been found within the expected time frame. VALID will toggle if the time stability of incoming video is such that sync positioning varies more than ±16 pixels of if occasional horizontal sync pulses are missing.
Analog Interface			
V_{REF}	38	+1.23 V	**V_{REF} input/output.** +1.23 Volt reference. When the internal voltage reference is used, this pin should be decoupled to A_{GND} with a 0.1 µF capacitor. An external +1.2 Volt reference may be connected here, overriding the internal reference source.
COMP	48	0.1 µF	**Compensation capacitor.** Compensation for DDS D/A converter circuitry. This pin should be decoupled to V_{DDA} with a 0.1 µF capacitor.
R_T,R_B	36, 28	0.1 µF	**A/D V_{REF} decoupling.** Decoupling points for A/D converter voltage references. These pins should be decoupled to A_{GND} with a 0.1 µF capacitor.
PLL Filter			
DDS OUT	45		**Internal DDS output.** Analog output from the internal Direct Digital Synthesizer D/A converter.
PFD IN	43		**Horizontal PLL input.** Analog input to the Phase/Frequency Detector of the horizontal phase-locked loop.
C_{BYP}	42	1 µF	**Comparator bypass.** Decoupling point for the internal comparator reference of the Phase/Frequency Detector. This pin should be decoupled to A_{GND} with a 0.1 µF capacitor.
Power Supply			
V_{DDA}	23, 25, 26, 30, 33, 40, 47	+5 V	**Analog power supply.** Positive power supply to analog section.
V_{DD}	1, 7,18, 22, 52, 58,59,63	+5 V	**Digital power supply.** Positive power supply to digital section.
Ground			
A_{GND}	24, 27, 32, 35, 37, 39, 41, 44, 49,	0.0 V	**Analog ground.** Ground for analog section.
D_{GND}	8, 15, 16, 20, 21, 50, 55-57, 65, 68	0.0 V	**Digital ground.** Ground for digital section.

Control and Status Registers

The TMC22071 is controlled by a single 47-bit long Control Register. Access to the Control Register is via the I/O Port Shift Register arranged as shown in Figure 1. The Control Register can be read and written, permitting software modification and examination of its contents. The 12-bit Status Register is read-only and accessed through the same I/O Port Shift Register. Reading the Status Register yields information about blanking level, subcarrier presence, and whether or not PXCK is locked or unlocked with respect to the line rate.

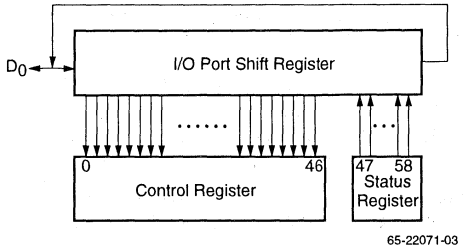


Figure 1. Control and Shift Register Structure

The host processor writes data into the TMC22071 using only one bit of the microprocessor's data and address bus. Once the shift register has input and positioned the 47 bits of desired data (bit 46 first, bit 0 last), a HIGH on A_0 and a LOW on R/$\overline{W}$ when $\overline{CS}$ falls transfers the I/O Port Shift Register contents to the Control Register. The I/O Port Shift Register, Control Register and Status Register are governed by $\overline{CS}$, R/$\overline{W}$, and A_0. R/$\overline{W}$ and A_0 are latched by the TMC22071 on the falling edge of $\overline{CS}$ and data input D_0 is latched on the rising edge of $\overline{CS}$. Data read from D_0 is enabled by the falling edge of $\overline{CS}$ and disabled by the rising edge of $\overline{CS}$. When the Control Register is read more than once consecutively, an extra $\overline{CS}$ pulse and accompanying A_0 is needed to align the circulated shift register data.

Table 1. Microprocessor Port Control

A_0	R/$\overline{W}$	Action
0	0	Write data from D_0 into I/O Port Shift Register
0	1	Read D_0 data from last stage of I/O Port Shift Register
1	0	Transfer I/O Port Shift Register contents to Control Register
1	1	Enables continuous update of status bits in I/O Port Shift Register

The full sequence of 47 bits of Control Register data must be written each time a change in that data is desired. All or a few of the Control and Status Register bits may be read, but the sequence always begins with bit 58 of the Status Register.

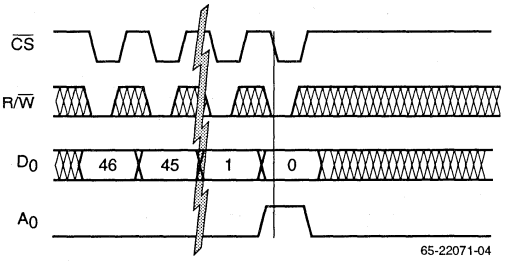


Figure 3. Data Write Sequence

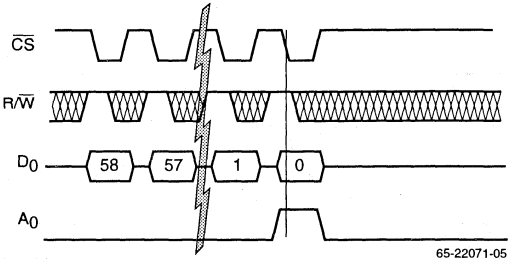


Figure 4. Data Read Sequence

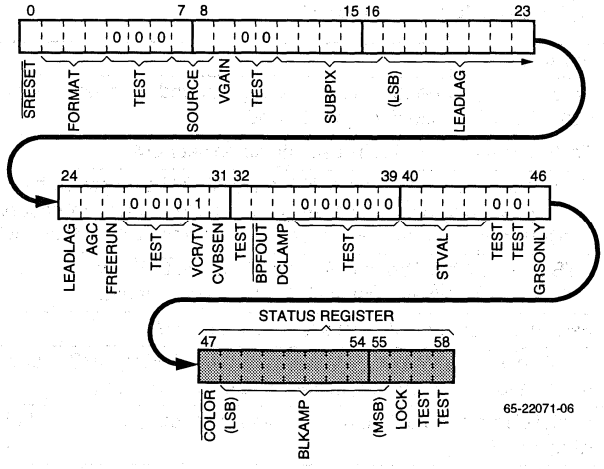


Figure 2. Control Register Map

Control Register Bit Functions

Bit	Name	Function
0	SRESET	Software reset. When LOW, resets and holds internal state machines, resets Control Register with previously written values, and disables output drivers. When HIGH, SRESET starts and runs state machines, PXCK, and enables outputs.
1-3	FORMAT	Input signal format select. Bit 3 is the MSB. 000 NTSC at 12.27 Mpps. 001 NTSC at 13.5 Mpps. 010 PAL at 14.75 MPPS. 011 PAL at 15.0 Mpps. 1 xx PAL at 13.5 Mpps.
4-6	TEST	Factory test control bits. These should be set LOW.
7,8	SOURCE	Video source select. Bit 8 is the MSB. 00 V_{IN1} 01 V_{IN2} 1x V_{IN3}
9	VGAIN	Video gain. When LOW, gain is set to unity. When HIGH, gain is set to 1.5X.
10-11	TEST	Factory test control bits. These should be set LOW.
12-16	SUBPIX	These control bits allows the HSYNC, VSYNC, and sample clock to be time-shifted by -16/32 to +15/32 pixels. Bit 16 is the two's complement MSB. When SUBPIX is 00_h, HSYNC and incoming video are subject to LEADLAG. A value of 18_h delays HSYNC 1/4 pixel. A value of 08_h advances HSYNC 1/4 pixel.
17-24	LEADLAG	This control word allows the HSYNC and VSYNC to be time-shifted -122 to +132 LDV cycles. When LEADLAG is $7B_h$, HSYNC and incoming video are in alignment. A value of 83_h delays HSYNC eight LDV cycles. A value of 73_h advances HSYNC eight LDV cycles. Bit 24 is the MSB.
25	AGC	AGC operation control. When LOW and after H and V sync acquisition, the A/D converter references are adjusted to encompass the full video range. The A/D adjustment sequence is initiated when this bit is HIGH.

Control Register Bit Functions (continued)

Bit	Name	Function
26	FRERUN	When HIGH, a free-running PXCK is generated, independent of incoming video. When LOW, PXCK is locked to incoming video.
27-29	TEST	Factory test control bits. These should be set LOW.
30	VCR/TV	Block sync enable. When HIGH the TMC22071 accepts both normal and block sync. When LOW, only normal sync may be input. For most applications, whether using a VCR or a studio video input source, best performance will be found when this bit is HIGH.
31	CVBSEN	CVBS bus enable. When LOW, the $CVBS_{7-0}$, $\overline{GHSYNC}$, and $\overline{GVSYNC}$ outputs are in a high-impedance state. When HIGH, they are enabled.
32	TEST	Factory test control bit. This should be set LOW.
33	$\overline{BPFOUT}$	Burst phase / frequency output control. When HIGH, GRS is disabled. When LOW, burst phase and frequency information is output on $CVBS_{3-0}$.
34	DCLAMP	Digital clamp enable. The digital clamp is enabled when DCLAMP is HIGH and disabled when LOW.
35-39	TEST	Factory test control bits. These should be set LOW.
40-43	STVAL	Sync tip value. When DCLAMP is HIGH and STVAL is set to its default value 3_h the output sync level is 3_h for NTSC and 7_h for PAL. Bit 43 is the MSB.
44	TEST	Factory test control bit. This should be set HIGH.
45	TEST	Factory test control bit. This should be set LOW.
46	GRSONLY	When the horizontal phase lock loop becomes unlocked (i.e. after video input is disconnected) and this Control Bit is HIGH, all CVBS data is forced LOW except subcarrier frequency and phase data (GRS). $\overline{GHSYNC}$, $\overline{GVSYNC}$, and PXCK continue with default GRS data until video is required. The presence of GRS also depends upon bit 33. If the GRSONLY bit is LOW, $\overline{GHSYNC}$, $\overline{GVSYNC}$, and PXCK continue with default GRS data continue but video pixel data is random. **Status Bits (read only)**
47	$\overline{COLOR}$	Burst present status bit. This bit is HIGH when no burst is present on the input video. It is LOW, when burst is present.
48-55	BLKAMP	Blanking amplitude status bit. These eight bits report the actual blanking level.
56	$\overline{LOCK}$	H-lock loop status bit. When HIGH, the TMC22071 is not locked to an input signal. When LOW, lock has been achieved.
57-58	TEST	These are read-only bits for testing puposes only.

Horizontal Timing

Horizontal line rate is selectable, and is determined by the FORMAT control bits (12.27 Mpps for NTSC, 13.5 Mpps for NTSC and PAL, and either 14.75 or 15.0 Mpps for PAL). Figure 5 illustrates the horizontal blanking interval. Figure 6 completes the definition of timing parameters with vertical blanking interval detail.

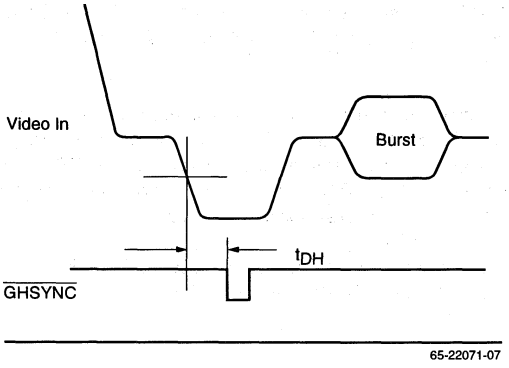


Figure 5. Horizontal Sync Timing

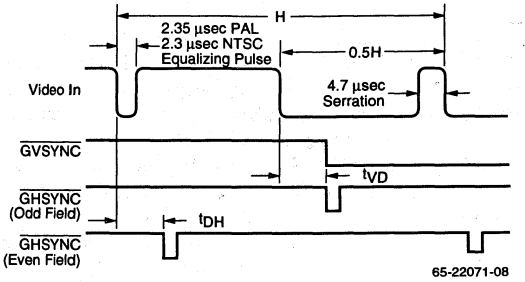


Figure 6. Vertical Sync timing

Programming the TMC22071

Upon power-up after bringing $\overline{\text{RESET}}$ LOW, the TMC22071 Control Register is set to default values as shown in the top entry of Table 3. These default values do not necessarily render the TMC22071 operational in any specific application. Before the TMC22071 is expected to acquire input video, its Control Register must be loaded with data that is specific to its use.

Table 2.TMC22071 Timing Options

Standard	Field Rate (Hz)	Line Rate (kHz)	Pixel Rate (Mpps)	PXCK Frequency (MHz)	Pixels Per Line
NTSC	59.94	15.734264	12.2727+	24.54+	780
NTSC-601	59.94	15.734264	13.50	27.0	858
PAL	50.00	15.625	14.75	29.5	944
PAL	50.00	15.625	15.00	30.0	960
PAL-601	50.00	15.625	13.50	27.0	864

Table 3. Control Register Example Data

	Control Register Data (Bit 56 ..... Bit 0)											
Standard	46	42	38	34	30	26	22	18	14	10	6	2
DEFAULT	0000	0110	0000	1001	0000	0010	0000	0000	0000	0000	0000	001
NTSC	0010	0110	0000	1001	1000	0010	0000	0000	0000	00xx	0000	000
NTSC-601	0010	0110	0000	1001	1000	0010	0000	0000	0000	00xx	0000	010
PAL	0010	1110	0000	1001	1000	0010	0000	0000	0000	00xx	0000	100
PAL	0010	1110	0000	1001	1000	0010	0000	0000	0000	00xx	0000	110
PAL-601	0010	1110	0000	1001	1000	0010	0000	0000	0000	00xx	0001	xx0

CVBS Bus Data Formats

The CVBS bus outputs a Genlock Reference Signal (GRS) along with the 8-bit digital composite video data. The range of output data versus video input voltage is illustrated in Figure 7 where sync tip and blanking levels are controlled by the digital backporch clamp of the TMC22071. During horizontal sync, the TMC22071 outputs field identification, subcarrier frequency, and subcarrier phase information on the CVBS bus.

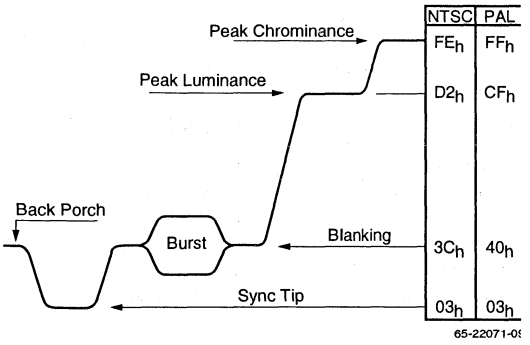


Figure 7. Output Data vs. Input Video Level

Field identification is output on $CVBS_{2-0}$. The LSB, $CVBS_0$, will be LOW during odd fields and HIGH for even fields. When NTSC operation is selected, $CVBS_{1-0}$ count 00,01,10,11 for fields 1 through 4 respectively. When PAL operation is selected, $CVBS_{2-0}$ count 000, 001, 010, etc. to 111 for fields 1 through 8, respectively.

$CVBS_3$ indicates V-component inversion in PAL. It is HIGH for NTSC lines (burst 135°) and LOW for PAL lines (burst 225°)

Subcarrier frequency is sent out in a 24-bit binary representation in six 4-bit nibbles on $CVBS_{3-0}$. Subcarrier frequency data, f_{23-0}, is identical to the pre-programmed BSEED value used in the TMC22071 to lock the subcarrier phase-locked loop to the incoming subcarrier frequency.

Subcarrier phase, Φ_{23-0}, is also sent out in a 24-bit binary representation in six 4-bit nibbles on $CVBS_{3-0}$. Bit Φ_{23} is the MSB.

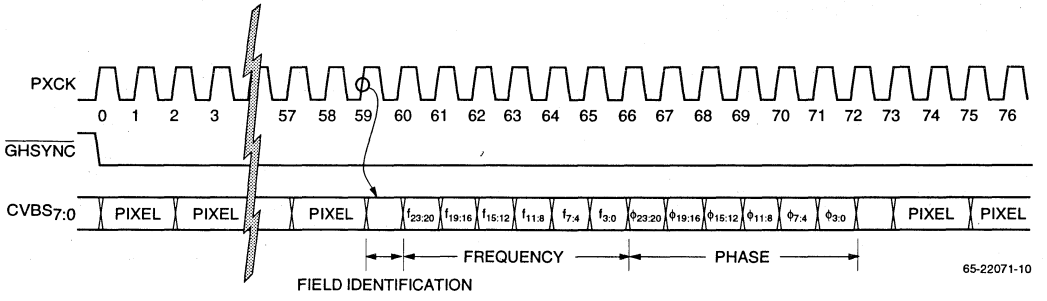


Figure 8. Genlock Reference Signal (GRS) Format

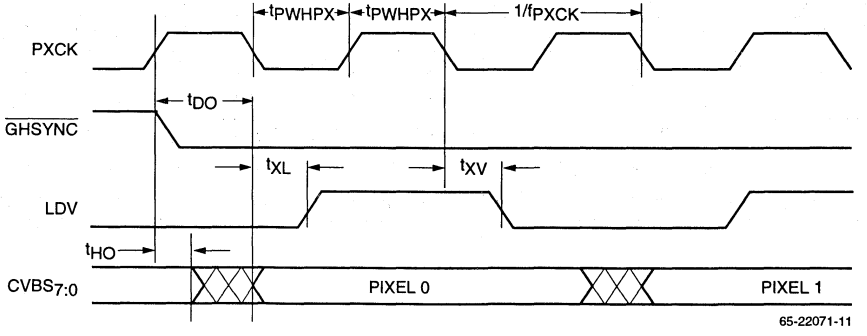


Figure 9. CVBS Bus Video Data Format

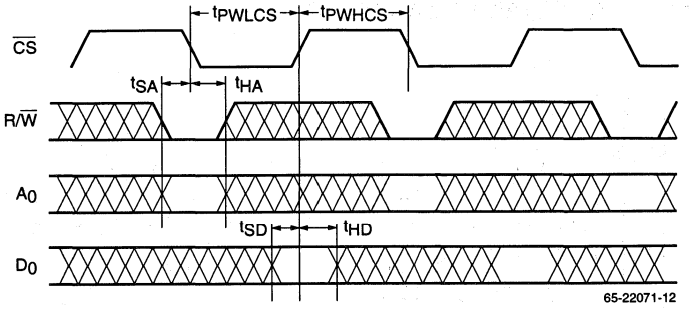


Figure 10. Microprocessor Port - Write Timing

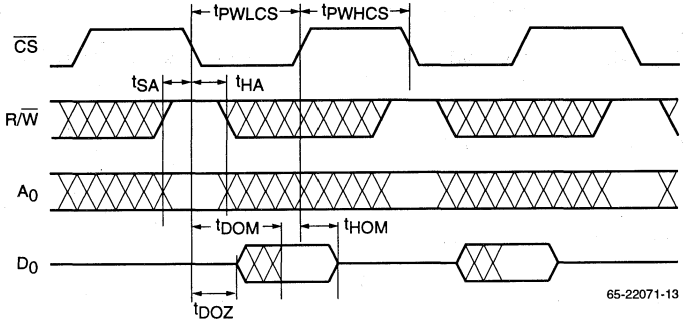


Figure 11. Microprocessor Port - Read Timing

Equivalent Circuits and Transition Levels

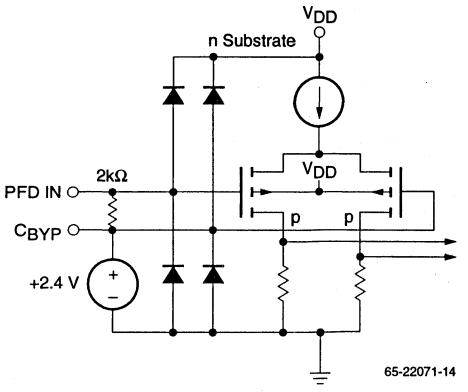


Figure 12. Equivalent PFD IN Circuit

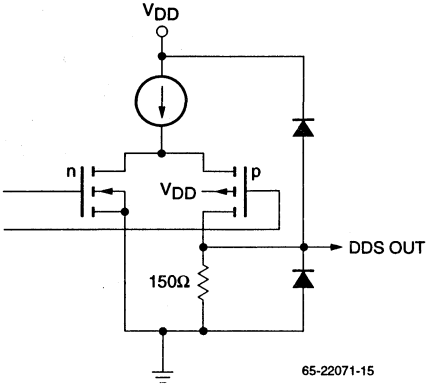


Figure 13. Equivalent DDS OUT Circuit

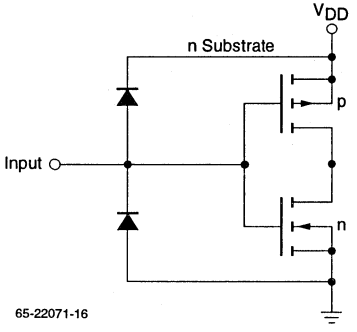


Figure 14. Equivalent Digital Input Circuit

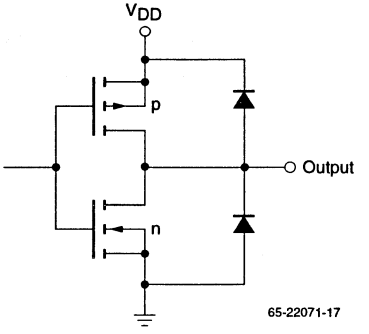


Figure 15. Equivalent Digital Output Circuit

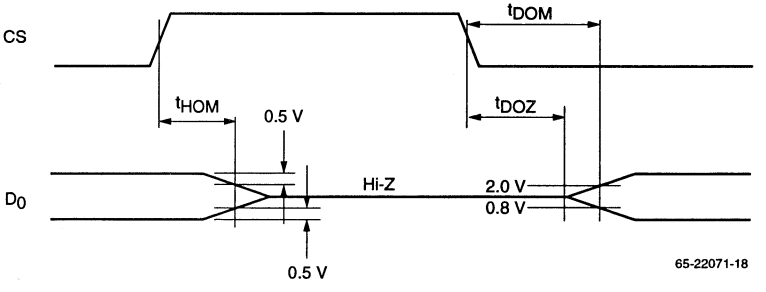


Figure 16. Transition Levels for Three-State Measurements

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Max	Unit
Power Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	V_{DD} + 0.5	V
Digital Outputs			
Applied Voltage[2]	-0.5	V_{DD} + 0.5	V
Forced Current[3,4]	-6.0	6.0	mA
Short Circuit Duration (single output in HIGH state to GND)		1	sec
Temperature			
Operating, Case	-60	130	°C
Operating, Junction		150	°C
Lead Soldering (10 seconds)		300	°C
Vapor Phase Soldering (1 minute)		220	°C
Storage	-65	150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions (for standard temperature range)

Parameter		Min	Nom	Max	Units
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH				
	TTL Inputs	2.0		V_{DD}	V
	CMOS Inputs	2/3V_{DD}		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW				
	TTL Inputs	D_{GND}		0.8	V
	CMOS Inputs	D_{GND}		1/3 V_{DD}	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
V_{IN}	Video Input Signal Level, Sync Tip to Peak White		1.0		V
V_{REF}	External Reference Voltage		1.235		V
T_A	Ambient Temperature, Still Air	0		70	°C
Microprocessor Interface					
t_{PWHCS}	$\overline{CS}$ Pulse Width, LOW		50		ns
t_{PWHCS}	$\overline{CS}$ Pulse Width, HIGH		50		ns
t_{SA}	Address Setup Time		0		ns
t_{HA}	Address Hold Time		7		ns
t_{SD}	Data Setup Time		7		ns
t_{HD}	Data Hold Time		0		ns

Note:

1. Timing reference points are at the 50% level.

Electrical Characteristics (for standard temperature range)

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Current[1]	Total Current V_{DD} = Max, f_{PXCK} = 30MHz		190	230	mA
I_{REF}	Reference Inputcurrent	V_{REF} = +1.235V			100	µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = 4.0V			±10	µA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0.4V			±10	µA
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = -2.0 mA	2.4			V
V_{OL}	Output Voltage, Logic LOW	I_{OL} = 4.0 mA			0.4	V
I_{OZH}	Hi-Z Output Leakage current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage current, LOW	V_{DD} = Max, V_{IN} =GND			±10	µA
C_I	Digital Input Capacitance	T_A = 25°C, f = 1 Mhz		4	15	pF
C_O	Digital Output Capacitance	T_A - 25°C, f = 1 Mhz		10		pF
C_V	Input Capacitance, V_{IN1-3}	T_A = 25°C, f = 3.58 Mhz			15	pF
R_V	Input Resistance, V_{IN1-3}		50			kΩ

Note:

1. Typical I_{DD} with V_{DD} = +5.0 Volts and T_A = 25°C, Maximum I_{DD} with V_{DD} = +5.25 Volts and T_A = 0°C.

Switching Characteristics (for standard temperature range)

Parameter		Conditions	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 35 pF	2		15	ns
t_{HO}	Output Hold Time		3		8	ns
f_{PCK}	Pixel Rate		12		15.3	MHz
f_{PXCK}	Master Clock Rate		24		30.6	MHz
t_{PWHPX}	PXCK Pulse Width, LOW		12			ns
t_{PWHPX}	PXCK Pulse Width, HIGH		12			ns
t_{DH}	Horizontal Sync to $\overline{GHSYNC}$			14		pixels
t_{VD}	Vertical Sync to $\overline{GVSYNC}$			14		pixels
t_{XL}	PXCK LOW to LDV HIGH				8	ns
t_{XV}	PXCK LOW to LDV LOW				8	ns
t_{DOM}	D_0 enable time			20		ns
t_{HOM}	D_0 disable time		10	15		ns
t_{DOZ}	$\overline{CS}$ LOW to D_0 output driven			5		ns

System Performance Characterlstics

Parameter		Min	Type	Max	Units
ESCH	Sync time-base variation[1]			±3	ns
ESCP	Subsarrier Phase Error[1]			±2	degrees
tAL	Line-lock Acquisition Time			2	frames
VXT	Channel-to-Channel Crosstalk @3.58 Mhz			-35	dB

Note:

1. NTSC/PAL compliant black burst at nominal input level ±10%, frequencies nominal ±10 ppm.

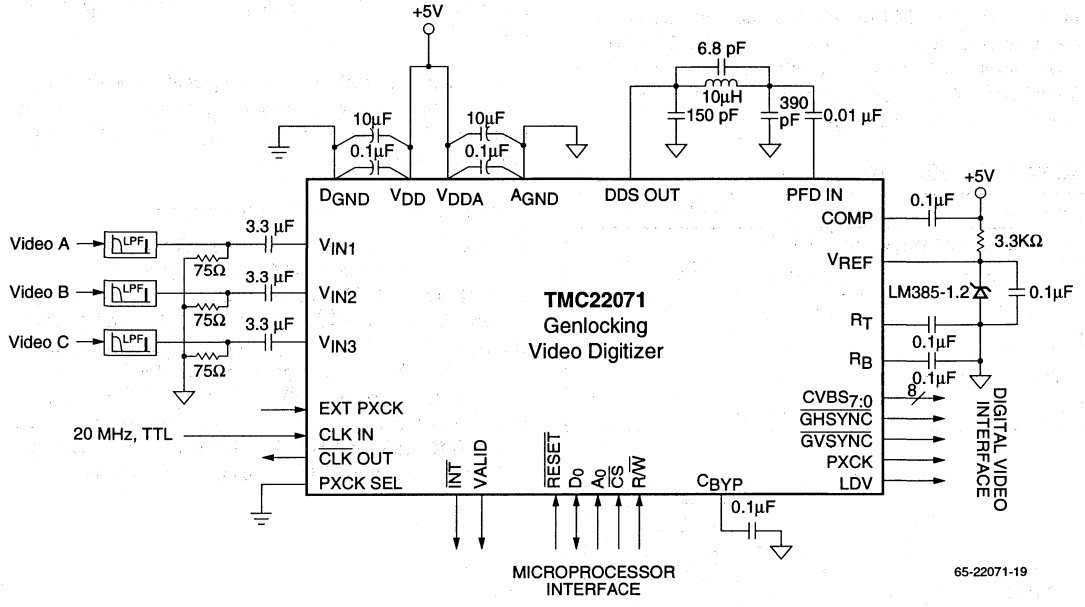


Figure 17. Typical Interface Circuit

Application Notes

The TMC22071 is a complex mixed-signal VLSI circuit. It produces CMOS digital signals at clock rates of up to 15 MHz while processing analog video inputs with a resolution of less than a few millivolts. To maximize performance it is important to provide an electrically quiet operating environment. The circuit shown in Figure 17 provides an optional external 1.2V reference to the VREF input of the TMC22071. The internal VREF source is adequate for most applications.

Filtering

Inexpensive low-pass anti-aliasing filters are shown in Figures 18 and 20. These filters would normally be inserted in the video signal path just before the 75Ω terminating resistor and AC-coupling capacitor for each of the three video inputs, VIN1-3. The filter of Figure 18 exhibits a 5th-order Chebyshev response with-3dB bandwidth of 6.7MHz and a group delay of 140 nanoseconds at 5MHz. The filter of Figure 19 has been equalized for group delay in the video signal band. Its -3dB passband is 5.5MHz while the group delay is constant at 220 nanoseconds through the DC to 5MHz frequency band.

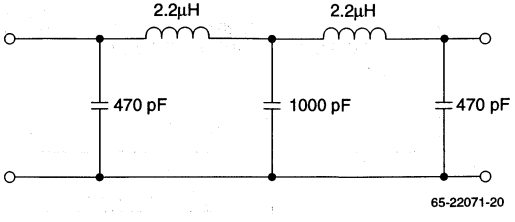


Figure 18. Simple Anti-aliasing Filter

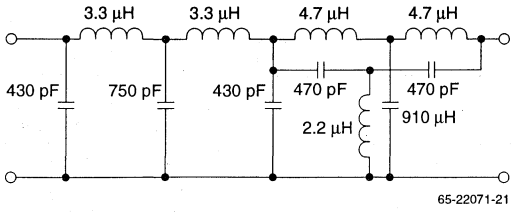


Figure 19. Group Delay Equalizer Filter

Using a 20 MHz Crystal

In systems where a 20 MHz clock is not available, a crystal may be used to generate the clock to the TMC22071. The crystal must be a 20 MHz "fundamental" type, not overtone. Specific crystal characteristics are listed in Table 4 and the connections are shown in Figure 20.

Table 4. Crystal Parameters

Parameter	Value
Fundamental frequency	20 MHz
Tolerance	±30 ppm @ 25°C
Stability	±50 ppm, 0°C to 70°C
Load Capacitance	20 pF
Shunt Capacitance	7 pF Max.
ESR	50 Ω, Max.

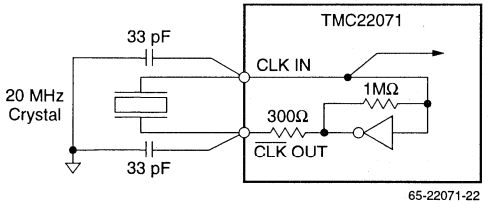


Figure 20. Direct Crystal Connections

Grounding

The TMC22071 has separate analog and digital circuits. To minimize digital crosstalk into the analog signals, the power supplies and ground connections are provided over separate pins (V_{DD} and V_{DDA} are digital and analog power supply pins; D_{GND} and A_{GND} are digital and analog ground pins). In general, the best results are obtained by tying all grounds to a solid, low-impedance ground plane. Power supply pins should be individually decoupled at the pin. Power supply noise isolation may be provided between analog and digital supplies via a ferrite bead inductor. Ultimately all +5 Volt power to the TMC22071 should come from the same power source.

Another approach calls for separating analog and digital ground. While some systems may benefit from this strategy, analog and digital grounds must be kept within 0.1V of each other at all times.

Interface to the TMC22x9x Encoder

The TMC22x9x Digital Video Encoders have been designed to directly interface to the TMC22071 Digital Video Genlock. The TMC22071 is the source for TMC22x9x input signals $CVBS_{7-0}$, $\overline{GHSYNC}$, $\overline{GVSYNC}$, LDV, and PXCK as shown in Figure 21. These signals directly connect to the TMC22x9x. The microprocessor interface for TMC22x9x and TMC22071 are identical. All R/$\overline{W}$, $\overline{RESET}$, data and address bus signals from the host microprocessor are shared by the TMC22x9x and TMC22071. Only $\overline{CS}$, VALID, and $\overline{INT}$ signals are separate from the microprocessor bus.

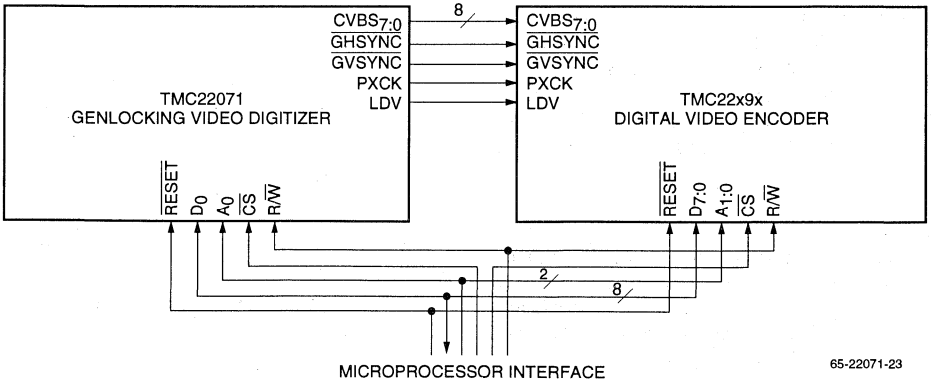


Figure 21. TMC22x9x Interface Circuit

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor picture quality. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (COMP, V_{REF}, R_T, R_B, DDS OUT, PFD IN, C_{BYP}, and V_{IN1-3}) as short as possible and as far as possible from all digital signals. The TMC22071 should be located near the board edge, close to the analog output connectors.

2. The power plane for the TMC22071 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC22071 is the same as that of the system's digital circuitry, power to the TMC22071 should be decoupled with ferrite beads and 0.1 µF capacitors to reduce noise.

3. The ground plane should be solid, nor cross-hatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They typically supply adjacent circuitry on the device, which generate varying amounts of noise. For best results, use 0.1µF capacitors in parallel with 0.01µF capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not overlap the TMC22071, the voltage reference or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the TMC22071 and its related analog circuitry can have an adverse effect on performance.

6. CLK should be handled carefully. Jitter and noise on this clock or its ground reference may degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Related Products

- TMC22x9x Digital Video Encoders
- TMC2242/TMC2243/TMC2246 Video Filters
- TMC22080 Digital Video Mixer
- TMC22x5y Digital Decoders
- TMC2302 Image Manipulation Sequencer

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC22071R1C	TA = 0°C to 70°C	Commercial	68-Lead PLCC	22071R1C

TMC22x5y

Multistandard Digital Video Decoder

Three-Line Adaptive Comb Decoder Family, 8 & 10 bit

Features

- Very high performance, low cost
- Adaptive comb-based decoding
- Multiple pin-compatible versions
  - 3-line, 2-line, and band-split
  - 8- and 10-bit processing
- Internal digital linestores
- Supports field- and frame-based decoding
- Multiple input formats
  - CCIR-601/624 (D1), D2, CVBS, YC
- Multiple output formats
  - CCIR-601/624 (D1), RGB, YC_BC_R
- 10-18 Mpps data rate
- Parallel and serial control interface
- Single +5V power supply

Applications

- Studio television equipment
- Personal computer video input

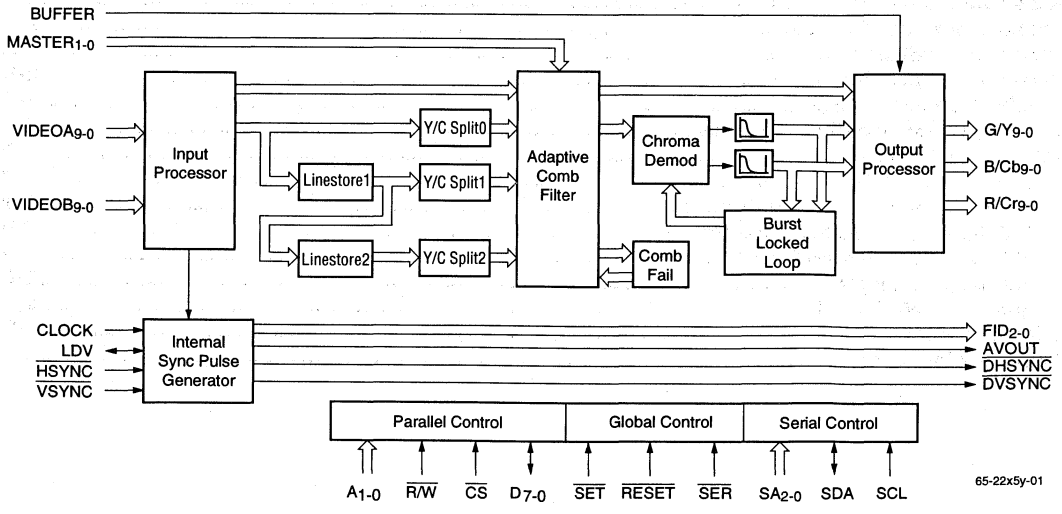
Description

The TMC22x5y family of Digital Video Decoders offers unprecedented, broadcast-quality video processing performance in a single chip. It accepts line-locked or subcarrier-locked composite, YC, or D1 digital video and produces digital components in a variety of formats.

An internal three-line adaptive comb decoder structure produces optimal picture quality with a wide range of source material. Field- and frame-based decoding is supported with external memory. Full comb programmability allows the user to tailor the decoder's response to particular system goals.

A family of products offers 3-line, 2-line, and simple decoders in 8-bit and 10-bit versions—all in a pin- and software-compatible format. Serial and parallel control ports are provided. These submicron CMOS devices are packaged in a 100-lead Metric Quad Flat Pack (MQFP).

Block Diagram



Rev. 0.9.0

Table of Contents

Preliminary Information

General Description

The TMC22x5y digital decoder can be used as a universal input to digital video processing systems by decoding digital composite video and transcoding digital component inputs into a common data format.

The digital comb filter decoder implements one of sixteen comb filter architectures to produce luminance and color difference component signals which are virtually free of the cross-color and cross-luminance artifacts associated with simple bandsplit filter decoders.

Table 1. TMC22x5y Decoder Family

Function	TMC2215y			TMC2205y		
	3	2	1	3	2	1
10-bit Data	✔	✔	✔			
8-bit Data	✔	✔	✔	✔	✔	✔
D1 Interface	✔	✔	✔	✔	✔	✔
Line-Locked Mode	✔	✔	✔	✔	✔	✔
f_{SC}-Locked Mode	✔	✔	✔	✔	✔	✔
Genlock Mode	✔	✔	✔	✔	✔	✔
Frame-Based Comb	✔			✔		
Field-Based Comb	✔			✔		
3-Line Comb	✔			✔		
2-Line Comb	✔	✔		✔	✔	
Line Grab	✔	✔		✔	✔	
Pixel Grab	✔	✔	✔	✔	✔	✔

Because the cost/performance tradeoff varies among applications, the TMC22x5y decoder has been developed as a family of six parts. They are all assembled in the same package, and fit the same footprint. The register,maps are identical.

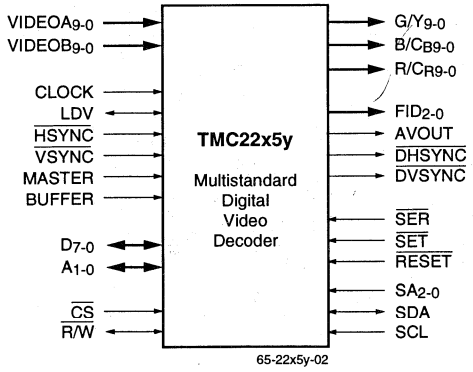


Figure 1. Logic Symbol

The devices come in 8- and 10-bit resolution versions (see Figure 2 for data alignment between 8- and 10-bit versions). Within each resolution version there are three models, offering three-line adaptive comb filtering, two-line adaptive combing, and simple decoding. The TMC22153 10-bit three-line comb filter can be programmed to emulate any of the other parts. All prototyping can be performed with this version to evaluate performance tradeoffs, and lower-cost versions are easily substituted in production.

Input Processor

The digitized video and clocks provided to the decoder can be either locked to the line frequency or the subcarrier frequency of the digitized waveform, providing broadcast quality decoding from the NTSC square pixel rate of 12.27 MHz to the PAL four times subcarrier pixel rate of 17.73 MHz.

MSB					LSB	
VA_9	VA_8		VA_2	VA_1	VA_0	
VB_9	VB_8		VB_2	VB_1	VB_0	
G/Y_9	G/Y_8	•••	G/Y_2	G/Y_1	G/Y_0	10 bit
B/C_{B9}	B/C_{B8}		B/C_{B2}	B/C_{B1}	B/C_{B0}	
R/C_{R9}	R/C_{R8}		R/C_{R2}	R/C_{R1}	R/C_{R0}	

VA_9	VA_8		VA_2	N/C	N/C	
VB_9	VB_8		VB_2	N/C	N/C	
G/Y_9	G/Y_8	•••	G/Y_2	N/C	N/C	8 bit
B/C_{B9}	B/C_{B8}		B/C_{B2}	N/C	N/C	
R/C_{R9}	R/C_{R8}		R/C_{R2}	N/C	N/C	

Figure 2. Pixel Data Format

Inputs containing embedded GRS (Raytheon Video Input Processors), TRS words (D1 multiplexed component signals), and TRS-ID words (deserialized D2 signals) can be used to lock the internal horizontal and vertical state machines to the embedded information. If this information is not provided, external horizontal and vertical syncs are required for all line-locked input formats, and are optional for NTSC inputs locked to four times the subcarrier (4*Fsc). A simple sync separator is provided for digitized inputs locked to the subcarrier frequency: the internal sync separator locks to the mid point of syncs during the vertical field group, then flywheels during the active portion of the field. For this reason, the $\overline{\text{DHSYNC}}$ and $\overline{\text{DVSYNC}}$ operations are not guaranteed in subcarrier mode.

Adaptive Comb Filter

The line based adaptive comb filter in the TMC22x5y adds or subtracts the high frequency data from three adjacent field lines to produce the average of the high frequency luminance by canceling the chrominance signals, which in flat fields of color are 180 degrees apart. Unfortunately flat fields of color are rare and, when vertical transitions in the picture occur, the output of the comb filter contains a mixture of both high frequency luminance and chrominance, at which time the comb fails. To avoid the comb filter artifacts that occur when this happens, three sets of error signals are sent to a user-programmable lookup table, allowing the output of the comb filter to be mixed with the output of an internal bandsplit decoder.

To produce these comb fail error signals, the video on each of the inputs to the comb filter is passed through a simple bandsplit decoder. The low-frequency portion of the signal is assumed to be luminance and the high frequency portion is

processed as chrominance to find the magnitude and phase of the chrominance vector. These three components are then compared across the (0H & 1H) and (1H & 2H) taps of the comb filter to produce the difference in luminance, chrominance magnitude, and chrominance phase. These differences are then translated in the user-programmable lookup table to produce the "K" signal which controls the complementary mix between the output of the comb filter and the simple bandsplit decoder. That is, the K signals controls how much of the combed high frequency luminance signal is subtracted from the simple bandsplit chrominance for chroma combs, or added to the low frequency output of the bandsplit for luma comb filters.

Output Processor

The demodulated chrominance signal and the luminance signal are passed through a programmable output matrix, producing RGB, YUV, or YC_BC_R. When the input is at 27MHz, a D1 signal can be produced on the R/V output with the embedded TRS words fixed to the external $\overline{HSYNC}$ and $\overline{VSYNC}$ timing.

Parallel and Serial Microprocessor Interfaces

The parallel microprocessor interface employs 12 pins, the serial port uses 5. A single pin, $\overline{SER}$, selects between the two interface modes.

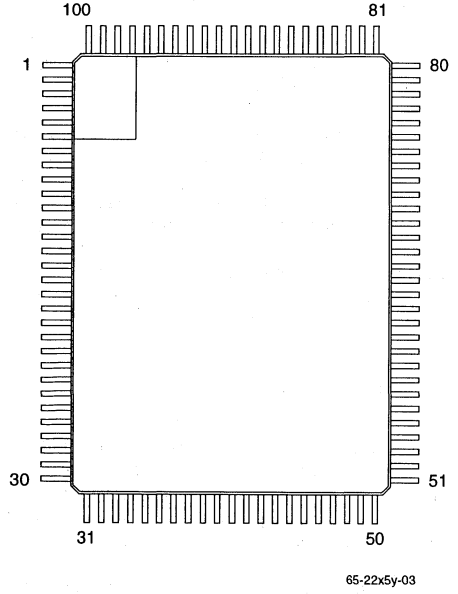
In parallel interface mode, one address line is decoded for access to the internal control register and its pointer. Controls are reached by loading a desired address through the 8-bit D_{7-0} port, followed by the desired data (read or write) for that address. The control register address pointer auto-increments to address 3Fh and then remains there.

A 2-line serial interface may also be used for initialization and control. The same set of registers accessed by the parallel port is available to the serial port. The device address in the serial interface is selected via pins SA_{2-0}.

The $\overline{RESET}$ pin sets all internal state machines to their initialized conditions and places the decoder in a power-down mode. All register data are maintained while in power-down mode.

Preliminary Information

Pin Assignments



65-22x5y-03

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	G/Y_1	26	R/Cr_1	51	$\overline{RESET}$	76	GND
2	G/Y_0	27	R/Cr_0	52	$\overline{SET}$	77	$VIDEOA_0$
3	LDV	28	GND	53	$\overline{SER}$	78	$VIDEOA_1$
4	GND	29	V_{DD}	54	SA_0	79	$VIDEOA_2$
5	V_{DD}	30	AVOUT	55	SA_1	80	$VIDEOA_3$
6	B/Cb_9	31	FID_0	56	SA_2	81	$VIDEOA_4$
7	B/Cb_8	32	FID_1	57	GND	82	$VIDEOA_5$
8	B/Cb_7	33	FID_2	58	SDA	83	$VIDEOA_6$
9	B/Cb_6	34	$\overline{DHSYNC}$	59	SCL	84	$VIDEOA_7$
10	B/Cb_5	35	$\overline{DVSYNC}$	60	$\overline{CS}$	85	$VIDEOA_8$
11	B/Cb_4	36	D_0	61	$R/\overline{W}$	86	$VIDEOA_9$
12	B/Cb_3	37	D_1	62	A_0	87	$MASTER_0$
13	B/Cb_2	38	D_2	63	A_1	88	$MASTER_1$
14	B/Cb_1	39	GND	64	GND	89	CLOCK
15	B/Cb_0	40	V_{DD}	65	V_{DD}	90	GND
16	GND	41	D_3	66	$VIDEOB_0$	91	V_{DD}
17	V_{DD}	42	D_4	67	$VIDEOB_1$	92	GND
18	R/Cr_9	43	D_5	68	$VIDEOB_2$	93	G/Y_9
19	R/Cr_8	44	D_6	69	$VIDEOB_3$	94	G/Y_8
20	R/Cr_7	45	D_7	70	$VIDEOB_4$	95	G/Y_7
21	R/Cr_6	46	GND	71	$VIDEOB_5$	96	G/Y_6
22	R/Cr_5	47	V_{DD}	72	$VIDEOB_6$	97	G/Y_5
23	R/Cr_4	48	$\overline{HSYNC}$	73	$VIDEOB_7$	98	G/Y_4
24	R/Cr_3	49	$\overline{VSYNC}$	74	$VIDEOB_8$	99	G/Y_3
25	R/Cr_2	50	BUFFER	75	$VIDEOB_9$	100	G/Y_2

Pin Descriptions

Pin Name	Pin Number	Value	Pin Function Description
Inputs			
VIDEOA$_{9-0}$	86, 85, 84, 83, 82, 81, 80, 79, 78, 77	TTL	**Video input A.** An 8 or 10 bit data input to the input multiplexer. For 8-bit versions (TMC2205y) the data are left-justified (VIDEOA$_{9-2}$).
VIDEOB$_{9-0}$	75, 74, 73, 72, 71, 70, 69, 68, 67, 66	TTL	**Video input B.** An 8 or 10 bit data input to the input multiplexer. For 8-bit versions (TMC2205y) the data are left-justified (VIDEOB$_{9-2}$).
$\overline{\text{VSYNC}}$	49	TTL	**Vertical sync input.** A vertical sync signal (active low) occurring at the start of the first vertical sync pulse in a vertical field group. A falling edge of $\overline{\text{VSYNC}}$ which is coincident with a falling edge of $\overline{\text{HSYNC}}$ indicates field 1. This signal is active only when SPGIP$_{1-0}$ = 00.
$\overline{\text{HSYNC}}$	48	TTL	**Horizontal sync input.** A horizontal sync signal (active low) occurring at the falling edge of the video sync. This signal is active only when SPGIP$_{1-0}$ = 00.
MASTER$_{1-0}$	88, 87	TTL	**Master decoder control.** 00 Adaptive comb decoder 01 Simple bandsplit decoder 10 Non adaptive comb filter 11 Flat notched luma and simple bandsplit chroma
BUFFER	50	TTL	**Control register select.** This signal switches between two sets of registers which control the gain or hue values in the output matrix. When BUFFER = 0, registers 17-1F are active. When BUFFER = 1, registers 27-2F take control.
CLOCK	89	TTL	**Master processing clock.** The clock signal can be either at the pixel data rate (10MHz to 18MHz), in which case the clock is frequency doubled internally; or the clock signal is at twice the pixel data rate (20MHz to 36MHz), and the clock frequency is halved internally. In either case the pixel rate clock is synchronized to the falling edge of $\overline{\text{HSYNC}}$. The interpretation of the CLOCK signal is set by the CKSEL bit.
$\overline{\text{SET}}$	52	TTL	**Programmable function pin.** The function specified by the SET register is active when $\overline{\text{SET}}$ is low. The decoder returns to its previous operation when $\overline{\text{SET}}$ goes high.
Outputs			
G/Y$_{9-0}$	93, 94, 95, 96, 97, 98, 99, 100, 1, 2	TTL	**Green or Luminance digital output.** For 8-bit versions (TMC2205y) the data are left-justified (G/Y$_{9-2}$).
B/C$_{B9-0}$	6, 7, 8, 9, 10, 11, 12, 13, 14, 15	TTL	**Blue or C_B digital output.** For 8-bit versions (TMC2205y) the data are left-justified (B/C$_{B\ 9-2}$).
R/C$_{R9-0}$	18, 19, 20, 21, 22, 23, 24, 25, 26, 27	TTL	**Red or C_R digital output.** For 8-bit versions (TMC2205y) the data are left-justified (R/C$_{R\ 9-2}$).
$\overline{\text{DVSYNC}}$	35	TTL	**Vertical sync output.** The $\overline{\text{DVSYNC}}$ signal occurs once per field and lasts for 1 video line.
$\overline{\text{DHSYNC}}$	34	TTL	**Horizontal sync output.** The $\overline{\text{DHSYNC}}$ signal occurs once per line and lasts for 64 clock periods.

Pin Descriptions (continued)

Pin Name	Pin Number	Value	Pin Function Description
LDV	3	TTL	**Data synchronization output.** LDV can be an internally or externally generated clock signal. The internal LDV signal is produced when the CLOCK input is at twice the pixel data rate (PXCK); and is a pixel data rate clock phase locked to the falling edge of the HSYNC. The external LDV can be selected under software control, and must be at the CLOCK, or a sub multiple of the CLOCK, frequency.
AVOUT	30	TTL	**Active video output flag.** The active video output is HIGH during the video portion of each line and LOW during the horizontal and vertical blanking intervals.
FID_{2-0}	33, 32, 31	TTL	**Field identification output.** A 3 bit field ident from the DRS signal.
µP Interface			
D_{7-0}	45, 44, 43, 42, 41, 38, 37, 36	TTL	**Parallel control port data I/O.** All control parameters are loaded into and read back over this 8 bit data port.
A_{1-0}	63, 62	TTL	**Parallel control port address inputs.** These pins govern whether the microprocessor interface selects a table/register address or reads/ writes table/register contents.
$\overline{CS}$	60	TTL	**Parallel control port chip select.** When $\overline{CS}$ is high the microprocessor interface port, D_{7-0}, is set to HIGH impedance and ignored. When $\overline{CS}$ is LOW, the microprocessor can read or write parameters over D_{7-0}.
$\overline{R/W}$	61	TTL	**Parallel control port read/write control.** When $\overline{R/W}$ and $\overline{CS}$ are LOW, the microprocessor can write to the control registers or XLUT over D_{7-0}. When $\overline{R/W}$ is HIGH and $\overline{CS}$ is LOW, it can read the contents of any selected XLUT address or control register over D_{7-0}.
$\overline{RESET}$	51	TTL	**Chip master reset.** Bringing $\overline{RESET}$ LOW sets the software reset control bit, $\overline{SRESET}$, LOW and disables the digital outputs. If HRESET is LOW the decoder outputs remain disabled after $\overline{RESET}$ goes HIGH until the $\overline{SRESET}$ bit is set high by the host. If HRESET is HIGH when $\overline{RESET}$ goes HIGH the decoder the internal state machines are enabled.
$\overline{SER}$	53	TTL	**Serial/parallel interface select.** This pin will select between a parallel (HIGH) or serial (LOW) interface port.
SDA	58	R-Bus	**Serial data interface.** Bi-directional serial interface to the control port.
SCL	59	R-Bus	**Serial interface clock.**
SA_{2-0}	56, 55, 54	TTL	**Serial Address.** Three bits providing the lsbs of the serial chip ID used to identify the decoder.
Power Supply			
V_{DD}	5, 17, 29, 40, 47, 65, 91	+5 V	**Power Supply.** Positive power supply for digital circuits, +5V.
GND	4, 16, 28, 39, 46, 57, 64, 76, 90, 92	0.0 V	**Ground.** Ground for digital circuits, 0V.

Control Register Map

The TMC22x5y is initialized and controlled by a set of registers which determine the operating modes.

An external controller is employed to write and read the Control Registers through either the 8-bit parallel or 2-line serial interface port. The parallel port, D_{7-0}, is governed by pins $\overline{CS}$, $\overline{R/W}$, and A_{1-0}. The serial port is controlled by SDA and SCL.

Reg	Bit	Name	Function
Global Control			
00	7	SRST	Software reset
00	6	HRST	Hardware reset
00	5-3	SET	$\overline{SET}$ pin function
00	2	DHVEN	Output H&V sync enable
00	1-0	STD	Selects video standard
Input Processor Control			
01	7		reserved, set to zero
01	6	IPMUX	Input mux control
01	5	IP8B	8 bit input format
01	4	TDEN	TRS detect enable
01	3	TBLK	TRS blank enable
01	2	IPCMSB	Chroma input msb invert
01	1	ABMUX	AB mux control
01	0	CKSEL	Input clock rate select
Burst Loop Control			
02	7		reserved, set to zero
02	6	VIPEN	Video Input Processor enable
02	5-4	LOCK	Global lock mode
02	3	BLM	BLL lock mode
02	2	KILD	Color kill disable
02	1	DMODBY	Demod bypass
02	0	CINT	C_BC_R interpolation enable
Chroma Processor Control			
03	7-5	BLFS	Burst loop filter select
03	4	CCEN	Chroma coring enable
03	3-2	CCOR	Chroma coring threshold
03	1	GAUBY	Gaussian filter bypass
03	0	GAUSEL	Gaussian filter select
Burst Threshold			
04	7-0	BTH	Burst threshold
Pedestal			
05	7-0	PED	Pedestal level
Luma Processor Control			
06	7-6		reserved, set to zero
06	5	ANEN	Adaptive notch enable
06	4	ANR	Adaptive notch rounding
06	3-2	ANT	Adaptive notch threshold
06	1	ANSEL	Adaptive notch select
06	0	NOTCH	Notch enable
Comb Processor Control			
07	7	LS1BY	Line store 1 bypass
07	6	LS1IN	Line store 1 input
07	5	LS2DLY	Line store 2 delay
07	4	SPLIT	Line store 2 data width
07	3	BSFBY	Bandsplit filter bypass
07	2	BSFSEL	Bandsplit filter select
07	1	BSFMSB	Inverts msb of bandsplit filter
07	0	GRSDLY	Delays input to GRS decode by 1H
Mid-Sync Level			
08	7-0	MIDS	Mid-sync level
Extended DRS			
09	7-4	PCKF	Clock rate
09	3-0	VSTD	Video standard
Output Control			
0A	7	OP8B	Output rounded to 8 bits
0A	6-5	OPLMT	Output limit select
0A	4-3	MSEN	Mixed sync enable
0A	2	OPCMSB	Chroma output msb invert
0A	1	YBAL	Luma color correction
0A	0	BUREN	Output burst enable
0B	7	FMT422	Enables C_BC_R output mux
0B	6	CDEC	C_BC_R decimation enable
0B	5	YUVT	Enables D1 output
0B	4-2		reserved, set to zero
0B	1	DRSEN	DRS output enable
0B	0	DRSCK	DRS data rate
Comb Filter Control			
0C	7-6	ADAPT	Adaption mode
0C	5	YCES	YC input error signal control
0C	4	YCSEL	luma/chroma comb filter select
0C	3-0	COMB	Comb filter architecture
0D	7-6	CEST	Chroma error signal transform

Reg	Bit	Name	Function
0D	5	CESG	Chroma error signal gain
0D	5-4	YESG	Luma error signal gain
0D	3	CESTBY	Chroma error signal bypass
0D	2	XFEN	XLUT filter enable
0D	1	FAST	Adaption speed select
0D	0	YWBY	Luma weighting bypass
0E	7-6	XIP	XLUT input select
0E	5-4	XSF	XLUT special function
0E	3-2	YMUX	Y output select
0E	1-0	CMUX	C output select
0F	7		reserved, set to zero
0F	6-5		Adaption Threshold
0F	4	DCES	D1 C_BC_R error signal
0F	3-2	IPCF	Comb filter input select
0F	1	YCCOMP	YC or Composite input select
0F	0	SYNC	Sync processor select
Sync Pulse Generator			
10	7-0	STS_{7-0}	Sync to sync 8 lsbs
11	7-0	STB	Sync to burst
12	7-0	BTV	Burst to video
13	7-0	AV_{7-0}	Active video line 8 lsbs
14	7-6		reserved, set to zero
14	5-4	AV_{9-8}	Active video line 2 msbs
14	3		reserved, set to zero
14	2-0	STS_{10-8}	Sync to sync 3 msbs
15	7		reserved, set to zero
15	6-2	VINDO	Number of lines in vertical window
15	1	VDIV	Action inside VINDO
15	0	VDOV	Action outside VINDO
16	7-6		reserved, set to zero
16	5-4	NFDLY	new field detect delay
16	3-2	SPGIP	SPG input select
16	1-0	MSIP	Mixed sync separator input select
Buffered register set 0 Active when BUFFER pin set LOW			
17	7-0	$SG0_{7-0}$	Msync gain, 8 lsbs
18	7-0	$YG0_{7-0}$	Y gain, 8 lsbs
19	7-0	$UG0_{7-0}$	U gain, 8 lsbs
1A	7-0	$VG0_{7-0}$	V gain, 8 lsbs

Reg	Bit	Name	Function
1B	7-6	$YG0_{9-8}$	Y gain, 2 msbs
1B	5-3	$UG0_{10-8}$	U gain, 3 msbs
1B	2		reserved, set to zero
1B	1-0	$VG0_{9-8}$	V gain, 2 msbs
1C	7-0	$YOFF0_{7-0}$	Y offset, 8 lsbs
1D	7-3		reserved, set to zero
1D	2	$YOFF0_8$	Y offset, msb
1D	1-0	$SG0_{7-0}$	Msync gain, 2 msbs
1E	7-0	$SYSPH0_{7-0}$	8 lsbs of phase
1F	7-0	$SYSPH0_{15-8}$	8 msbs of phase
Normalized Subcarrier Frequency			
20	7-4	FSC_{3-0}	Bottom 4 bits of f_{SC}
20	3-0		reserved, set to zero
21	7-0	FSC_{11-4}	Lower 8 bits of f_{SC}
22	7-0	FSC_{19-12}	Middle 8 bits of f_{SC}
23	7-0	FSC_{27-20}	Top 8 bits of f_{SC}
24-25	7-0		reserved, set to zero
Output Format Control			
26	7-6		reserved, set to zero
26	5	LDVIO	LDV clock select
26	4	OPCKS	Output clock select
26	3	DPCEN	DPC enable
26	2-0	DPC	Decoder product code
Buffered register set 1 Active when BUFFER pin set HIGH			
27	7-0	$SG1_{7-0}$	Msync gain, 8 lsbs
28	7-0	$YG1_{7-0}$	Y gain, 8 lsbs
29	7-0	$UG1_{7-0}$	U gain, 8 lsbs
2A	7-0	$VG1_{7-0}$	V gain, 8 lsbs
2B	7-6	$YG1_{9-8}$	Y gain, 2 msbs
2B	5-3	$UG1_{10-8}$	U gain, 3 msbs
2B	2		reserved, set to zero
2B	1-0	$VG1_{9-8}$	V gain, 2 msbs
2C	7-0	$YOFF1_{7-0}$	Y offset, 8 lsbs
2D	7-3		reserved, set to zero
2D	2	$YOFF1_8$	Y offset, msb
2D	1-0	$SG1_{7-0}$	Msync gain, 2 msbs
2E	7-0	$SYSPH1_{7-0}$	8 lsbs of phase
2F	7-0	$SYSPH1_{15-8}$	8 msbs of phase

Reg	Bit	Name	Function
Video Measurement			
30	7		set to zero
30	6	LGF	Line grab flag
30	5	LGEN	Line grab enable
30	4	LGEXT	Ext line grab enable
30	3		reserved, set to zero
30	2	PGG	Pixel grab gate
30	1	PGEN	Pixel grab enable
30	0	PGEXT	Ext pixel grab enable
31	7-0	PG_{7-0}	Pixel grab, 8 lsbs
32	7-0	LG_{7-0}	Line grab, 8 lsbs
33	7		reserved, set to zero
33	6-4	FG	Field grab number
33	3	LG_8	Msb of line grab
33	2-0	PG_{10-8}	Pixel grab, 3 msbs
34	7-0	GY_{9-2}	G/Y grab, 8 msbs
35	7-0	BU_{9-2}	B/U grab, 8 msbs
36	7-0	RV_{9-2}	R/V grab, 8 msbs
37	7-6		reserved
37	5-4	GY_{1-0}	G/Y grab, 2 lsbs
37	3-2	BU_{1-0}	B/U grab, 2 lsbs
37	1-0	RV_{1-0}	R/V grab, 2 lsbs
38	7-0	Y_{9-2}	Luma grab, 8 msbs
39	7-0	M_{9-2}	Msync grab, 8 msbs
3A	7-0	U_{9-2}	U grab, 8 msbs
3B	7-0	V_{9-2}	V grab, 8 msbs
3C	7-6	Y_{1-0}	Luma grab, 2 lsbs
3C	5-4	M_{1-0}	Msync grab, 2 lsbs
3C	3-2	U_{1-0}	U grab, 2 lsbs
3C	1-0	V_{1-0}	V grab, 2 lsbs
Test Control			
3D-3F	7-0	TEST	set to zero
Auto-increment stops at 3F			
Status - Read Only			
40	7-0	DDSPH	DDS phase, 8 msbs
41	7	LINEST	Pixel count reset
41	6	BGST	Start of burst gate
41	5	VACT2	Half line flag
41	4	PALODD	PAL Ident
41	3	VFLY	Vertical count reset
41	2	FGRAB	Field grab
41	1	LGRAB	Line grab
41	0	PGRAB	Pixel grab
42	7	FLD	Field flag (F in D1 output)
42	6	VBLK	Vertical blanking (V in D1 output)
42	5	HBLK	Horizontal blanking (H in D1 output)
42	4-0	LID	Line identification
43	7	YGO	Y/G overflow
43	6	YGU	Y/G underflow
43	5	UBO	C_B/B overflow
43	4	UBU	C_B/B underflow
43	3	VRO	C_R/R overflow
43	2	VRU	C_R/R underflow
43	1-0		reserved
44	7	MONO	Color kill active
44	6-0	FPERR	Frequency/Phase error
45	7-0	DRS	DRS signal
46	7-0	PARTID	Reads back xx_h
47	7-0	REVID	Revision number
48-4A	7-0		reserved
4B	7	PKILL	Phase kill from comb fail
4B	6-5	CFSTAT	Comb filter status
4B	4-0	XOP	XLUT output
4C-FF	7-0		reserved

Notes:

1. Functions are listed in the order of reading and writing.
2. For each register listed above up to register 3F, all bits not specified are reserved and must be set to zero to ensure proper operation.

Control Register Definitions

Global Control Register (00)

7	6	5	4	3	2	1	0
$\overline{\text{SRST}}$	HRST	SET			DHVEN	STD	

Reg	Bit	Name	Description
00	7	$\overline{\text{SRST}}$	**Software reset.** When LOW, resets and holds internal state machines and disables outputs. When HIGH (normal), starts and runs state machines and enables outputs. This bit is ignored while HRST is high.
00	6	HRST	**Hardware reset.** When HRST is HIGH, $\overline{\text{SRST}}$ is forced low when $\overline{\text{RESET}}$ pin is taken LOW. State machines are reset and held. When HRST is low the $\overline{\text{RESET}}$ pin can be taken HIGH at any time. The state machines remain disabled until $\overline{\text{SRST}}$ is programmed HIGH. When HRST is high the state machines are enabled as soon as the $\overline{\text{RESET}}$ pin goes HIGH.
00	5-3	SET	**$\overline{\text{SET}}$ pin function.** These bits control the set function when the $\overline{\text{SET}}$ pin goes low. A = all outputs high-impedance B = internal state machines C = burst locked loop **SET** / **Function** 000 — Reset and hold A, B, & C. 001 — Set output to BLUE and flywheel B & C. (RGB outputs) Set output to "color" and flywheel B & C (YC_BC_R outputs) 010 — Hold A, lock B & C to external input 011 — Reset C only 100 — Reset B & C 101 — Set output to BLUE and lock B & C to input video (RGB output) 110 — Line and pixel grab depending on $VMCR_{6-0}$ (reg 30) 111 — Toggle reset function of SET = 010. For each $\overline{\text{SET}}$ = 0 pulse the chip operation will change from normal to that of SET = 010 or visa versa. The first $\overline{\text{SET}}$ pulse after a software or hardware reset, with SET = 111, causes a toggle to SET = 010.
00	2	DHVEN	**Output H&V sync enable.** Disables $\overline{\text{DHSYNC}}$ and $\overline{\text{DVSYNC}}$ signals when HIGH.
00	1-0	STD	**Selects video standard.** Selects video standard. **SET** / **Function** 00 — NTSC 01 — reserved 10 — PAL/M 11 — All PAL standards except PAL/M

Control Register Definitions (continued)

Input Processor Control (01)

7	6	5	4	3	2	1	0
Reserved	IPMUX	IP8B	TDEN	TBLK	IPCMSB	ABMUX	CKSEL

Reg	Bit	Name	Description
01	7	Reserved	**Reserved, set to zero.**
01	6	IPMUX	**Input mux control.** Used to select the Video Input Processor, D1, or D2 data as the VA input to the input processor. VIDEOA is selected for VA and VIDEOB is selected for VB when IPMUX is set LOW. VIDEOB is selected for VA and VIDEOA for VB when IPMUX is set HIGH. For YC inputs, the luma data must be passed through the VA input and chroma through the VB input. IPMUX should be set LOW for line locked composite inputs.
01	5	IP8B	**8 bit input format.** Bottom two bits of inputs $VIDEOA_{9-0}$ and $VIDEOB_{9-0}$ are set to zero when HIGH.
01	4	TDEN	**TRS detect enable.** When HIGH, the TRS words embedded in incoming video are used to reset the horizontal and vertical state machines. When LOW the externally provided or internally generated HSYNC and VSYNC are used to reset the horizontal and vertical state machines.
01	3	TBLK	**TRS blank enable.** Blanks the TRS and AUX data words when HIGH. For line locked and D1 data, the TRS and AUX data words are set to the luma and chroma blanking levels as appropriate. For D2 ($4*f_{SC}$) data, the TRS and AUX data words are set to the sync tip level.
01	2	IPCMSB	**Chroma input msb invert.** The msb of the chroma or C_BC_R data are inverted when HIGH.
01	1	ABMUX	**AB mux control.** Selects the primary and secondary inputs to the decoder from the DA and DB outputs of the input processor. When ABMUX is LOW, DA is selected as the primary and DB as the secondary decoder input.
01	0	CKSEL	**Input clock rate select.** Set HIGH when input clock rate is PXCK (twice the pixel rate) and set LOW when input clock rate is PCK.

Control Register Definitions (continued)

Burst Loop Control (02)

7	6	5	4	3	2	1	0
Reserved	VIPEN	LOCK		BLM	KILD	DMODBY	CINT

Reg	Bit	Name	Description
02	7	Reserved	**Reserved, set to zero.**
02	6	VIPEN	**Video Input Processor enable.** Selects interface protocol for Raytheon video input devices. Active only when $LOCK_{1-0} = 10$. VIPEN: 0 = Video Input Processor Interface; 1 = TMC22071 Interface
02	5-4	LOCK	**Global Lock mode.** Sets the decoder locking mode. LOCK: 00 = Line Locked Mode; 01 = Subcarrier Locked Mode; 10 = Video Input Processor Mode; 11 = D1 Mode
02	3	BLM	**BLL lock mode.** Sets the decoder burst locking mode. BLM: 0 = Frequency Lock; 1 = Phase Lock
02	2	KILD	**Color kill disable.** Color killer is disabled when HIGH.
02	1	DMODBY	**Demod bypass.** Chroma data bypasses the demodulator when HIGH.
02	0	CINT	**C_BC_R interpolation enable.** Interpolation of C_BC_R input data from 0:2:2 to 0:4:4 is enabled when HIGH.

Control Register Definitions (continued)

Chroma Processor Control (03)

7	6	5	4	3	2	1	0
BLFS			CCEN	CCOR		GAUBY	GAUSEL

Reg	Bit	Name	Description
03	7-5	BLFS	**Burst loop filter select.**
03	4	CCEN	**Chroma coring enable.** Enables Chroma Coring when HIGH.
03	3-2	CCOR	**Chroma coring threshold.** Sets the Chroma Coring threshold.
03	1	GAUBY	**Gaussian filter bypass.** The chroma data bypasses the Gaussian LPF when HIGH.
03	0	GAUSEL	**Gaussian LPF select.** Selects the Gaussian filter response to be used on the demodulated chrominance.

BLFS	fs (Mpps)	Recommended Criteria
000	13.5	PAL, Line-Locked YC
000	15	PAL, Line-Locked YC
001	12.27	NTSC, Line-Locked YC
001	13.5	PAL, Line-Locked Composite
010	13.5	NTSC, Line-Locked YC
010	15	PAL, Line-Locked Composite
011	14.32	NTSC, Subcarrier-Locked YC
011	17.73	PAL, Subcarrier-Locked Composite
100	17.73	PAL, Subcarrier-Locked YC
101	13.5	NTSC, Line-Locked Composite
110	12.27	NTSC, Line-Locked Composite
111	14.32	NTSC, Subcarrier-Locked Composite

CCOR	Function
00	1 lsb
01	2 lsb
10	3 lsb
11	4 lsb

GAUSEL	Function
0	Select Gaussian LPF resp. 2
1	Select Gaussian LPF resp. 1

See Figure 6 for filter responses.

Control Register Definitions (continued)

Burst Threshold (04)

7	6	5	4	3	2	1	0
BTH							

Reg	Bit	Name	Description
04	7-0	BTH	**Burst threshold.** The 8 bit value to be compared against the demodulated U and V component data. If over 127 lines occur in a field in which the burst is below this threshold, then the color is set to chroma black for the next field.

Pedestal (05)

7	6	5	4	3	2	1	0
PED							

Reg	Bit	Name	Description
05	7-0	PED	**Pedestal level.** An 8 bit magnitude subtracted from the luma data to remove the setup before processing by the output matrix.

Luma Processor Control (06)

7	6	5	4	3	2	1	0
Reserved		ANEN	ANR	ANT		YSEL	NOTCH

Reg	Bit	Name	Description
06	7-6	Reserved	**Reserved, set to zero.**
06	5	ANEN	**Adaptive notch enable.** Enables adaptive notch when HIGH.
06	4	ANR	**Adaptive notch rounding.** Sets adaptive notch rounding point. ANR: 0 = Round to 10 bits; 1 = Round to 8 bits
06	3-2	ANT	**Adaptive notch threshold level.** Sets the adaptive notch threshold. ANT: 00 = Magnitude difference less than 32; 01 = Magnitude difference less than 24; 10 = Magnitude difference less than 16; 11 = Magnitude difference less than 8
06	1	YSEL	**Adaptive notch select.** Selects adaptive notch filter response. YSEL: 0 = Adaptive notch response ANF1; 1 = Adaptive notch response ANF2
06	0	NOTCH	**Notch enable.** Adaptive notch filter ANF3 selected when HIGH and ANEN is HIGH, non-adaptive notch filter selected when HIGH and ANEN is LOW. Function may be overridden by XSF (Reg 0E, bits 5-4).

Control Register Definitions (continued)

Comb Processor Control (07)

7	6	5	4	3	2	1	0
LS1BY	LS1IN	LS2DLY	SPLIT	BSFBY	BSFSEL	BSFMSB	GRSDLY

Reg	Bit	Name	Description
07	7	LS1BY	**Line store 1 bypass.** Bypasses linestore 1 when HIGH.
07	6	LS1IN	**Line store 1 input.** Selects the input of linestore 1: **LS1IN** = 0: Primary Input **LS1IN** = 1: Secondary Input
07	5	LS2DLY	**Line store 2 delay.** LSTORE2 uses STS to store 1H when LOW and uses VL to store SAV to EAV (or max count) when HIGH.
07	4	SPLIT	**Line store 2 delay.** Splits data through LSTORE2, 9 bits chroma and 7 bits luma when HIGH (chroma combs) and 8 bits chroma and 8 bits luma when LOW (luna combs).
07	3	BSFBY	**Bandsplit filter bypass.** Bandsplit filter is bypassed when HIGH.
07	2	BSFSEL	**Bandsplit filter select.** Selects the bandsplit filter to be used: **BSFSEL** = 0: Select bandsplit filter response 1 **BSFSEL** = 1: Select bandsplit filter response 2
07	1	BSFMSB	**Inverts msb of bandsplit filter.** When HIGH, inverts the msb of the input to the bandsplit filter.
07	0	GRSDLY	**Delays input to GRS decode.** When HIGH, delays the input to the GRS extraction circuit by 1H.

Mid-Sync Level (08)

7	6	5	4	3	2	1	0
MIDS							

Reg	Bit	Name	Description
08	7-0	MIDS	**Mid-sync level.** Sets the mid point of syncs in the mixed sync separator.

Control Register Definitions (continued)

Extended DRS (09)

7	6	5	4	3	2	1	0
PCKF				VSTD			

Reg	Bit	Name	Description
09	7-4	PCKF	**Clock rate.**

PCKF	Function
0000	13.50 MHz
0001	reserved
0010	reserved
0011	reserved
0100	14.32 MHz
0101	17.73 MHz
0110	reserved
0111	reserved
1000	12.27 MHz
1001	14.75 MHz
1010	15.00 MHz
1011	reserved
1100	reserved
1101	reserved
1110	reserved
1111	reserved

Reg	Bit	Name	Description
09	3-0	VSTD	**Video Standard.** Selects the video standard.

VSTD	Function
0000	NTSC-M
0001	NTSC-EIAJ
0010	reserved
0011	reserved
0100	reserved
0101	reserved
0110	reserved
0111	reserved
1000	PAL-B, G, H, I
1001	PAL-M
1010	PAL-N (Argentina, Paraguay, Uruguay)
1011	PAL-N (Jamaica)
1100	reserved
1101	reserved
1110	reserved
1111	reserved

Control Register Definitions (continued)

Output Control (0A)

7	6	5	4	3	2	1	0
OP8B	OPLMT	OPLMT	MSEN		OPCMSB	YBAL	BUREN

Reg	Bit	Name	Description
0A	7	OP8B	**Output rounded to 8 bits.** Rounds the outputs to 8 bits when HIGH. The two lsbs are set to zero.
0A	6-5	OPLMT	**Output limit select.** Sets the output format and limiters:
0A	4-3	MSEN	**Mixed sync enable.** Sets composite sync output format:
0A	2	OPCMSB	**Chroma output msb invert.** Inverts the msb of the C_BC_R or Chroma output when HIGH.
0A	1	YBAL	**Luma color correction.** Setting this bit HIGH forces the chroma to zero whenever the luma equals or exceeds the luma limit.
0A	0	BUREN	**Output burst enable.** When HIGH, passes the burst through on the chroma channel. Sets the burst region to zero when LOW.

OPLMT	Function
00	RGB output format Limited to 0 to 1023
01	YC_BC_R output format Y limited to 0 to 1023 C_BC_R limited to ±511
10	RGB output format Limited to 64 to 940
11	YC_BC_R output format Y limited to 64 to 940 C_BC_R limited to ±448

MSEN	Function
00	No sync
01	No sync
10	Sync on G/Y output only
11	Sync on RGB outputs

Control Register Definitions (continued)

Output Control (0B)

7	6	5	4	3	2	1	0
FMT422	CDEC	YUVT	Reserved			DRSEN	DRSCK

Reg	Bit	Name	Description
0B	7	FMT422	**Enables C_BC_R output mux.** When HIGH, multiplexes the C_B and C_R data onto the same data bus. The chroma or multiplexed C_BC_R output appears on the B/C_B output. The R/C_R output is forced low.
0B	6	CDEC	**C_BC_R decimation enable.** When HIGH, the C_BC_R data are decimated to 0:2:2 in the output processor.
0B	5	YUVT	**Enables D1 output.** When HIGH, enables 4:2:2 multiplexed YC_BC_R onto the R/C_R data output with TRS words inserted into the output data stream. The Y data are still available on the G/Y output and multiplexed C_BC_R is available on the B/U output.
0B	4-2	Reserved	**Reserved, set to zero.**
0B	1	DRSEN	**DRS output enable.** When HIGH, enables the DRS onto the G/Y output.
0B	0	DRSCK	**DRS data rate.** Sets the DRS output data rate.

DRSCK	Function
0	Embeds data bytes (8 bits) at PCK clock rate
1	Embeds data nibbles (4 bits) at PXCK clock rate

Control Register Definitions (continued)

Comb Filter Control (0C)

7	6	5	4	3	2	1	0
ADAPT		YCES	YCSEL	COMB			

Reg	Bit	Name	Description
0C	7-6	ADAPT	**Adaption mode.** Sets the 3-line comb filter adaption mode in NTSC.

ADAPT	Function
00	Adapts to best of 3 types of line comb.
01	3 line comb always adapts to (0H & 1H) comb when the 3 line comb fails
10	3 line comb only. Never adapts to a 2 line comb. The higher of the 2 line comb error signals provides the input to the XLUT
11	Adapts to best of 5 types of line comb.

Reg	Bit	Name	Description
0C	5	YCES	**YC input error signal control.** Error signal control for YC input, luma comb.

YCES	Function
0	LPF and HPF error signal, between (0H & 1H) or (1H & 2H) in NTSC or between (0H & 2H) in PAL,are sent to XLUT
1	LPF error signal, between (0H & 1H) and (1H & 2H) in NTSC or between (0H & 2H) in PAL, are sent to XLUT

Reg	Bit	Name	Description
0C	4	YCSEL	**Luma/chroma comb filter select.** Selects luma or chroma comb filter.

YCSEL	Function
0	Chroma comb filter
1	Luma comb filter

Reg	Bit	Name	Description
0C	3-0	COMB	**Comb filter architecture.**

COMB	Function
YC or composite comb filter architectures	
0000	PAL or NTSC 3 line comb
0001	NTSC 3 line comb (0H & 1H)
0010	NTSC 3 line comb (1H & 2H)
0011	NTSC 2 line comb (0H & 1H)
0100	NTSC (2 line) field comb
0101	NTSC or PAL field comb
0110	NTSC (2 line) frame comb
0111	NTSC or PAL frame comb
D1 comb filter architectures	
1000	3 line comb
1001	3 line comb (0H & 1H)
1010	3 line comb (1H & 2H)
1011	3 line comb (0H & 2H)
1100	(2 line) field comb
1101	field or 2 line (0H & 1H) comb
1110	(2 line) frame comb
1111	frame comb

Control Register Definitions (continued)

Comb Filter Control (0D)

7	6	5	4	3	2	1	0
CEST		CESG	YESG	CESTBY	XFEN	FAST	YWBY

Reg	Bit	Name	Description
0D	7-6	CEST	**Chroma error signal transform.**
0D	5	CESG	**Chroma error signal gain.**
0D	4	YESG	**Luma error signal gain.**
0D	3	CESTBY	**Chroma error signal bypass.** When HIGH, bypasses chroma error signal.
0D	2	XFEN	**XLUT filter enable.** When HIGH, enables the LPF on the XLUT output.
0D	1	FAST	**Adaption speed select.** When HIGH, the 3 line comb filter selects between comb filter architectures on a pixel by pixel basis. When LOW, the selection is filtered.
0D	0	YWBY	**Luma weighting bypass.** When HIGH bypasses the luma fail weighting.

CEST	Video Standard	Clock Rate (MHz)
00	PAL/NTSC	4*Fsc & 13.5MHz
01	NTSC	12.27MHz
10	PAL	14.75MHz
11	PAL	15MHz

CESG	Function
0	Normal chroma fail signal levels
1	Double the chroma error signal levels

YESG	Function
0	Normal luma fail signal levels
1	Double the luma error signal levels

Control Register Definitions (continued)

Comb Filter Control (0E)

7	6	5	4	3	2	1	0
XIP		XSF		YMUX		CMUX	

Reg	Bit	Name	Description
0E	7-6	XIP	**XLUT input select.** Selects the comb fail signals presented to the XLUT:
0E	5-4	XSF	**XLUT special function.**
0E	3-2	YMUX	**Y output select.** Output selection of luma 4:1 mux
0E	1-0	CMUX	**C output select.** Output selection of chroma 4:1 mux

XIP	Input to XLUT
00	2 bits of phase error, 3 bits of chroma error, and 3 bits of luma magnitude error
01	4 bits of chroma and 4 bits of luma magnitude error
10	3 bits of phase error, 3 bits of chroma magnitude error, and 2 bits of luma magnitude error
11	4 bits of phase error and 4 bits of chroma magnitude error

XSF	Luma	Chroma
00	Comb	Simple
01	Simple	Comb
10	Flat with notch	Simple
11	Flat with notch	Comb

YMUX	Output
00	Comb
01	Flat - Comb
10	Flat
11	Simple

CMUX	Output
00	Comb
01	Flat - Comb
10	Flat
11	Simple

Control Register Definitions (continued)

Comb Filter Control (0F)

7	6	5	4	3	2	1	0
Reserved			DCES	IPCF		YCCOMP	SYNC

Reg	Bit	Name	Description
0F	7	Reserved	**Reserved, set to zero.**
0F	6-5	Reserved	**Adaption threshold.** Fixes threshold at which different comb filters are selected. 0 0 5% of max error 0 1 15% of max error 1 0 25% of max error 1 1 50% of max error
0F	4	DCES	**D1 C_BC_R error signal.** When set LOW for D1 chroma comb filters: a) In 3 line comb filter architectures, the magnitude error between the component data for that pixel selects the 3 line comb or adapts to a 2 line comb. On a 'C_B pixel' the error signal selected on pixel (x+4) is sent to the XLUT with the magnitude difference between 'C_R pixels' on the same piar of lines, but from pixel (x+3). Likewise on a 'C_R pixel' the error signal selected on pixel (x+5) is sent to the XLUT with the magnitude difference between 'C_B pixels' on the same lines but from pixel (x+4). b) In 2 line comb filters the magnitude differences between the same pair of lines is always sent to the XLUT, On a 'C_B pixel' the error from the preceding 'C_R pixel' is used and on a 'C_R pixel' the preceding 'C_B pixel' would be used. When set HIGH for D1 chroma filters: This is used for 3 line comb filter architecture that are inhibited from adapting to 2 line comb filter architectures. The input to the XLUT is the magnitude error in C_R between (0H & 1H) and (1H & 2H) on 'C_R pixels' and the magnitude error between (0H & 1H) and (1H & 2H) on 'C_B pixels'.
0F	3-2	IPCF	**Comb filter input select.** Selects primary inputs to the comb filter. IPCF: 0 0 Flat video; 0 1 LPF output; 1 0 HPF output; 1 1 Reserved
0F	1	YCCOMP	**YC or Composite input select.** Selects YC inputs when HIGH and composite inputs when LOW.
0F	0	SYNC	**Sync processor select.** The syncs are obtained by a LPF when HIGH and by the comb filter when LOW.

Sync Pulse Generator (10)

7	6	5	4	3	2	1	0
STS_7	STS_6	STS_5	STS_4	STS_3	STS_2	STS_1	STS_0

Reg	Bit	Name	Description
10	7-0	STS_{7-0}	**Sync to sync 8 lsbs.** Bottom 8 bits of the number of pixels between sync pulses.

Control Register Definitions (continued)

Sync Pulse Generator (11)

7	6	5	4	3	2	1	0
STB							

Reg	Bit	Name	Description
11	7-0	STB	**Sync to burst.** Controls the number of pixels from sync to burst. This signal starts the burst sample and hold. In SC mode, subtract 25 from the desired delay to generate this value.

Sync Pulse Generator (12)

7	6	5	4	3	2	1	0
BTV							

Reg	Bit	Name	Description
12	7-0	BTV	**Burst to video.** Controls the number of pixels from STB to the start of active video.

Sync Pulse Generator (13)

7	6	5	4	3	2	1	0
AV_7	AV_6	AV_5	AV_4	AV_3	AV_2	AV_1	AV_0

Reg	Bit	Name	Description
13	7-0	AV_{7-0}	**Active video line 8 lsbs.** Bottom 8 bits of the number of pixels during the active video line.

Sync Pulse Generator (14)

7	6	5	4	3	2	1	0
Reserved		AV_9	AV_8	Reserved	STS_{10}	STS_9	STS_8

Reg	Bit	Name	Description
14	7-6	Reserved	**Reserved, set to zero.**
14	5-4	AV_{9-8}	**Active video line 2 msbs.** Two most significant bits of AV.
14	3	Reserved	**Reserved, set to zero.**
14	2-0	STS_{10-8}	**Sync to sync 3 msbs.** Three most significant bits of STS.

Control Register Definitions (continued)

Sync Pulse Generator (15)

7	6	5	4	3	2	1	0
Reserved	VINDO					VDIV	VDOV

Reg	Bit	Name	Description
15	7	Reserved	**Reserved, set to zero.**
15	6-2	VINDO	**Number of lines in vertical window.** The number of lines (0 to 31) after the last EQ pulse that the decoder passes through the Vertical INterval winDOw.
15	1	VDIV	**Action inside VINDO.** The vertical data inside the `VINDO' is passed through a simple decoder when LOW, or is passed unprocessed on the luma channel with the chroma channel set to zero when HIGH.
15	0	VDOV	**Action outside VINDO.** The vertical data after the `VINDO' and before the end of vertical blanking is blanked (YUV = 0) when LOW, or passed through the simple decoder when HIGH.

Sync Pulse Generator (16)

7	6	5	4	3	2	1	0
Reserved		NFDLY		SPGIP		MSIP	

Reg	Bit	Name	Description
16	7-6	Reserved	**Reserved, set to zero.**
16	5-4	NFDLY	**new field detect delay.** NTSC frame detect delay:
16	3-2	SPGIP	**SPG input select.** Selects the input to the Sync Pulse Generator:
16	1-0	MSIP	**Mixed sync separator input select.**:

NFDLY	Function
00	pixel count = 0
01	pixel count = 1
10	pixel count = 2
11	pixel count = 3

SPGIP	Input
00	External $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$
01	Digitized sync (subcarrier mode)
10	TRS words embedded in the D1 data stream
11	TRS words embedded in the D2 data stream

MSIP	Input
00	0H offset, input from 0HL
01	1H offset, input from 1HL
10	0H offset, input from INPUT B
11	1H offset, input from INPUT B (external 1H delay)

Control Register Definitions (continued)

Buffered register set 0 (17) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$SG0_7$	$SG0_6$	$SG0_5$	$SG0_4$	$SG0_3$	$SG0_2$	$SG0_1$	$SG0_0$

Reg	Bit	Name	Description
17	7-0	$SG0_{7-0}$	**Msync gain, 8 lsbs.** Bottom 8 bits of mixed sync scalar lsb = 1/256

Buffered register set 0 (18) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$YG0_7$	$YG0_6$	$YG0_5$	$YG0_4$	$YG0_3$	$YG0_2$	$YG0_1$	$YG0_0$

Reg	Bit	Name	Description
18	7-0	$YG0_{7-0}$	**Y gain, 8 lsbs.** Bottom 8 bits of the luma gain lsb = 1/256

Buffered register set 0 (19) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$UG0_7$	$UG0_6$	$UG0_5$	$UG0_4$	$UG0_3$	$UG0_2$	$UG0_1$	$UG0_0$

Reg	Bit	Name	Description
19	7-0	$UG0_{7-0}$	**U gain, 8 lsbs.** Bottom 8 bits of the U gain lsb = 1/256

Buffered register set 0 (1A) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$VG0_7$	$VG0_6$	$VG0_5$	$VG0_4$	$VG0_3$	$VG0_2$	$VG0_1$	$VG0_0$

Reg	Bit	Name	Description
1A	7-0	$VG0_{7-0}$	**V gain, 8 lsbs.** Bottom 8 bits of the V gain lsb = 1/256

Buffered register set 0 (1B) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$YG0_9$	$YG0_6$	$UG0_{10}$	$UG0_9$	$UG0_8$	Reserved	$VG0_9$	$VG0_8$

Reg	Bit	Name	Description
1B	7-6	$YG0_{9-8}$	**Y gain, 2 msb.** Top 2 bits of the Y gain. msb = 2
1B	5-3	$UG0_{10-8}$	**U gain, 3 msbs.** Top 3 bits of the U gain.msb = 4
1B	2	Reserved	**Reserved, set to zero.**
1B	1-0	$VG0_{9-8}$	**V gain, 2 msbs.** Top 2 bits of the V gain. msb = 2

Control Register Definitions (continued)

Buffered register set 0 (1C) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$YOFF0_7$	$YOFF0_6$	$YOFF0_5$	$YOFF0_4$	$YOFF0_3$	$YOFF0_2$	$YOFF0_1$	$YOFF0_0$

Reg	Bit	Name	Description
1C	7-0	$YOFF0_{7-0}$	**Y offset, 8 lsbs.** Bottom 8 bits of luma or RGB offset

Buffered register set 0 (1D) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
Reserved					$YOFF0_8$	$SG0_1$	$SG0_0$

Reg	Bit	Name	Description
1D	7-3	Reserved	**Reserved, set to zero.**
1D	2	$YOFF0_8$	**Y offset, msb.** msb of YOFF
1D	1-0	$SG0_{1-0}$	**Msync gain, 2 msbs.** Top 2 bits of mixed sync scalar. msb = 2

Buffered register set 0 (1E) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$SYSPH0_7$	$SYSPH0_6$	$SYSPH0_5$	$SYSPH0_4$	$SYSPH0_3$	$SYSPH0_2$	$SYSPH0_1$	$SYSPH0_0$

Reg	Bit	Name	Description
1E	7-0	$SYSPH0_{7-0}$	**8 lsbs of phase.** Bottom 8 bits of the system phase offset

Buffered register set 0 (1F) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$SYSPH0_{15}$	$SYSPH0_{14}$	$SYSPH0_{13}$	$SYSPH0_{12}$	$SYSPH0_{11}$	$SYSPH0_{10}$	$SYSPH0_9$	$SYSPH0_8$

Reg	Bit	Name	Description
1F	7-0	$SYSPH0_{15-8}$	**8 msbs of phase.** Top 8 bits of the system phase offset

Normalized Subcarrier Frequency (20)

7	6	5	4	3	2	1	0
FSC_3	FSC_2	FSC_1	FSC_0	Reserved			

Reg	Bit	Name	Description
20	7-4	FSC_{3-0}	**Bottom 4 bits of fsc.** Bottom 4 bits of the 28 bit subcarrier SEED
20	3-0	Reserved	**Reserved, set to zero.**

Control Register Definitions (continued)

Normalized Subcarrier Frequency (21)

7	6	5	4	3	2	1	0
FSC_{11}	FSC_{10}	FSC_9	FSC_8	FSC_7	FSC_6	FSC_5	FSC_4

Reg	Bit	Name	Description
21	7-0	FSC_{11-4}	**Lower 8 bits of fsc.** Lower 8 bits of the 28 bit subcarrier SEED

Normalized Subcarrier Frequency (22)

7	6	5	4	3	2	1	0
FSC_{19}	FSC_{18}	FSC_{17}	FSC_{16}	FSC_{15}	FSC_{14}	FSC_{13}	FSC_{12}

Reg	Bit	Name	Description
22	7-0	FSC_{19-12}	**Middle 8 bits of fsc.** Middle 8 bits of the 28 bit subcarrier SEED

Normalized Subcarrier Frequency (23)

7	6	5	4	3	2	1	0
FSC_{27}	FSC_{26}	FSC_{25}	FSC_{24}	FSC_{23}	FSC_{22}	FSC_{21}	FSC_{20}

Reg	Bit	Name	Description
23	7-0	FSC_{27-20}	**Top 8 bits of fsc.** Top 8 bits of the 28 bit subcarrier SEED

Normalized Subcarrier Frequency (24-25)

7	6	5	4	3	2	1	0
Reserved							

Reg	Bit	Name	Description
24-25	7-0	Reserved	**Reserved, set to zero.**

Control Register Definitions (continued)

Output Format Control (26)

7	6	5	4	3	2	1	0
Reserved		LDVIO	OPCKS	DPCEN	DPC		

Reg	Bit	Name	Description
26	7-6	Reserved	**Reserved, set to zero.**
26	5	LDVIO	**LDV clock select.** LDV is an output when LOW and an input when HIGH
26	4	OPCKS	**Output clock select.** The output data are clocked by the CLOCK pin when LOW and by the LDV pin when HIGH.
26	3	DPCEN	**DPC enable.** When HIGH on the TMC22153, the Decoder Product Code is enabled: a value written into DPC determines the decoder product emulated by the TMC22153. In all other versions of the decoder, DPC is read-only, and returns the code of the particular encoder version installed.
26	2-0	DPC	**Decoder product code** DPC / Function 000 Reserved 001 TMC22051 010 TMC22052 011 TMC22053 100 Reserved 101 TMC22151 110 TMC22152 111 TMC22153 Read/Write in the TMC22153 only. Read-only in all other devices.

Buffered register set 1 (27) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
$SG1_7$	$SG1_6$	$SG1_5$	$SG1_4$	$SG1_3$	$SG1_2$	$SG1_1$	$SG1_0$

Reg	Bit	Name	Description
27	7-0	$SG1_{7-0}$	**Msync gain, 8 lsbs.** Bottom 8 bits of mixed sync scalar lsb = 1/256

Buffered register set 1 (28) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
$YG1_7$	$YG1_6$	$YG1_5$	$YG1_4$	$YG1_3$	$YG1_2$	$YG1_1$	$YG1_0$

Reg	Bit	Name	Description
28	7-0	$YG1_{7-0}$	**Y gain, 8 lsbs.** Bottom 8 bits of the luma gain lsb = 1/256

Preliminary Information

Control Register Definitions (continued)

Buffered register set 1 (29) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
$UG1_7$	$UG1_6$	$UG1_5$	$UG1_4$	$UG1_3$	$UG1_2$	$UG1_1$	$UG1_0$

Reg	Bit	Name	Description
29	7-0	$UG1_{7-0}$	**U gain, 8 lsbs.** Bottom 8 bits of the U gain lsb = 1/256

Buffered register set 1 (2A) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
$VG1_7$	$VG1_6$	$VG1_5$	$VG1_4$	$VG1_3$	$VG1_2$	$VG1_1$	$VG1_0$

Reg	Bit	Name	Description
2A	7-0	$VG1_{7-0}$	**V gain, 8 lsbs.** Bottom 8 bits of the V gain lsb = 1/256

Buffered register set 1 (2B) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
$YG1_9$	$YG1_8$	$UG1_{10}$	$UG1_9$	$UG1_8$	Reserved	$VG1_9$	$VG1_8$

Reg	Bit	Name	Description
2B	7-6	$YG1_{9-8}$	**Y gain, 2 msbs.** Top 2 bits of the Y gain msb = 2
2B	5-3	$UG1_{10-8}$	**U gain, 3 msbs.** Top 3 bits of the U gain. msb = 4
2B	2	Reserved	**reserved, set to zero**
2B	1-0	$VG1_{9-8}$	**V gain, 2 msbs.** Top 2 bits of the V gain msb = 2

Buffered register set 1 (2C) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
$YOFF1_7$	$YOFF1_6$	$YOFF1_5$	$YOFF1_4$	$YOFF1_3$	$YOFF1_2$	$YOFF1_1$	$YOFF1_0$

Reg	Bit	Name	Description
2C	7-0	$YOFF1_{7-0}$	**Y offset, 8 lsbs.** Bottom 8 bits of luma or RGB offset

Control Register Definitions (continued)

Buffered register set 1 (2D) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
Reserved					$YOFF1_8$	$SG1_7$	$SG1_0$

Reg	Bit	Name	Description
2D	7-3	Reserved	**Reserved, set to zero.**
2D	2	$YOFF1_8$	**Y offset, msb.** msb of YOFF
2D	1-0	$SG1_{7-0}$	**Msync gain, 2 msbs.** Top 2 bits of mixed sync scalar msb = 2

Buffered register set 1 (2E) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
$SYSPH1_7$	$SYSPH1_6$	$SYSPH1_5$	$SYSPH1_4$	$SYSPH1_3$	$SYSPH1_2$	$SYSPH1_1$	$SYSPH1_0$

Reg	Bit	Name	Description
2E	7-0	$SYSPH1_{7-0}$	**8 lsbs of phase.** Bottom 8 bits of the system phase offset

Buffered register set 1 (2F) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
$SYSPH1_{15}$	$SYSPH1_{14}$	$SYSPH1_{13}$	$SYSPH1_{12}$	$SYSPH1_{11}$	$SYSPH1_{10}$	$SYSPH1_9$	$SYSPH1_8$

Reg	Bit	Name	Description
2F	7-0	$SYSPH1_{15-8}$	**8 msbs of phase.** Top 8 bits of the system phase offset

Control Register Definitions (continued)

Video Measurement (30)

7	6	5	4	3	2	1	0
Reserved	LGF	LGEN	LGEXT	RESERVED	PGG	PGEN	PGEXT

Reg	Bit	Name	Description
30	7	Reserved	**Reserved, set to zero.**
30	6	LGF	**Line grab flag.** Set HIGH when the decoder has grabbed a line, and must be reset LOW before another line can be grabbed.
30	5	LGEN	**Line grab enable.** When HIGH, the line grabber is used to freeze the contents of the line store, at the programmed line and field count. The phase and frequency of the frozen line are also stored from the DRS, and are continually used to reset the DDS, once per line, until LGF is set LOW. When LGEN is LOW, the line freeze is disabled, the internal loops operate normally, and the line grab signal is used only to gate the pixel grab.
30	4	LGEXT	**Ext line grab enable.** The SET pin is used to produce the line grabber pulse when HIGH and the internal line decode is used when LGEXT is LOW.
30	3	Reserved	**Reserved, set to zero.**
30	2	PGG	**Pixel grab gate.** When HIGH the pixel grab is gated by the field and line grab signals to enable one pixel per four fields in NTSC and 8 field in PAL to be grabbed. This function is disabled if PGEN is set LOW.
30	1	PGEN	**Pixel grab enable.** When HIGH the 10 bit G/Y, B/U, and R/V data, and the mixed sync and luma data after the comb filter, and the demodulated (B-Y) and (R-Y) color difference signals are grabbed once every line at the programmed pixel grab number. When LOW the contents of the pixel grab registers are held and the pixel grab pulse is ignored.
30	0	PGEXT	**Ext pixel grab enable.** The SET pin is used to produce the pixel grab pulse when HIGH and the internal pixel decode is used when PGEXT is LOW.

Video Measurement (31)

7	6	5	4	3	2	1	0
PG_7	PG_6	PG_5	PG_4	PG_3	PG_2	PG_1	PG_0

Reg	Bit	Name	Description
31	7-0	PG_{7-0}	**Pixel grab, 8 lsbs.** Bottom 8 bits of the pixel grab.

Video Measurement (32)

7	6	5	4	3	2	1	0
LG_7	LG_6	LG_5	LG_4	LG_3	LG_2	LG_1	LG_0

Reg	Bit	Name	Description
32	7-0	LG_{7-0}	**Line grab, 8 lsbs.** Bottom 8 bits of the line grab.

Control Register Definitions (continued)

Video Measurement (33)

7	6	5	4	3	2	1	0
Reserved	FG			LG_8	PG_{10}	PG_9	PG_8

Reg	Bit	Name	Description
33	7	Reserved	**Reserved.**
33	6-4	FG	**Field grab number.** Field grab number
33	3	LG_8	**Msb of line grab.** msb of line grab
33	2-0	PG_{10-8}	**Pixel grab, 3 msbs.** 3 msbs of pixel grab

Registers 34-3C are Read-Only

Register (34)

7	6	5	4	3	2	1	0
GY_9	GY_8	GY_7	GY_6	GY_5	GY_4	GY_3	GY_2

Reg	Bit	Name	Description
34	7-0	GY_{9-2}	**G/Y grab, 8 msbs.** Top 8 bits of the "grabbed" G/Y data

Register (35)

7	6	5	4	3	2	1	0
BU_9	BU_8	BU_7	BU_6	BU_5	BU_4	BU_3	BU_2

Reg	Bit	Name	Description
35	7-0	BU_{9-2}	**B/U grab, 8 msbs.** Top 8 bits of the "grabbed" B/U data

Register (36)

7	6	5	4	3	2	1	0
RV_9	RV_8	RV_7	RV_6	RV_5	RV_4	RV_3	RV_2

Reg	Bit	Name	Description
36	7-0	RV_{9-2}	**R/V grab, 8 msbs.** Top 8 bits of the "grabbed" R/V data

Register (37)

7	6	5	4	3	2	1	0
Reserved		GY_1	GY_0	BU_1	BU_0	RV_1	RV_0

Reg	Bit	Name	Description
37	7-6	Reserved	**Reserved.**
37	5-4	GY_{1-0}	**G/Y grab, 2 lsbs.** Bottom two bits of G/Y data
37	3-2	BU_{1-0}	**B/U grab, 2 lsbs.** Bottom two bits of B/U data
37	1-0	RV_{1-0}	**R/V grab, 2 lsbs.** Bottom two bits of R/V data

Control Register Definitions (continued)

Register (38)

7	6	5	4	3	2	1	0
Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2

Reg	Bit	Name	Description
38	7-0	Y_{9-2}	**Luma grab, 8 msbs.** Top 8 bits of the "grabbed" luma data after YPROC

Register (39)

7	6	5	4	3	2	1	0
M_9	M_8	M_7	M_6	M_5	M_4	M_3	M_2

Reg	Bit	Name	Description
39	7-0	M_{9-2}	**Msync grab, 8 msbs.** Top 8 bits of the "grabbed" mixed sync data after YPROC

Register (3A)

7	6	5	4	3	2	1	0
U_9	U_8	U_7	U_6	U_5	U_4	U_3	U_2

Reg	Bit	Name	Description
3A	7-0	U_{9-2}	**U grab, 8 msbs.** Top 8 bits of the "grabbed" U data

Register (3B)

7	6	5	4	3	2	1	0
V_9	V_8	V_7	V_6	V_5	V_4	V_3	V_2

Reg	Bit	Name	Description
3B	7-0	V_{9-2}	**V grab, 8 msbs.** Top 8 bits of the "grabbed" V data

Register (3C)

7	6	5	4	3	2	1	0
Y_1	Y_0	M_1	M_0	U_1	U_0	V_1	V_0

Reg	Bit	Name	Description
3C	7-6	Y_{1-0}	**Luma grab, 2 lsbs.** Bottom 2 bits of luma data
3C	5-4	M_{1-0}	**Msync grab, 2 lsbs.** Bottom 2 bits of mixed sync data
3C	3-2	U_{1-0}	**U grab, 2 lsbs.** Bottom 2 bits of U data
3C	1-0	V_{1-0}	**V grab, 2 lsbs.** Bottom 2 bits of V data

Control Register Definitions (continued)

Test Control (3D-3F)

7	6	5	4	3	2	1	0
TEST							

Reg	Bit	Name	Description
3D-3F	7-0	TEST	**Must be set to zero.** Auto increment stops at 3F

Status - Read Only (40)

7	6	5	4	3	2	1	0
DDSPH							

Reg	Bit	Name	Description
40	7-0	DDSPH	**DDS phase, 8 msbs.** The top 8 bits of the sine data generated in the internal DDS.

Status - Read Only (41)

7	6	5	4	3	2	1	0
LINEST	BGST	VACT2	PALODD	VFLY	FGRAB	LGRAB	PGRAB

Reg	Bit	Name	Description
41	7	LINEST	**Pixel count reset.** Pixel count reset
41	6	BGST	**Start of burst gate.** Start of burst gate
41	5	VACT2	**Half line flag.** Half line flag
41	4	PALODD	**PAL Ident.** PAL Ident (low on NTSC lines)
41	3	VFLY	**Vertical count reset.** Vertical count reset
41	2	FGRAB	**Field grab.** Field grab
41	1	LGRAB	**Line grab.** Line grab
41	0	PGRAB	**Pixel grab.** Pixel grab

Status - Read Only (42)

7	6	5	4	3	2	1	0
FLD	$\overline{\text{VBLK}}$	$\overline{\text{HBLK}}$	LID				

Reg	Bit	Name	Description
42	7	FLD	**Field flag (F in D1 output).** Field flag (F in D1 output)
42	6	$\overline{\text{VBLK}}$	**Vertical blanking (V in D1 output).** Vertical blanking (V in D1 output)
42	5	$\overline{\text{HBLK}}$	**Horizontal blanking (H in D1 output).** Horizontal blanking (H in D1 output)
42	4-0	LID	**Line identification.** Line identification

Control Register Definitions (continued)

Status - Read Only (43)

7	6	5	4	3	2	1	0
YGO	YGU	UBO	UBU	VRO	VRU	Reserved	

Reg	Bit	Name	Description
43	7	YGO	**Y/G overflow.** Y/G overflow
43	6	YGU	**Y/G underflow.** Y/G underflow
43	5	UBO	**C_B/B overflow.** C_B/B overflow
43	4	UBU	**C_B/B underflow.** C_B/B underflow
43	3	VRO	**C_R/R overflow.** C_R/R overflow
43	2	VRU	**C_R/R underflow.** C_R/R underflow
43	1-0	Reserved	**Reserved.**

Status - Read Only (44)

7	6	5	4	3	2	1	0
MONO	FPERR						

Reg	Bit	Name	Description
44	7	MONO	**Color kill active.** Color kill active
44	6-0	FPERR	**Frequency/Phase error.** Magnitude of the frequency or phase error. Reported once per line.

Status - Read Only (45)

7	6	5	4	3	2	1	0
DRS							

Reg	Bit	Name	Description
45	7-0	DRS	**DRS signal.** The 8-bit Decoder Reference Signal.

Status - Read Only (46)

7	6	5	4	3	2	1	0
PARTID							

Reg	Bit	Name	Description
46	7-0	PARTID	**Part family ID.** Reads back the 8-bit part ID number. Read-only. Returns CDh.

Control Register Definitions (continued)

Status - Read Only (47)

7	6	5	4	3	2	1	0
REVID							

Reg	Bit	Name	Description
47	7-0	REVID	**Revision number.** The 8-bit chip revision number.

Status - Read Only (48-4A)

7	6	5	4	3	2	1	0
Reserved							

Reg	Bit	Name	Description
48-4A	7-0	Reserved	**Reserved.**

Status - Read Only (4B)

7	6	5	4	3	2	1	0
$\overline{\text{PKILL}}$	CFSTAT		XOP				

Reg	Bit	Name	Description
4B	7	$\overline{\text{PKILL}}$	**Phase kill from comb fail.** Phase kill from comb fail.
4B	6-5	CFSTAT	**Comb filter status.** Comb filter status.
4B	4-0	XOP	**XLUT output.** XLUT output.

CFSTAT	STATUS
00	3 tap comb
01	3 tap [lower] comb
10	3-tap [upper] comb
11	2 tap comb

Status - Read Only (4C-FF)

7	6	5	4	3	2	1	0
Reserved							

Reg	Bit	Name	Description
4C-FF	7-0	Reserved	**Reserved.**

Functional Description

Input Processor

The input processor selects between the two external video sources on VIDEO A and VIDEO B. If the TRS stripper or GRS stacker is active, then the user must select the input with either the GRS (in genlock mode) or with the embedded TRS words as output VA. If the input data are separate luma and chroma or Y and C_BC_R data the input processor must be programmed to put the chrominance or C_BC_R onto output VB and the luminance or Y onto VA.

To ensure that the chrominance data or the C_BC_R data are in two's complement arithmetic format, the register bit MSBI inverts the msb of the DB input. For composite inputs, the IPCMSB register bit should be set LOW, as the ABMUX register bit is used to select the input(s) to the comb filter.

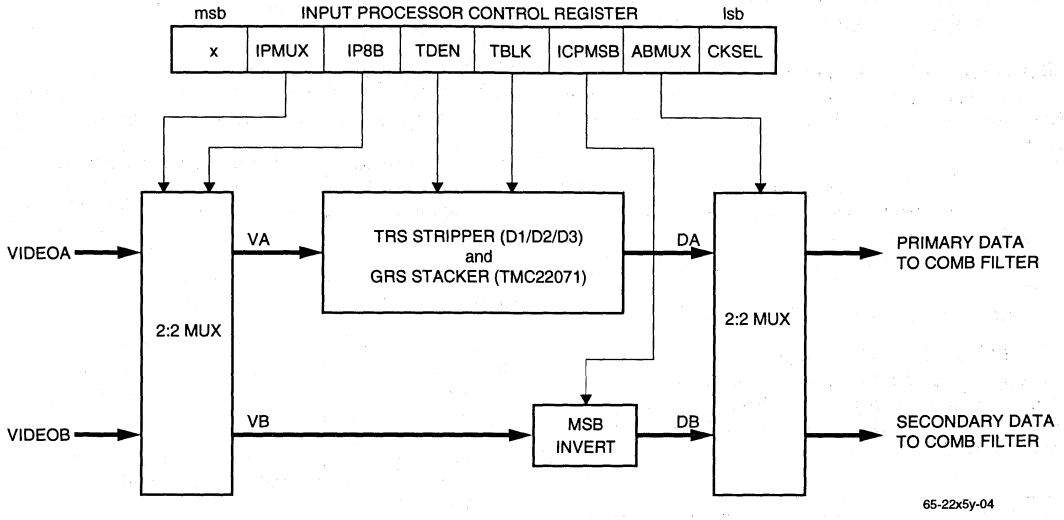


Figure 3. Input Processor

Sync Pulse Generator

The vertical and horizontal references to the decoder can be from external VSYNC and HSYNC pulses, decoded from TRS and TRS-ID words, or from the internal sync separator which extracts the sync information from the digitized input video.

The sync pulse generator (SPG) provides all the clock and enable pulses required to synchronize the decoder operation to the incoming video signal. These pulses are described below, along with the microprocessor data required to control them.

Internal field and line numbering scheme

The internal line numbering of the digital decoder differs from the standard video line numbering as shown in the following tables. The internal line numbers for a 3 line comb advance the numbering by 1 line with respect to the input, but are identical with respect to the internally one line delayed decoded video.

Table 2. NTSC field and line numbering

Standard Field #	Standard Line #	Internal Field #	Internal Line #
1 & 3	1 - 3	1 & 3	260 - 262
1 & 3	4 - 263	0 & 2	0 - 259
2 & 4	264 - 265	0 & 2	260 - 261
2 & 4	266 - 525	1 & 3	0 - 259

Table 3. PAL B, G, H, I field and line numbering

Standard Field #	Standard Line #	Internal Field #	Internal Line #
1 & 5	1 - 312	0 & 4	0 - 311
2 & 6	313 - 625	1 & 5	0 - 312
3 & 7	626 - 937	2 & 6	0 - 311
4 & 8	938 - 1250	3 & 7	0 - 312

Table 4. PAL M field and line numbering

Standard Field #	Standard Line #	Internal Field #	Internal Line #
1 & 5	1 - 262	0 & 2	0 - 261
2 & 6	263 - 525	1 & 3	0 - 262
3 & 7	1 - 262	0 & 2	0 - 261
4 & 8	263 - 525	1 & 3	0 - 262

HSTBG (Burst gate)[1]
The burst gate starts the 16 clock period average of the demodulated burst envelope. The position of the burst gate is programmed into a register as the number of clock periods from the falling edge of sync to the burst envelope.

$\overline{\text{HBLK}}$ (Horizontal blanking period) [1]
The horizontal blanking period is LOW between the start of SAV and the end of EAV. This signal is used in the following places:

- To clear the SYSPH offset when LOW, this is required for correct operation of the subcarrier phase locked loop
- To aid in the comb filter management
- To remove the burst envelope on the demodulated UV data
- To remove the syncs on the BLUE and RED outputs

$\overline{\text{BBLK}}$ (Vertical burst blanking period)
The vertical burst blanking blanks the lines with no burst from the burst phase locked loop. This signal is decoded from the line ident, $\text{LID}_{4\text{-}0}$, and is modified by the video standard and the field count.

$\overline{\text{MBLK}}$ (Mixed blanking)
This signal is used in the matrix to switch between the sync scalar and the luma scalar. The $\overline{\text{MBLK}}$ signal is active whenever $\overline{\text{HBLK}}$ is active or becomes active when $\overline{\text{VBLK}}$ becomes active. $\overline{\text{MBLK}}$ is also active in PAL on line 310 when both VACT1 and FLD are HIGH and in NTSC and PAL M on line 259 when VACT2 is HIGH and FLD is LOW.

FLD*
The FLD is LOW for field 1 and HIGH for field 2.

$\text{LID}_{4\text{-}0}$[1]
The line ID signals are used in the vertical comb filter management to control the comb filter on the leading and trailing lines of active video around the vertical blanking period, to start and stop the VINDO operation, and in generating the vertical blanking and burst blanking periods.

VACT2[1]
VACT2 is HIGH during the second half of all active lines.

GRABF[1]
The GRABF signal goes HIGH when the internal field count is equal to the programmed field number for the GRAB operation. f a pixel grab is being, this signal is held HIGH to not inhibit the GRABS signal on each line.

GRABL[1]
The GRABL signal goes HIGH when the internal line count is equal to the programmed line number for the GRAB operation. If a pixel grab is being performed, this signal is held HIGH to not inhibit the GRABS signal on each line.

GRABP*
The GRABP signal goes HIGH when the internal pixel count is equal to the programmed pixel number for the GRAB operation.

$\overline{\text{DVSYNC}}$ and $\overline{\text{DHSYNC}}$ (output pins)
The $\overline{\text{DVSYNC}}$ and $\overline{\text{DHSYNC}}$ signals are active when GCR_2 is LOW. When GCR_2 is HIGH these signals are three stated.

Three line comb based decoders have an inherent line delay, therefore the input $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$ signals can not be just delayed by a few registers and output as $\overline{\text{DVSYNC}}$ and $\overline{\text{DHSYNC}}$: they need to be delayed by one complete line. In all other comb filter configurations the $\overline{\text{DVSYNC}}$ and $\overline{\text{DHSYNC}}$ are referenced to the input data (0HFLAT) and not the output of the LSTORE1, i.e. 1HFLAT.

The duration of the $\overline{\text{DVSYNC}}$ signal is fixed to one line and the duration of the $\overline{\text{DHSYNC}}$ signal is 64 clock periods. Both these signals are generated by the internal horizontal and vertical state machines.

The falling edge of these signals relative to the data matches the requirements of the TMC22x91 family of digital encoders.

AVOUT Active video (output pin)
The decoder produces an active video signal starting 4 PCK before the programmed start of active video and ending 4 PCK after the programmed end of active video. This signal is used in both the video mixer (TMC22x8x) family and the digital encoder (TMC22x9x) family. The end points of this signal are flagged by the internally generated SAV and EAV signals.

$\overline{\text{VBLK}}$ (Vertical blanking period)[1]
The vertical blanking period conforms to the CCIR656 specification for D1 component data streams. This signal is decoded from the line ident, $\text{LID}_{4\text{-}0}$, and is active low.

[1] Signal is available over the microprocessor bus.

Table 5. Vertical Blanking Period

NTSC	Internal field no	Internal line no
	0,2	0 - 5
		260 & 261
	1,3	0 - 6
		260 - 262
PAL	**Internal field no**	**Internal line no**
	0, 2, 4, & 6	0 - 21
		310 & 311
	1, 3, 5, & 7	0 - 22
		311 & 312
PAL-M	**Internal field no**	**Internal line no**
	0, 2, 4, & 6	0 - 5
		260 & 261
	1, 3, 5, & 7	0 - 6
		260 & 262

$\overline{BBLK}$ (Vertical burst blanking period)
The vertical burst blanking blanks the lines with no burst from the burst phase locked loop. This signal is controlled by the video standard and the field count. The burst blanking signal is active low.

Table 6. Vertical Burst Blanking Period

NTSC	Internal field #	Internal line #
	0,2	0 - 5
		259 - 261
	1,3	0 - 6
		260 - 262
PAL	**Internal field #**	**Internal line #**
	0 & 4	0 - 5
		309 - 311
	1 & 5	0 - 5
		309 - 312
	2 & 6	0 - 4
		310 & 311
	3 & 7	0 - 6
		310 - 312

Table 6. Vertical Burst Blanking Period

PAL-M	Internal field #	Internal line #
	0 & 4	0 - 7
		259 - 261
	1 & 5	0 - 7
		259 - 262
	2 & 6	0 - 6
		258 & 261
	3 & 7	0 - 6
		260 - 262

LID_{4-0} List of line idents
The line numbers required to produce all the decoder control signals are summarized in Table 7.

Table 7. Line Idents

Line Number	LID_{4-0}
0	00
1–4	01
5	02
6	03
7	04
8	05
9–16	06
17	07
18	08
19–21	09
22	0A
23	0B
24	0C
25–257	0D
258	0E
259	0F
260–261	10
262	11
263–307	12
308	13
309	14
310	15
311	16
312	17

Comb Processor

The comb processor contains the line stores and bandsplit filters required to produce the inputs to the adaptive comb filter.

LSTORE1

The primary comb filter input, INPUTA, is passed through line store 1 when the LS1BY register bit is LOW, as would be the case for all line-based comb filters. For frame- and field-based comb filters the secondary input, INPUTB, is passed through line store 1 when LS1IN is set HIGH. For NTSC frame- and field-based comb filters the LS1IN register bit is set HIGH to allow VIDEOB to bypass line store 1. LSTORE1 is also used to grab a line of video.

LSTORE2

LSTORE2 is actually two line stores, LSTORE 2HH and LSTORE 2HL. For chroma comb filters, LSTORE2 2HH is used to delay the output of the 1H high pass filter and LSTORE2 1HL is used to delay the output of the 1H low pass filter. For luma combs, the composite waveform needs to be delayed and requires one additional bit of headroom. Therefore, LSTORE 2HH delays the top bits of the bypassed 1H high pass filter and LSTORE 2HL delays the bottom bits of the bypassed 1H high pass filter. This operation is controlled by the SPLIT register bit.

The maximum length of LSTORE 2HH and LSTORE 2HL is fixed at 960 pixels. If the line length is greater than this number, as would be the case in PAL four times subcarrier, only the active video portion of the video line is stored.

Bandsplit filter (BSF)

The complementary Band Split Filter (BSF) separates the baseband composite video into two bands by passing it through a low pass filter and subtracting the low pass (luminance) data from the composite video to produce the high-pass (chrominance) data. The complementary filter technique ensures that none of the baseband signal is lost even though it may have been incorrectly separated into luma (cross-color) and chroma (cross-luma) signals.

As the base bandwidths and subcarrier frequencies of the different NTSC and PAL video formats are so different, and the decoder has to be capable of working over a large range of clock frequencies, it is necessary to have two selectable low pass filters (Figure 4, Figure 5). These filters are selectable by the BSFSEL register bit and are independent of the video standard selected.

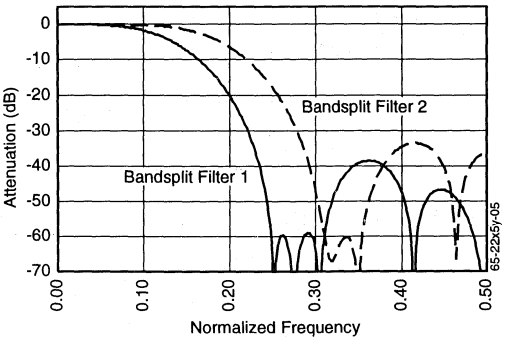


Figure 4. Bandsplit Filter, Full Spectrum Response

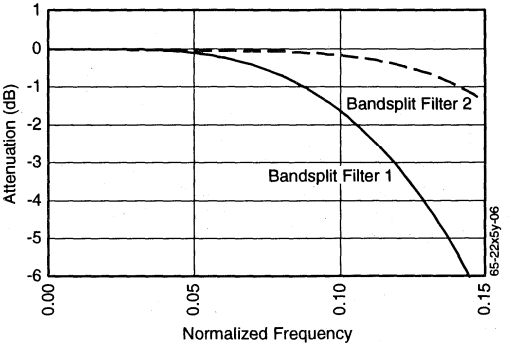


Figure 5. Bandsplit Filter, Passband Response

Table 8. Normalized Subcarrier Frequencies

Pixel Rate (MHz)	Normalized fSC	Comments
12.27	0.2917	NTSC square pixel rate
13.50	0.2652	NTSC D1 pixel rate
13.50	0.3284	PAL D1 pixel rate
14.32	0.2500	NTSC four times subcarrier (D2/D3)
14.75	0.3006	PAL square pixel rate
15.00	0.2956	PAL square pixel rate
17.73	0.2500	PAL four time subcarrier (D2/D3)

Adaptive Comb Filter

The comb filter architecture performs chrominance or luminance comb filtering on PAL or NTSC video signals.

The TMC22x5y performs 16 independent chroma and luma comb filter algorithms. The comb filter configuration is determined by the $COMB_{3-0}$ register bits (Table 9).

The primary input to the comb filter is controlled by $IPCF_{1-0}$, and can be the HPF output on line x (xHH), flat video on line x (xHF), or the LPF output on line x (xHL). The combed video is weighted within the comb filter to allow complementary mixing with the output of the simple (band split) decoder. The mix between these two decoder outputs is controlled by either a register bit or by the instantaneous magnitude of the comb fail detect circuit.

In NTSC it is possible to switch from a 3 line comb to a 2 line comb, and then to a simple decoder output. The 3 line comb to 2 line comb switch can be disabled, forcing the 3 line comb to switch directly to simple. The switching between these two comb architectures is independent of the mix signal, K.

For 3-line Y/C comb filters, an external 1H delay is required in the uncombed channel to compensate for the comb filter delay.

This principle is equally true for NTSC frame and field based comb decoders. The feature is not available for any of the PAL comb filter architectures.

Table 9. Comb filter architectures

$COMB_{3-0}$	Comb Filter Description
0	YC or Composite, PAL or NTSC, 3 line comb
1	YC or Composite, NTSC, 3 line comb (0H & 1H)
2	YC or Composite, NTSC, 3 line comb (1H & 2H)
3	YC or Composite, NTSC, 2 line comb (0H & 1H)
4	YC or Composite, NTSC, (2 line) field comb
5	YC or Composite, NTSC or PAL, field comb
6	YC or Composite, NTSC, (2 line) frame comb
7	YC or Composite, NTSC or PAL, frame comb
8	D1, Y or C_BC_R, 3 line comb
9	D1, Y or C_BC_R, 3 line comb (0H & 1H)
10	D1, Y or C_BC_R, 3 line comb (1H & 2H)
11	D1, Y or C_BC_R, 3 line comb (0H & 2H)
12	D1, Y or C_BC_R, (2 line) field comb
13	D1, Y or C_BC_R, field or 2 line comb (0H & 1H)
14	D1, Y or C_BC_R, (2 line) frame comb
15	D1, Y or C_BC_R, Frame

Comb Fail Detection

The inputs to the comb filter are monitored to detect discontinuities that would cause the comb filter operation to fail. Whenever a significant failure is predicted, the comb filter architecture is modified and an error signal proportional to the discontinuity is produced.

A comb filter will fail to some extent whenever there are vertical transitions in the video signal. For example, a single line transition from yellow to blue will result in a severe comb fail. This type of transition without adaption causes vertical smearing of the picture. For flat areas of color, it is a relatively simple to produce an error signal that switches between the outputs of the comb filter and the simple band split filter without visibly softening the picture horizontally or vertically. However, as horizontal frequencies increase during vertical transitions, so the decision for switching between the comb and simple bandsplit decoder becomes more complex.

To aid in this decision making process, comprehensive comb fail signals are generated and fed to a user-programmable lookup table(XLUT). The output of the lookup table provides the control for the cross fade between the comb and simple bandsplit decoder.

The TMC22x53 comb filter architecture has three taps. These taps are three consecutive field lines in a line based comb, three consecutive picture lines in a field based comb, or lines that are one frame and one field line apart in the frame based comb. In addition to these different inputs to the comb filter, NTSC and PAL video signals comb over different taps in different architectures.

Chroma comb fail

In the past, comb decoders have relied upon comparing the difference in chroma magnitude between two lines to determine a comb fail. In fact, this chroma signal is normally the output of the high-pass or band-pass filter, and therefore contains all the high frequency luminance information as well. As this signal was never demodulated, the sign bit was immaterial and was used only to rectify the chroma signal. This allowed chroma signals which where equal in magnitude but opposite in phase, and high frequency luminance signals, to fool the comb fail circuit.

In the TMC22x5y a new, innovative approach has been developed to overcome this problem. To detect comb failures in the high-frequency portion of the video signal the outputs from the three high-pass filters, 0HH, 1HH, and 2HH, are passed through simple demodulators. The outputs from these provide the phase and magnitude of the "in phase" and "quadrature" components of the high frequency data. These components are compared to determine the difference in phase and magnitude between 0H & 1H in all configurations, and between 1H & 2H in NTSC or 0H & 2H in PAL. The magnitude error signal can be doubled to facilitate inputs with low picture levels by setting the $FAIL2_1$ register bit HIGH. The doubled error signal is limited to ensure no overflow occurs.

Luma comb fail

The signals from the 3 low pass filters, 0HL, 1HL, and 2HL are subtracted from one another to produce an error signal proportional to the luma comb fail. The resulting signals (0HL - 1HL) and (1HL - 2HL) in NTSC and (0HL - 2HL) in PAL are rectified if negative. In cases where the luminance component is constant, the error will be zero. Where the luminance goes from black to white over 2 lines, the error signal will go to its maximum value.

The luma error signals can be doubled to facilitate inputs with low picture levels by setting the $FAIL2_0$ register bit HIGH. The resulting signal is clipped to ensure no overflow occurs.

XLUT

The comb fail signals control the adaption algorithm. Which of the fail signals is fed to the XLUT is determined by the KIS_{1-0} control signal, while the resolution of the error signals is selected by the XIP_{1-0} register bits as shown in Table 10.

Table 10. XIP error signals

XIP_{1-0}	Function
00	2 bits of phase error and 3 bits of chroma and luma magnitude error.
01	4 bits of chroma and luma magnitude error.
10	3 bits of phase error, 3 bits of chroma magnitude error and 2 bits of luma magnitude error
11	4 bits of phase error and chroma magnitude error

The selected comb fail signals are translated by the user-programmed configuration in the 256*5 XLUT into a mix signal (K) which is used to cross-fade between the weighted comb filter and the band split filters. The 0 to 31 mix signal is modified on the input to the cross-fade to produce a 0 to 32 control signal, as shown in Table 11.

Table 11. XLUT Output Function

XLUT OUTPUT	K
0	Special function (e.g. luma comb and HPF on chroma)
1	0 - 100% Bandsplit
2	2
3	3
:	:
16	16 - 50% Bandsplit, 50% Comb
:	:
29	29
30	30
31	32 - 100% Comb

Combed Luma
= Simple + (K * Combed High Freq Luma)

Combed Chroma
= Simple - (K * Combed High Freq Luma)

The special function assigned to K=0 is programmed into the XSF_{1-0} register bits, as shown in Table 12.

Table 12. XLUT special function definitions

XSF_{1-0}	XLUT special function selection	
	Y	C
00	comb	simple
01	simple	comb
10	flat with notch	simple
11	flat with notch	comb

The XLUT output, is fed through a bypassable low-pass filter KLPF to avoid switching between comb and simple decoders on a pixel by pixel basis. When the special function is selected (K=0) the input to the KLPF is held and the filter is automatically bypassed.

Digital Burst Locked Loop

The digital burst locked loop provides sine and cosine signals which are phase locked to the incoming burst signal. These sine and cosine signals are used to demodulate the chrominance data, producing the U and V color-difference signals. The U data are phase-referenced to sin(wt) and the V data to cos(wt). The demodulated signal is passed through a low pass filter to remove signals at twice the subcarrier frequency.

The magnitude of the U and V data within the demodulated burst signal provides the error signal which, after filtering, is used to adjust the frequency and/or phase of the subcarrier DDS. The output of the subcarrier DDS is translated into sine and cosine signals in ROM-based lookup tables.

The PALODD signal is low on lines without the 180 degree phase advance in the modulated V signal, termed NTSC lines, and high for lines with the 180 degree phase advance, termed PAL lines. This signal is used in the burst locked loop to advance the phase of the cosine table on PAL lines. PALODD is always low for NTSC.

Color kill counter

The demodulated U and V components are compared to a programmable burst level threshold. If both the U and V data fall below this threshold, a color kill flag is set high. The color kill counter is incremented once per line if the color kill flag is high. If the count reaches 127 within one field, the color kill circuit becomes active during the next field group. When this occurs, the input video will be passed unaltered on the luminance channel and the color difference signals will be set to chroma black.

The color kill signal remains active until a field with less than 127 lines without burst is encountered, at which time, during the next vertical blanking period, the decoder is reset.

Field flag, FLD

The FLD signal is the lsb of the field count FID_{2-0} and is LOW for fields where the first vertical sync occurs in the first half of the line and is HIGH for fields when it occurs in the second half of the line. This signal is synchronized with the frame and color frame flags in the FID generator.

Frame bit

- **NTSC**

  The middle bit (frame bit) of the field count is determined, by the phase of the subcarrier on a given pixel and on a given line. The signal used to determine this is NFDET (New Field DETect), and occurs when the line count is zero and the pixel count is one of four programmable pixel positions, zero, one, two, or three.

- **PAL**

  The frame bit in PAL is detected through the Bruch blanking sequence. The error signal control circuit generates a color kill flag whenever a line is detected without a burst. It is therefore possible to compare this signal with specific line idents to determine the field sequence in both PAL-I and PAL-M. A set of specific patterns determine the correct phase of FID_1; if any of these patterns is detected then FID_1 is forced to a known state and then flywheels until the next fixed pattern is detected.

Table 13. PAL-B,G,H,I Bruch Blanking Sequence

Internal line #	Burst present	Internal frame #	Internal field #
5	No	0 or 2	0 or 4
309	No	0 or 2	0 or 4
6	Yes	0 or 2	1 or 5
309	No	0 or 2	1 or 5
5	Yes	1 or 3	2 or 6
309	Yes	1 or 3	2 or 6
6	No	1 or 3	3 or 7
309	Yes	1 or 3	3 or 7

The frame bit is low for frames 0 and 2 and high for frames 1 and 3.

Table 14. PAL-M Bruch Blanking Sequence

Internal line #	Burst present	Internal frame #	Internal field #
7	No	0 or 2	0 or 4
258	Yes	0 or 2	0 or 4
7	No	0 or 2	1 or 5
259	No	0 or 2	1 or 5
7	Yes	1 or 3	2 or 6
258	No	1 or 3	2 or 6
7	Yes	1 or 3	3 or 7
259	Yes	1 or 3	3 or 7

The frame bit is low for frames 0 and 2 and high for frames 1 and 3.

PAL color frame bit

The PAL color frame bit is the msb of the field count, FID_2. In NTSC this is always low, as NTSC has only a 4 field sequence. For both PAL-I and PAL-M inputs, the PAL color frame bit is determined in the same way the frame bit is determined in NTSC, by using the phase of the subcarrier on a given pixel and on a given line.

Hue control

One of two programmable 16 bit system phase offsets can be added to the subcarrier oscillator between SAV and EAV. The selection is made by the BUFFER pin. This feature allows the user to change the picture hue on known frames without affecting the burst locked loop.

System monitoring of the burst loop error

The burst loop error signal is stored once per line in an 8 bit register that can be accessed over the microprocessor port. This allows the user to check for non-mathematical PAL inputs and to the change the decoder architecture from frame-based to line-based or simple decoder depending on this information.

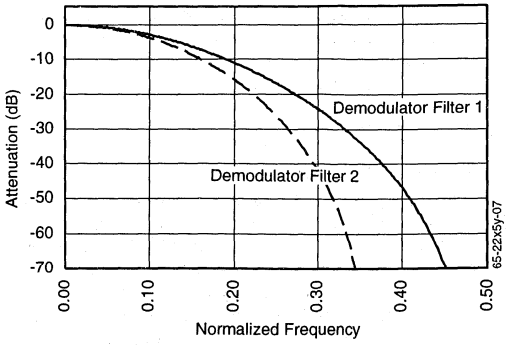


Figure 6. Gaussian Low Pass Filters

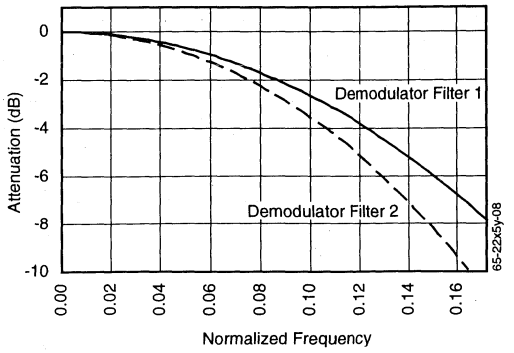


Figure 7. Gaussian LPF Passband Detail

Bypassing the chrominance demodulator

The demodulation of the chrominance signal needs to be bypassed when the decoder is processing C_BC_R component data or when a YC output is required. The bypass operation is controlled by the DMODBY register bit.

Demodulation low pass filter

There are two different demodulation low pass filters that can be selected under software. Gaussian filters are used as they have no negative coefficients and therefore have no undershoots or overshoots which could cause in-band ringing.

Bypassing the demodulation low pass filter

The demodulation low pass filter needs to be bypassed when processing C_BC_R component data or when a YC output is required. The C_BC_R data can also be passed through the Gaussian filter if the bandwidth needs to be reduced. The bypass operation is controlled by the GAUBY register bit.

Chrominance coring

Chrominance coring, when active, sets the lsbs of the chroma channel (below a programmable threshold) to zero.

$VMCR_5$ operation

When $VMCR_5$ is HIGH, the decoder will grab one line of video in LSTORE1. This effectively removes the comb filter from the decoding process, and the comb filter output is forced to simple mode.

Output Processor

Clamp and pedestal removal

A clamp pulse generated by the Burst Gate signal is used to grab a sample of the low-pass-filtered luma during the video back porch, providing the blanking level for the following video line. The blanking level is subtracted from the decoded luma. If the sign is negative, the result is assumed to be mixed sync and is passed through a delay and into the output matrix. If the sign is positive, the result is assumed to be pure luma (blanking to peak white) and is fed to the pedestal removal circuit. The 8 bit programmable pedestal is subtracted from the pure luma and the resulting luma is passed through a limiter to set any negative results to zero.

Adaptive Luma Notch Filter

The PAL line-locked comb decoder can never provide perfect subcarrier cancellation due to the 25Hz offset in the subcarrier frequency. This 25Hz offset causes residual and phase modified subcarrier to be left on the luminance signal which can produce a visible dot crawl on flat areas of color. However, for all comb filter structures, the quality of the comb depends on the quality of the sampling clock, as line to line clock jitter will also cause small phase changes between the inputs to the comb filter. It is therefore possible that NTSC comb decoders may also require some filtering of the luma output. To meet the wide range of sample frequencies that the decoder must deal with three separate adaptive luma notch filters are selectable.

The luma signal from the pedestal stripper is compared against the preceding pixel to detect the magnitude change between pixels. This magnitude difference will be almost zero for flat areas of picture, and large for high frequency changes in the picture. The magnitude difference is compared to one of four programmable thresholds. The programmable threshold is selected by the ANT_{1-0} register bits as shown in Table 15.

Table 15. Adaptive Notch Threshold Control

ANT_{1-0}	Magnitude difference
00	less than 32
01	less than 24
10	less than 16
11	less than 8

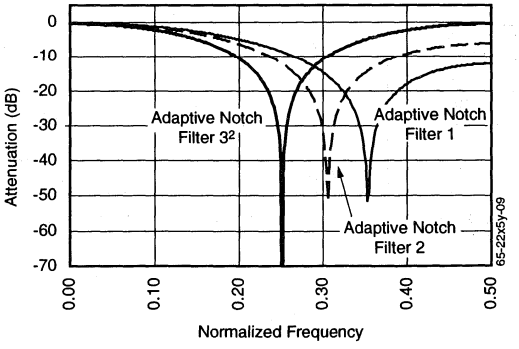


Figure 8. Adaptive Luma Notch Filters

If over a fixed number of pixels the error signal indicates that the magnitude difference is above the programmed threshold, or if ANEN is LOW, the adaptive notch filter is bypassed. However, if the error signal is below the programmed threshold the luma signal is passed through the adaptive notch filter. The output of the adaptive notch filter is

[2] Adaptive luma filter response in Figure 8 is the same as the non-adaptive filter response in Figure 9.

rounded to 8 or 10 bits, or the luma data that bypasses the coring filter is truncated to 8 or 10 bits depending upon the CORO register bit.

Non-adaptive luma notch filter

The simple luma notch filter is centered at 0.25 of normalized frequency, it therefore intended for use only in the subcarrier mode (4 * f_{SC}) and for limited use with 13.5MHz NTSC as the subcarrier sits at 0.265 of normalized frequency. The notch filter is enabled by setting the NOTCH register bit HIGH, and the ANEN register bit is LOW.

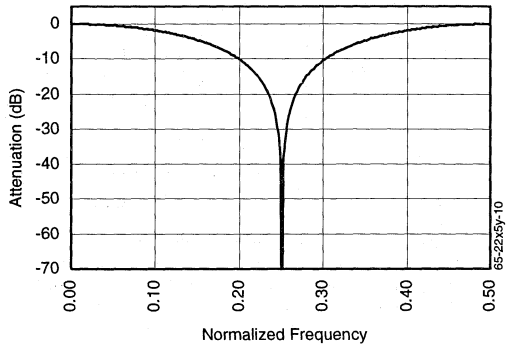


Figure 9. Non Adaptive Luminance Notch Filter

Matrix

The magnitude of the decoded luminance and color difference signals will vary, not only with the standard, but also with the input mode. For this reason the output matrix contains programmable multipliers, and not just fixed scaling factors. The following sub sections explain the different scalar in the output matrix. The gain term in the Y, mixed sync, U and V scalar is the same—only the weighting makes them different. The scalar are capable of independently providing 6dB of gain if required.

Programmable U Scalar

The U scalar (UGx) provides the weighting required to produce (B-Y) or C_B from the demodulated U signal.

hence

$$(B\text{-}Y) = UGx * U$$

where UGx = gain / 0.493, and

$$C_B = UGx * U$$

where UGx = (gain * 448) / Umax

UGx has a scaling range of 0 to (2047/256).

Programmable V Scalar

The V scalar (VGx) provides the weighting required to produce (R-Y) or C_R from the demodulated V signal.

hence

$$(R\text{-}Y) = VGx * V$$

where VGx = gain / 0.877, and

$$C_R = VGx * V$$

where VGx = (gain * 448)/Vmax

VGx has a scaling range of 0 to (1023/256).

Programmable Y Scalar

The Y scalar (YGx) provides the scaling for the luminance signal if the output is YC_BC_R, or controls the magnitude of the RGB output along with the U scalar and V scalar. It is not possible to control the magnitude of the RGB signals independently.

YGx has a scaling range of 0 to (1023/256).

Programmable MS Scalar

The sync scalar (SGx) provides the scaling for the sync signal if the output requires sync on Y or RGB. The programmed sync scaling factor is used during the horizontal and vertical burst blanking periods. During the active lines, the luma scaling factor is used to allow equal scaling of luma signals above and below the black level.

SGx has a scaling range of 0 to (1023/256).

Fixed (B-Y) and (R-Y) Scalars

These two scalars are zero when the output is YC_BC_R and provide the (B-Y) and (R-Y) weighting when the output is RGB. These are fixed scaling factors and are derived from the following equations.

$$(G\text{-}Y) = -[(0.299/0.587) * (R\text{-}Y)] - [(0.114/0.587) * (B\text{-}Y)]$$

or

$$(G\text{-}Y) = -[(1043/2048) * (R\text{-}Y)] - [(398/2048) * (B\text{-}Y)]$$

Y Offset

The 8 bit Y offset adds any offset required in the Y or RGB data outputs. For example 64 (16) for the 64 (16) to 940 (235) 10 bit (8 bit) "601" outputs. When the output is YC_BC_R this offset is applied to the luminance data only. The Y offset also provides the blanking level for RGB outputs with syncs.

Matrix Limiters

The different limiters are listed below, 10 bit data is assumed.

Table 16. Matrix Limiters

LMT_{1-0}	Comments
00	RGB output format, limited from 0 to 1023
01	YC_BC_R output format, Y limited from 0 to 1023 and C_BC_R limited to ±511.
10	RGB output format, limited from 64 to 940
11	YC_BC_R output format, Y limited from 64 to 940 and C_BC_R limited to ±448

Examples of output matrix operation
From the SMPTE-170M specification:

Color	Y	U	V
White	584	0	0
Yellow	523	-236	54
Cyan	423	79	-332
Green	361	-156	-278
Magenta	267	156	278
Red	205	-79	332
Blue	105	236	-54
Black	44	0	0

YC_BC_R data ranges are:

Y data range is 64 to 940 (876)
C_BC_R data ranges are 64 to 960 (+/- 448)

Matrix programming:

YGx = (876 / 540) = 1 + (159/256)
UGx = (448 / 236) = 1 + (230/256)
VGx = (448 / 332) = 1 + (89/256)
YOFF = 64
PED = 44

	Decoder Output			CCIR 601 Spec		
Color	Y	C_B	C_R	Y	C_B	C_R
White	939	0	0	940	0	0
Yellow	841	-448	73	840	-448	72
Cyan	678	150	-447	678	151	-448
Green	578	-296	-376	578	-296	-375
Magenta	426	296	376	426	296	375
Red	325	-150	447	326	-151	448
Blue	163	448	-73	164	448	-72
Black	64	0	0	64	0	0

PAL digital composite input and RGB (0-1023) outputs:

Color	Y	U	V
White	572	0	0
Yellow	507	-250	57
Cyan	401	84	-352
Green	336	-165	-295
Magenta	236	165	295
Red	171	-84	352
Blue	65	250	-57
Black	0	0	0

The nominal scaling factors are simply:

YGx = 1023/572 = 1 + (202/256)
UGx = (1023/572)*(1/0.492) = 3 + (163/256)
VGx = (1023/572)*(1/0.877) = 2 + (10/256)
YOFF= 0
PED = 0

Color	G	R	B
White	1023	1023	1023
Yellow	1023	1023	0
Cyan	1023	0	1023
Green	1023	0	1
Magenta	0	1023	1022
Red	0	1023	1
Blue	0	0	1023
Black	0	0	0

It is also possible with the architecture supplied to use the limiters on the output of the matrix to clip the output video deliberately by using a slightly larger gain than is required. The Y_Offset can achieve the same by setting its value to be one lsb less than the minimum clip level.

Buffer Registers

The BUFFER pin allows the user to externally switch between two sets of internal registers that have the same function. This register buffering allows the matrix gain, picture hue, and luma offset to be changed at a known time relative to the input data.

Registers 17 to 1D are selected when the BUFFER pin is LOW and registers 27 to 2D are selected when the BUFFER pin is HIGH. If the msb of the decoder product code DPC_2 is LOW, an 8 bit decoder has been selected and the bottom 2 bits of registers 17 to 1A and 27 to 2A are forced to zero.

Simple luma color correction
If the YBAL register bit is set HIGH, and the luma data reaches or exceeds the luma limits, there should be no C_BC_R or UV data at that time; therefore the color data are set to ZERO. If YBAL is set LOW then the C_BC_R/UV data are unaffected by the luma data.

C_BC_R msb inversion
The msb of the C_BC_R data can be inverted by setting the MSBO register bit HIGH. As this would affect the chroma blanking level, this circuit appears at the output of the MATRIX circuit.

Output rounding
For compatibility with 8 bit systems, the output of the matrix can be rounded to 8 bits by setting the RND8 register bit HIGH.

Output Formats

RGB outputs

The RGB data are simply passed through to the decoder output. When the DRSEN register bit is HIGH the DRS data are inserted into the green data path only.

YUV outputs

The YUV data are simply passed through to the decoder output. When the DRSEN register bit is HIGH the DRS data are inserted into the luminance data path only.

YC_BC_R outputs

The YC_BC_R data can be output in 3 ways, depending upon the CDEC, F422, and YUVT register bits. These output modes are summarized in *Table 19*.

When CDEC is HIGH and F422 is HIGH, the G/Y output is set to 64 and the B/U output is set to 512 between the EAV TRS data word and the first preamble word of the SAV TRS, i.e. during the digital horizontal blanking period. When YUVT is HIGH, R/V is set to 512, 64, 512, 64, etc., starting after the EAV TRS data word and finishing before the SAV preamble.

Table 17. Output Format

CDEC	YUVT	F422	G/Y	B/U	R/V	Comments
0	x	x	G or Y	B or C_B	R or C_R	[4:4:4] data
1	0	0	Y	C_B	C_R	[4:2:2] data
1	0	1	Y	C_BC_R	0	[4:2:2] data
1	1	x	Y	C_BC_R	D1 data	[4:2:2] data & D1 output

Decimating C_BC_R data

Whenever the CDEC register bit is set HIGH the B/U and R/V data are simply sample dropped, with respect to CBSEL, to produce the multiplexed C_BC_R data stream at the PCK clock rate. If the input was initially D1 then the dropped samples will be the interpolated samples produced by the chroma interpolation filter. If however the C_BC_R data are simply weighted UV data then the sample dropped demodulated color difference signals (UV) will alias around 0.25 of the normalized sample frequency.

Multiplexed YC_BC_R output (TRS words inserted)

When both the CDEC and YUVT register bits are HIGH the Y, C_B, and C_R component data are multiplexed into a single 27MHz (PXCK) data stream with embedded TRS words. The TRS words are generated based on the $\overline{\text{HSYNC}}$ or $\overline{\text{VSYNC}}$ pulses provided to the decoder, and the internally derived horizontal blanking ($\overline{\text{HBLK}}$), vertical blanking ($\overline{\text{VBLK}}$), and the field flag (FLD). This mode of operation is only available if a line locked PXCK clock, at 27MHz, is provided. The TRS words will be generated with respect to the $\overline{\text{HSYNC}}$ signal as per the ANSI/SMPTE 125M-1992 and CCIR656 specifications.

YC outputs

The YC data are passed through to the decoder output. When the DRSEN register bit is HIGH the DRS data are inserted into the luminance data path only. The luminance appears on G/Y, chrominance is on B/U and the R/V output is set to zero, by setting the V_scalar to zero.

The LDV clock

The decoder can accept clocks at either the pixel clock rate (PCK) or at twice the pixel clock rate (PXCK). In the cases where the clock provided is PXCK, for example the genlock mode, the output data still needs to be at the PCK clock rate. To aid in the design of external circuitry a LDV clock is provided if the LDVIO register bit is LOW, if LDVIO is HIGH then the LDV pin becomes an input for an external clock.

If an external LDV clock is employed the user must ensure that the rising edge of the external LDV meets the specified setup and hold times relative to the input CLOCK pin. The selection of which clock to use on the decoder output is set by the OPSEL register bit. When OPSEL is set LOW the output is clocked at the same rate as the clock on the CLOCK pin, and when OPSEL is set HIGH the output is clocked by the internal or external clock on the LDV pin.

Timing Parameters

Subcarrier Programming

The color subcarrier is produced by an internal 28 bit Direct Digital Synthesizer (DDS) which is phase locked to the burst signal of the digitized video input. The nominal frequency is programmed into the DDS as follows:

FREQ = (number of subcarrier cycles per line / number of pixels per line) * 2^28

An example would be NTSC subcarrier mode

FREQ = (227.5 / 910) * 2^28 = 4000000 hex

Horizontal Timing

The horizontal video line is broken down into four horizontal timing parameters.

STS: The number of pixels between sync pulses

STB: The number of pixels between the nominal mid point of sync and the start of the 16 pixel burst gate. This value is modified depending upon the mode of operation.

Standard	Mode	Offset required
x	Genlock	-8
x	Line locked	-8
x	Subcarrier	-22
PAL	D2 mode	-12
NTSC	D2 mode	-8
x	D1 mode	+12

BTV: The number of pixels between the start of the 16 pixel burst gate and the nominal start of active video.

AV: The number of active pixels in the active video line.

The difference between the sum of STB+BTV+AV subtracted from STS provides the nominal front porch.

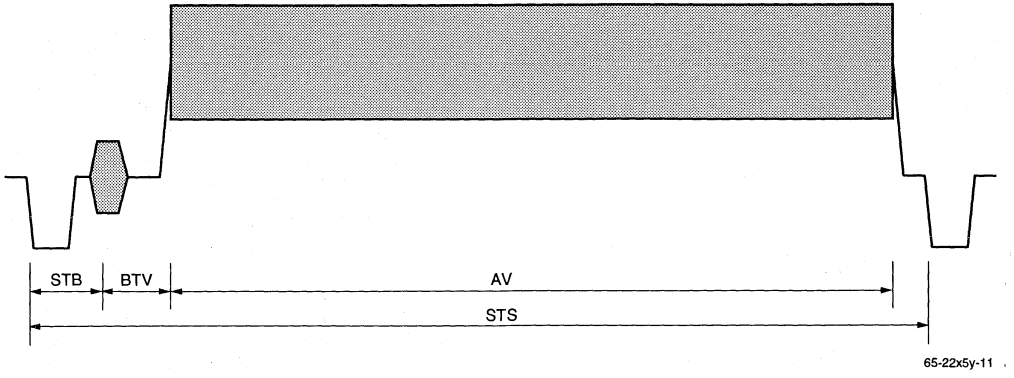


Figure 10. Horizontal Timing

Horizontal and Vertical Timing Parameters

When external horizontal and vertical syncs are provided the timing shown in Figure 11 is required to synchronize the internal state machines to beginning of a field 1 (3, 5, or 7).

For field 2 (4, 6, or 8) the falling edge of $\overline{\text{VSYNC}}$ must occur at least 2 clock periods but not more than (H–2) clock periods after the falling edge of $\overline{\text{HSYNC}}$, where H is the total number of pixels in an active video line.

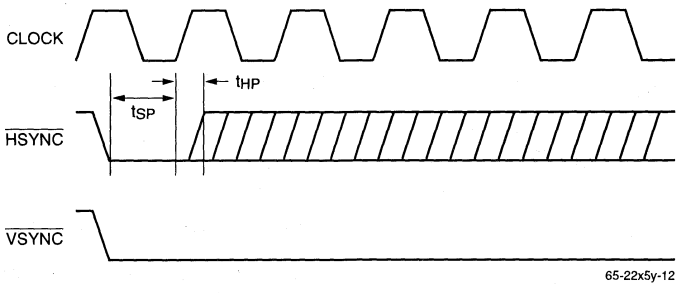


Figure 11. External HSYNC and VSYNC TIming for Field 1 (3, 5, or 7)

Preliminary Information

Vertical Blanking

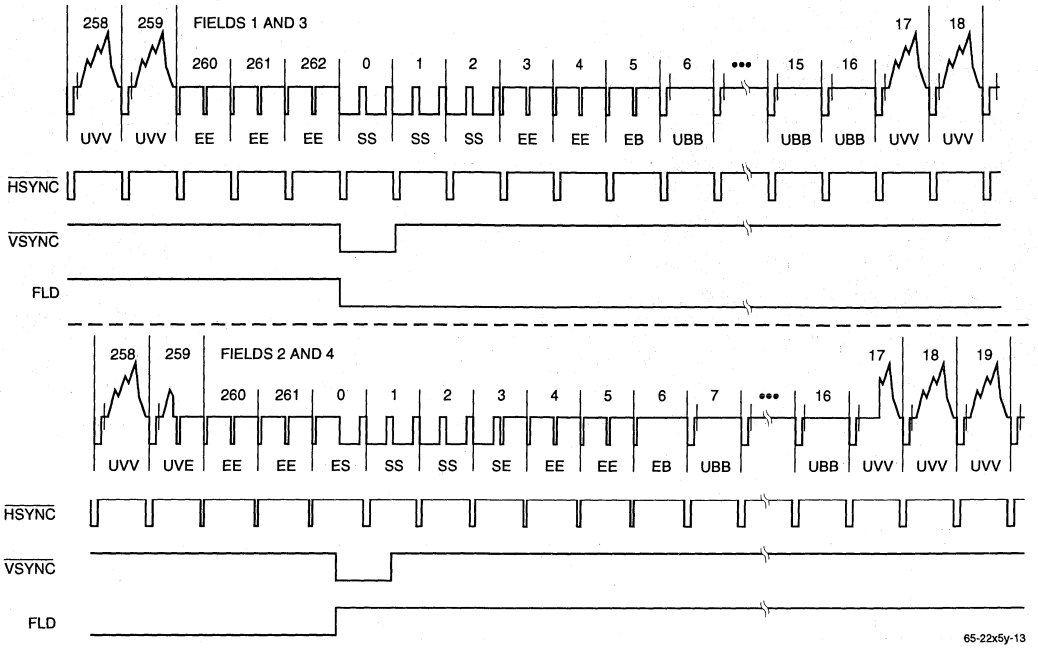


Figure 12. NTSC Vertical Interval

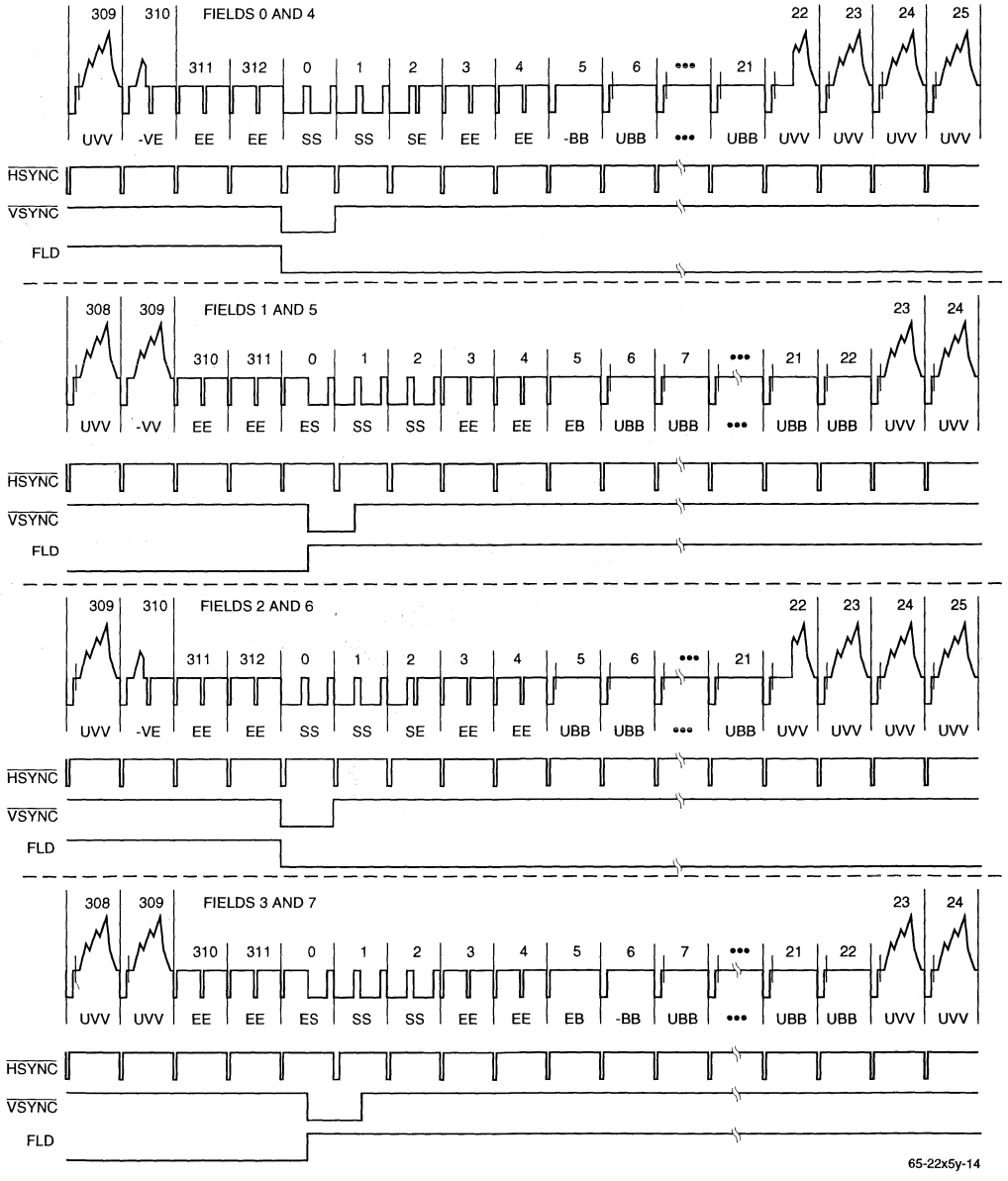


Figure 13. PAL-B, G, H, I, N Vertical Interval

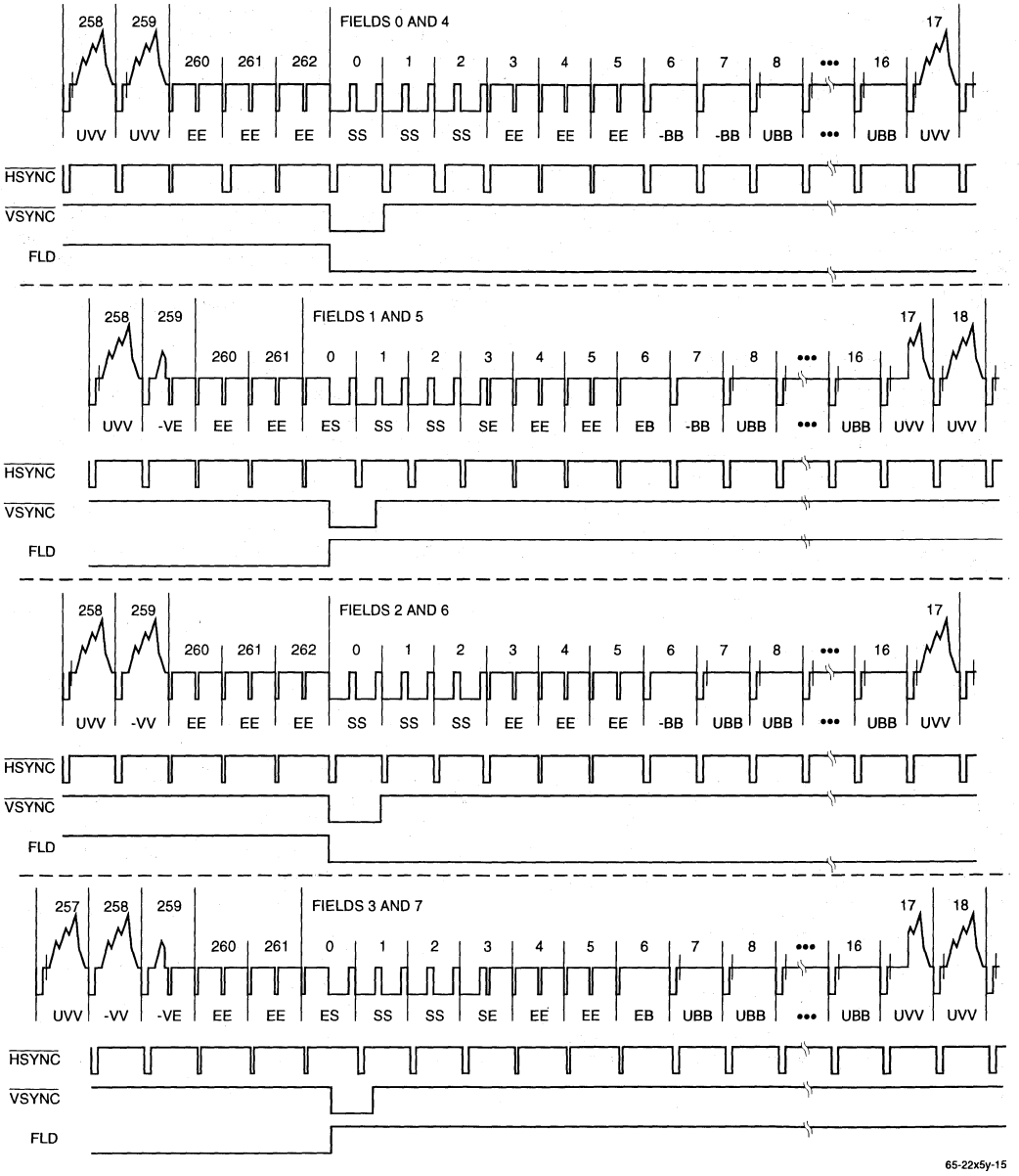


Figure 14. PAL-M Vertical Interval

VINDO Operation

The VINDO circuit uses the line idents on LID_{4-0}, and the blanking signals to control the comb filter output and the blanking of the YUV data in the output matrix during the vertical blanking period.

The vertical window VINDO starts on the first line after the last equalizing pulse, at $LID_{4-0} = 02$. The VINDO stays HIGH from this line until the VINDO count = $VINDO_{4-0}$, or the $\overline{VBLK}$ signal goes HIGH, at which time the VINDO goes LOW. While the VINDO is HIGH the decoder operation is controlled by VDIV, and during the time the VINDO and $\overline{VBLK}$ are LOW the decoder operation is controlled by VDOV.

Table 18. PAL VINDO operation

LID_{4-0}	VINDO	VDIV	VDOV	Y	C
00–01	x	x	x	normal	normal
02–0A	1	0	x	simple	simple
02–0A	1	1	x	flat	black
02–0A	0	x	0	black	black
02–0A	0	x	1	simple	simple
0B–17	x	x	x	normal	normal

NTSC VINDO operation

LID_{4-0}	VINDO	VDIV	VDOV	Y	C
00–02	x	x	x	normal	normal
03–06	1	0	x	simple	simple
03–06	1	1	x	flat	black
03–06	0	x	0	black	black
03–06	0	x	1	simple	simple
07–17	x	x	x	normal	normal

Parallel Microprocessor Interface

The parallel microprocessor interface, active when $\overline{SER}$ is HIGH, employs a 12-line interface, with an 8-bit data bus and one address bit: two addresses are required for device programming and pointer-register management. Address bit 0 selects between reading/writing the register addresses and reading/writing register data. When writing, the address is presented along with a LOW on the $\overline{R/W}$ pin during the falling edge of $\overline{CS}$ Eight bits of data are presented on D_{7-0} during the subsequent rising edge of $\overline{CS}$. One additional falling edge of $\overline{CS}$ is needed to move input data to its assigned working registers.

In read mode, the address is accompanied by a HIGH on the $\overline{R/W}$ pin during a falling edge of $\overline{CS}$. The data output pins go to a low-impedance state t_{DOZ} after $\overline{CS}$ falls. Valid data are present on D_{7-0} t_{DOM} after the falling edge of $\overline{CS}$. Because this port operates asynchronously with the pixel timing, there is an uncertainty in this data valid output delay of one PXCK period. This uncertainty does not apply to t_{DOZ}.

Writing data to specific control registers of the TMC22x5y requires that the 8-bit address of the control register of interest be written. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 3Fh.

Table 19. Parallel Port Control

A_{1-0}	$\overline{R/W}$	Action
00	0	Load D_{7-0} into Control Register pointer (block 00)
00	1	Read Control Register pointer on D_{7-0}
01	0	Load D_{7-0} into addressed XLUT Location pointer (block 01)
01	1	Read addressed XLUT Location pointer on D_{7-0}.
10	0	Write D_{7-0} to addressed Control Register
10	1	Read addressed Control Register on D_{7-0}
11	0	Write D_{7-0} to addressed XLUT Location
11	1	Read addressed XLUT Location on D_{7-0}

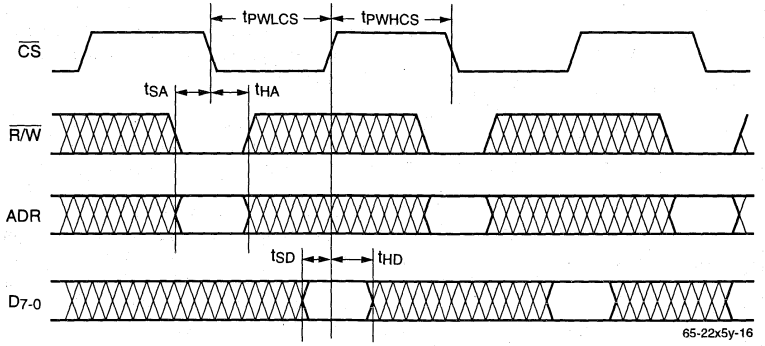


Figure 15. Microprocessor Parallel Port – Write Timing

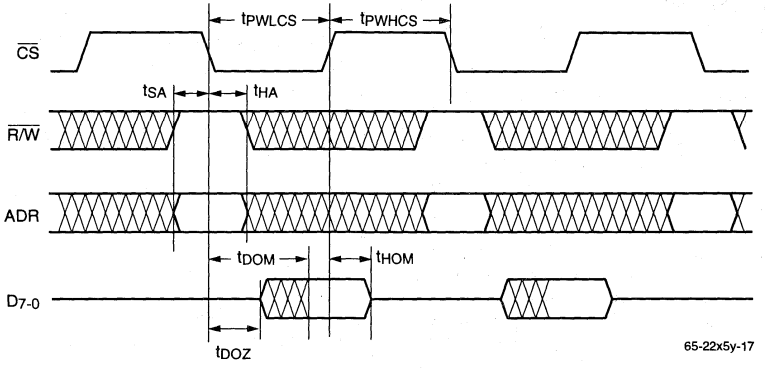


Figure 16. Microprocessor Parallel Port – Read Timing

Serial Control Port (R-Bus)

In addition to the 12-wire parallel port, a 2-wire serial control interface is provided, and active when $\overline{SER}$ is LOW. Either port alone can control the entire chip. Up to eight TMC22x5y devices may be connected to the 2-wire serial interface with each device having a unique address.

The 2-wire interface comprises a clock (SCL) and a bi-directional data (SDA) pin. The Decoder acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is LOW. If SDA changes state while SCL is HIGH, the serial interface interprets that action as a start or stop sequence.

There are six components to serial bus operation:

- Start signal
- Slave address byte
- Block Pointer
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are HIGH) communications are initiated by sending a start signal. The start signal is a HIGH-to-LOW transition on SDA while SCL is HIGH. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a seven bit slave address (the first seven bits) and a single $\overline{R/W}$ bit (the eighth bit). The $\overline{R/W}$ bit indicates the direction of data transfer, read from or write to the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA_{2-0} input pins in Table 20), the TMC22x5y acknowledges by bringing SDA LOW on the 9th SCL pulse. If the addresses do not match, the TMC22x5y does not acknowledge.

Table 20. Serial Port Addresses

bit 7 A_6 (MSB)	bit 6 A_5	bit 5 A_4	bit 4 A_3	bit 3 A_2 (SA_2)	bit 2 A_1 (SA_1)	bit 1 A_0 (SA_0)
1	0	1	1	0	0	0
1	0	1	1	0	0	1
1	0	1	1	0	1	0
1	0	1	1	0	1	1
1	0	1	1	1	0	0
1	0	1	1	1	0	1
1	0	1	1	1	1	0
1	0	1	1	1	1	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the TMC22x5y does not acknowledge the master device during a write sequence, the SDA remains HIGH so the master can generate a stop signal. If the master device does not acknowledge the TMC22x5y during a read sequence, the Decoder interprets this as "end of data." The SDA remains HIGH so the master can generate a stop signal.

Writing data to specific control registers of the TMC22x5y requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 3Fh. Any base address higher than 3Fh will not produce an ACKnowledge signal.

Data are read from the control registers of the TMC22x5y in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W\ bit of the slave address byte LOW to set up a sequential read operation.

Reading (the $\overline{R/W}$ bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the TMC22x5y, a stop signal must be sent. A stop signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to one control register

- Start signal
- Slave Address byte ($\overline{R/W}$ bit = LOW)
- Block Pointer (00)
- Base Address byte
- Data byte to base address
- Stop signal

Write to four consecutive XLUT locations

- Start signal
- Slave Address byte ($\overline{R/W}$ bit = LOW)
- Block Pointer (01)
- Base Address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Read from one XLUT location

- Start signal
- Slave Address byte ($\overline{R/W}$ bit = LOW)
- Block Pointer (01)
- Base Address byte
- Stop signal

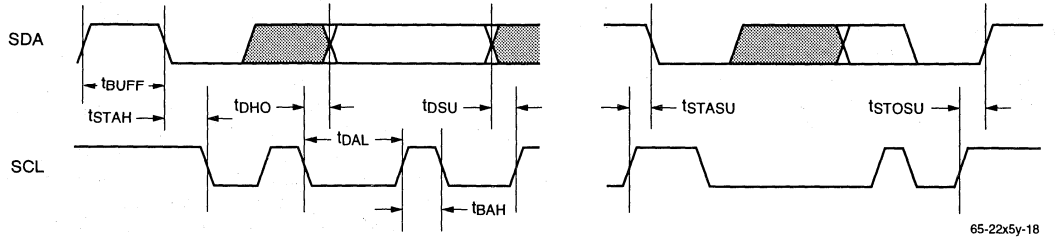


Figure 17. Serial Port Read/Write Timing

- Start signal
- Slave Address byte ($\overline{R/W}$ bit = HIGH)
- Data byte from base address
- Stop signal

Read from four consecutive control registers

- Start signal
- Slave Address byte ($\overline{R/W}$ bit = LOW)
- Block Pointer (00)
- Base Address byte
- Stop signal
- Start signal
- Slave Address byte ($\overline{R/W}$ bit = HIGH)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

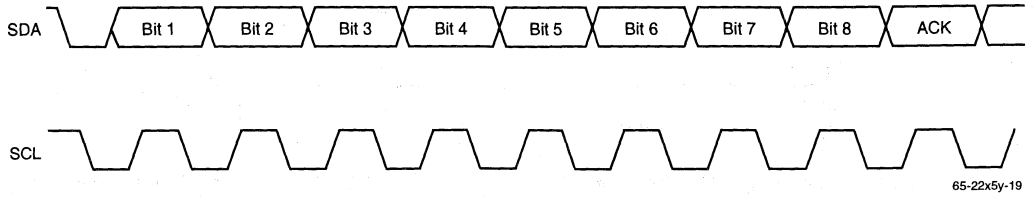


Figure 18. Serial Interface – Typical Byte Transfer

Video Measurement

The TMC22x5y supports a comprehensive set of video measurement techniques to aid the user in setting up the gain, phase, etc. of the decoder and in tracking down system errors.

Pixel Grab

The pixel grab allows the user to grab one pixel every line, or one pixel out of the four field sequence in NTSC or the 8 field sequence in PAL, under software control. The SET pin can also be used to produce the pixel grab pulse if $SET_{2\text{-}0}$ = 110 and PGEXT is set HIGH.

The 10 bit G/Y, B/U, R/V outputs are stored in one set of four 8 bit registers while the 10 bit luma and mixed sync data and the 10 bit demodulated U and V color difference signals are stored in a set of five 8 bit registers. The pixel grab signal, whether internally or externally generated, is internally delayed to ensure that the all the grabbed data are from the same pixel relative to the line sync pulse. The GRABS signal is PGRAB or the logical AND of PGRAB with FGRAB and LGRAB, and is controlled by the LPGEN, PGEN, and PGEXT register bits.

Table 21. Pixel grab control

LGEXT	PGEN	PGEXT	LGEN	GRABS signal
0	0	x	x	GRABS = 0
0	1	0	0	GRABS = PGRAB
0	1	0	1	GRABS = FGRAB & LGRAB & PGRAB
0	1	1	x	GRABS = NOT (SET pin)
1	x	0	x	GRABS = PGRAB
1	x	1	x	GRABS = NOT (SET pin)

An example of the pixel grab feature is grabbing a pixel in the center of the burst period, allowing the user to check the burst height by reading the magnitude of the demodulated U and V components. This allows the user to compensate for any chrominance gain errors in the output matrix.

Composite Line Grab

The composite line grab is only available in the 3 line comb based decoders (TMC22053 and TMC22153), and allows the user to grab any line from the 4 field sequence in NTSC or 8 field sequence in PAL when LGEN is set HIGH. When the LGEN register bit is set HIGH the decoder automatically switches to operate as a "simple" bandsplit decoder. The SET pin can also be used to produce the line grab pulse if $SET_{2\text{-}0}$ = 110 and LGEXT is set HIGH.

Once the line grab has been activated the subcarrier oscillator is frozen with the SEED and phase from the beginning of the line, and the composite video in the 1H line store is frozen by disabling the write signals in LSTORE1. The read cycle for the frozen line store is still clocked by PCK. The subcarrier DDS and the internal read only registers will be updated once per clock period as normal, but will reload the DRS SEED and PHASE values at the beginning of each line. The G/Y, B/U, and R/V outputs will remain active, and the $\overline{DHSYNC}$ and $\overline{DVSYNC}$ signals will remained locked to the input or flywheel if the input has been removed.

The pixel grab function can be used in conjunction with the frozen line to examine individual pixels inside the decoder.

Equivalent Circuits and Threshold Levels

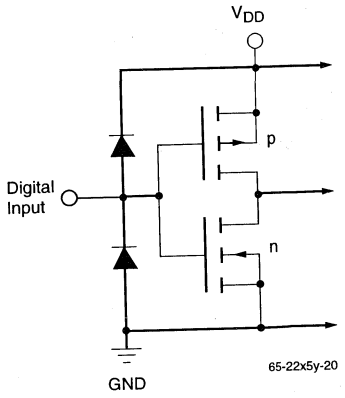


Figure 19. Equivalent Digital Input Circuit

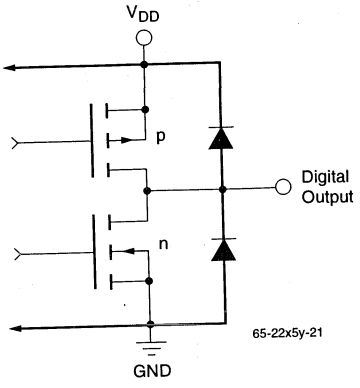


Figure 20. Equivalent Digital Output Circuit

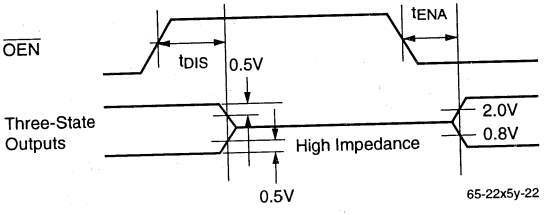


Figure 21. Threshold Levels for Three-State Measurement

Preliminary Information

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Max	Unit
Power Supply Voltage	-0.5	+7.0	V
Digital Inputs			
Applied Voltage	-0.5	V_{DD}+0.5	V
Forced current [3, 4]	-20.0	+20.0	mA
Output			
Applied voltage [2]	-0.5	(V_{DD}+ 0.5)	V
Forced current [3, 4]	-3.0	+6.0	mA
Short circuit duration (single output in HIGH state to ground)		1 second	
Analog Output Short circuit duration (all outputs to ground)		infinite	
Temperature			
Operating, ambient	-20	110	°C
junction		+140	°C
Lead, soldering (10 seconds)		+300	°C
Vapor Phase soldering (1 minute)		+220	°C
Storage	-65	+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Conditions	Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH	TTL Compatible Inputs	2.0		V_{DD}	V
		CLK Input	2.4		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW		GND		0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C
Pixel Interface						
f_{CLK}	Pixel Rate	(CKSEL=0)	10		18	MHz
	Master Clock Rate, = 2X pixel rate	(CKSEL=1)	20		36	MHz
t_{PWHCK}	CLOCK pulse width, HIGH		10			ns
t_{PWLCK}	CLOCK pulse width, LOW		10			ns
t_{SP}	Input data setup time				12	ns
t_{HP}	Input data hold time		0			ns
t_{POD}	Clock to output data, propagation delay				25	ns
t_{HOD}	Output data hold time		3			ns
t_{ENA}	Enable to Low Z on output data		8		23	ns
t_{DIS}	Disable to High Z on output data		10		20	ns

Operating Conditions (continued)

Parameter		Conditions	Min	Nom	Max	Units
Parallel Microprocessor Interface						
t_{PWLCS}	$\overline{CS}$ Pulse Width, LOW		3			CLOCK
t_{PWHCS}	$\overline{CS}$ Pulse Width, HIGH		2			CLOCK
t_{SA}	Address Setup Time		10			ns
t_{HA}	Address Hold Time		0			ns
t_{SD}	Data Setup Time (write)		15			ns
t_{HD}	Data Hold Time (write)		0			ns
Serial Microprocessor Interface						
t_{DAL}	SCL Pulse Width, LOW		1.0			µs
t_{DAH}	SCL Pulse Width, HIGH		0.48			µs
t_{STAH}	Hold Time for START or Repeated START		0.48			µs
t_{STASU}	Setup Time for START or Repeated START		0.48			µs
t_{STOSU}	Setup Time for STOP		0.48			µs
t_{BUFF}	Bus Free Time Between a STOP and a START Condition		1.0			µs
t_{DSU}	Data Setup Time		80			ns

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Current[1]	V_{DD} = Max, f_{PXCK} = 27MHz			150	mA
I_{DDQ}	Power Supply Current, Disabled	V_{DD} = Max, f_{PXCK} = 27MHz			45	mA
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	S_{15-0}, I_{OH} = MAX	2.4			V
V_{OL}	Output Voltage, LOW	S_{15-0}, I_{OL} = MAX			0.4	V
C_I	Digital Input Capacitance			4	10	pF
C_I	Digital Output Capacitance			10		pF

Notes:

1. Typical I_{DD} with V_{DD} = NOM and T_A = NOM, Maximum I_{DD} with V_{DD} = MAX and T_A = MIN.

Preliminary Information

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DOZ}	Output Delay, $\overline{CS}$ to low-Z		10			ns
t_{HOM}	Output Hold Time, $\overline{CS}$ to high-Z		10			ns
t_{DOM}	Output Delay, $\overline{CS}$ to Data Valid			30		ns
t_{DOTP}	Output Delay, TCK to TDO Valid			10		ns
t_{HOTP}	Output Hold Time, TCK to TDO Valid			5		ns

Note:

1. Timing reference points are at the 50% level, digital output load <40pF.

System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Units
RES	Video Processing Resolution	TMC2205y		8		bits
		TMC2215y		10		bits

Applications Information

Line-based Comb Decoders

The principle of line based comb filters exploits the fact that the chrominance vectors rotate by 180 degrees every line in NTSC and every two lines in PAL, while the luminance component does not.

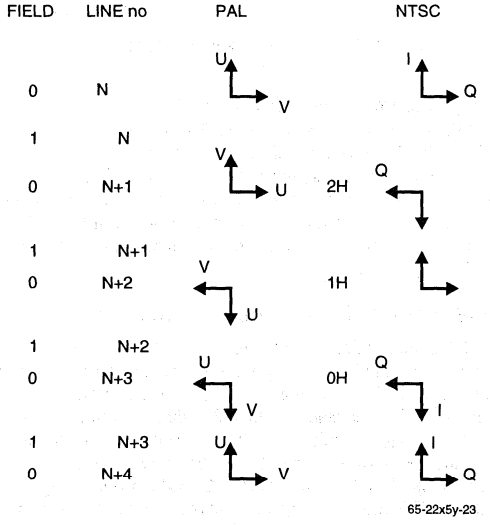


Figure 22. Chrominance vector rotation in PAL and NTSC

The three line comb based decoder is clearly biased towards `1H' which illustrates the inherent one line delay through a 3 line comb, while a two line comb based decoder is biased towards `0H'. In the following discussions a flat color represents video of constant luma and chroma magnitude and phase.

Composite Line-based comb decoders

In NTSC adding two adjacent lines of flat color will cancel the chroma and leave the luma while subtracting two lines of flat color will cancel the luma and leave the chroma. In 3 line comb filters the flat color on 0H and 2H is added to provide the flat color average before adding or subtracting from 1H.

In PAL, adding the flat color from 0H & 2H will cancel the chroma and leave the luma while subtracting the flat color from 0H & 2H will cancel the luma and leave the chroma.

YC Line-based comb filters

The luminance and chrominance are already separated for YC inputs. However, if the original source was composite, there is a distinct possibility that there is some residual luminance (cross color) in the chrominance signal and some residual chrominance (cross luma) in the luminance signal. It is therefore legitimate to treat these signals as if they were simply the output of our internal bandsplit filters and comb the luma and chroma signals accordingly.

If desired the decoder can be programmed to pass the YC data unprocessed through the comb filter and feed the YC data directly to the demodulator and output processor. For 3-line Y/C comb filters, an external 1H delay is required for the uncombed channel to compensate for the comb filter delay.

D1 Line-based comb filters

The D1 data are already in the YC_BC_R component format but if the original source was composite there is a distinct possibility that there is luminance (cross color) in C_BC_R and chrominance (cross luma) in Y. In the first case any luminance that was passed through a demodulator along with the chroma to produce the baseband C_BC_R color difference

signals would have the same characteristics as chroma. That is to say, the cross color would advance by 180° every line in NTSC and every 2 lines in PAL. It is therefore possible to remove this cross color in a comb filter. In the latter case any chrominance that is still in the Y data can obviously be removed in a comb filter as well.

The original source for the D1 signal could also have been computer graphics. In this case, the comb filter can be used to remove the picture flicker and convert the output to RGB.

NTSC Frame- and Field-based Decoders

Composite frame-based comb filters

In NTSC the chrominance vectors advance by 180 degrees every line, therefore after 525 lines the 2 adjacent frame lines 0H and FR0H and the two consecutive field lines FR0H and FR1H are 180 degrees apart. The flat color on FR0H and FR1H can be added or subtracted to provide the luminance or chrominance to subtract from 0H.

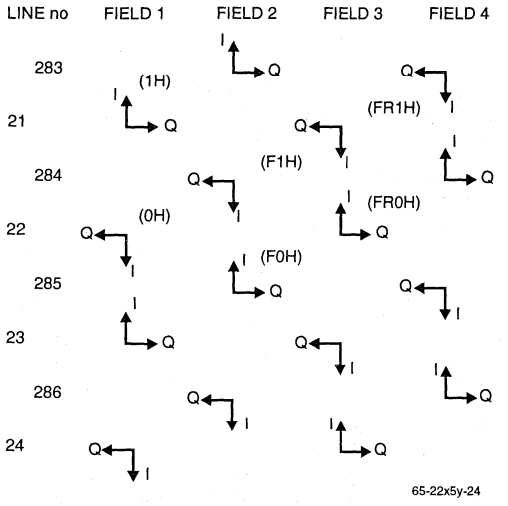


Figure 23. Chrominance vector rotation over 4 fields in NTSC

Composite field-based comb filters

In NTSC field based comb decoders, VIDEOA is externally delayed by 263 lines, therefore the 2 adjacent picture lines 0H and F0H and the two consecutive field lines F0H and F1H are 180 degrees apart. The flat color on F0H and F1H can be added or subtracted to provide the luminance or chrominance to subtract from 0H.

PAL Frame- and Field-based Decoders

Composite PAL frame-based comb filters

In PAL the chrominance vectors advance by 270 degrees every line. After 625 lines the two adjacent frame lines 0H and FR0h are 90 degrees apart. It is therefore necessary to delay the FR0H data internally by 1H so that 0H and FR0H are 180 degrees apart. The flat color on 0H and FR0H can now be added to provide the luminance or subtracted to produce chrominance. Due to the 270 degree advance, it is not possible to use information from consecutive field lines without adding a PAL modifier. In fields 5, 6, 7, and 8 the U and V vectors are 180 degrees advanced from fields 1, 2, 3, and 4.

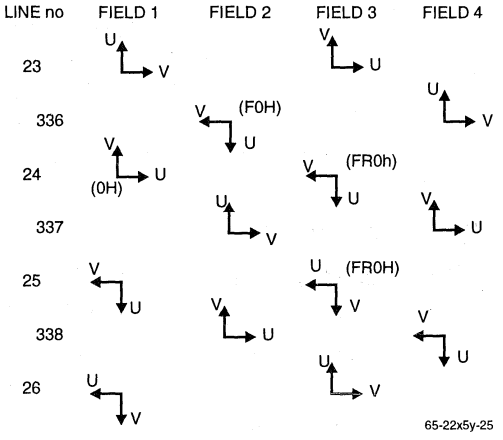


Figure 24. Chrominance vector rotation over 4 fields in PAL

Composite, PAL field-based comb filters

In PAL field based comb decoders, VIDEOA is externally delayed by 312 lines, therefore the 2 adjacent picture lines 0H and F0H are 180 degrees apart. Due to the 270 degree advance, it is not possible to use information from consecutive field lines without adding a PAL modifier. In fields 5, 6, 7, and 8 the U and V vectors are 180 degrees advanced from fields 1, 2, 3, and 4.

YC Frame- or Field-based Comb Filters

For YC frame or field based comb filters it is only possible to comb the Y and C signals separately. It is therefore necessary to either pass the uncombed signal through a frame or field store + t_P to compensate for the delay through the decoder or comb both signals independently. The time t_P is defined as the time taken for data at INPUT A/B to be processed through the decoder and appear at the G/Y, B/U, and R/V outputs. This time t_P is fixed across the product line and is independent of the internal architecture.

Programming Examples

Standard: NTSC-M

Mode: Line-Locked

Input Format: 13.5 MHz Composite Video

Output Format: RGB (0-1023)

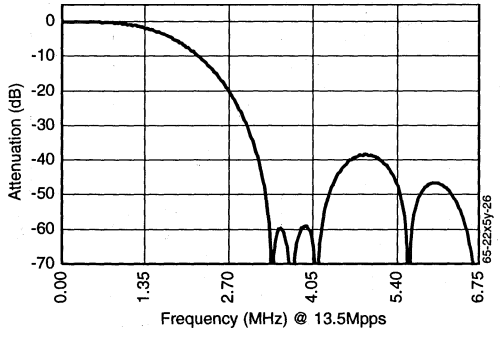
Decoder: Adaptive 3-Line Chroma Comb Filter

Register Map:

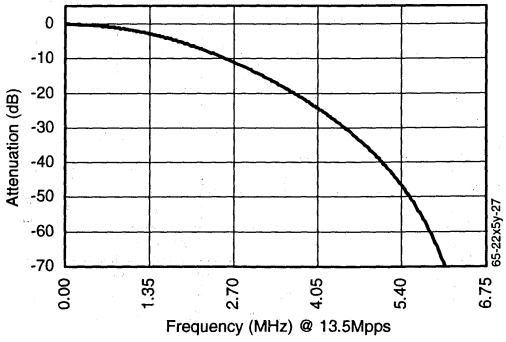
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C0	01	00	A1	20	2C	00	00	40	00	00	03	00	04	24	09
1	5A	50	2E	C8	23	00	01	00	E5	DD	2B	5A	00	00	00	00
2	40	F8	E0	43	00	00	00	xx	xx	xx	xx	xx	xx	xx	xx	xx

The DRS appears on the G/Y output at the PXCK rate.

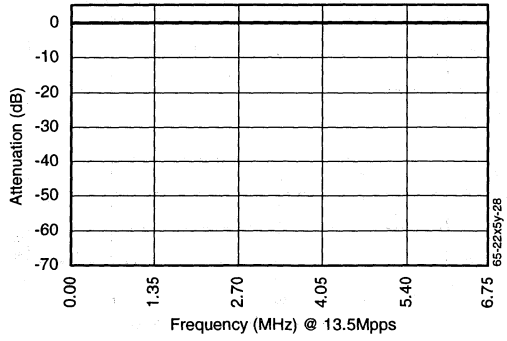
Bandsplit Filter (BSF 1)



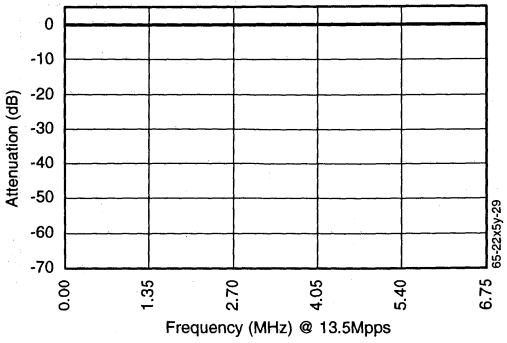
Demodulator Filter (LPF 1)



Adaptive Notch Filter (bypassed)



Notch Filter (bypassed)



Programming Examples (continued)

Standard: PAL-I

Mode: Line-Locked

Input Format: 13.5 MHz Composite Video

Output Format: RGB (0-1023)

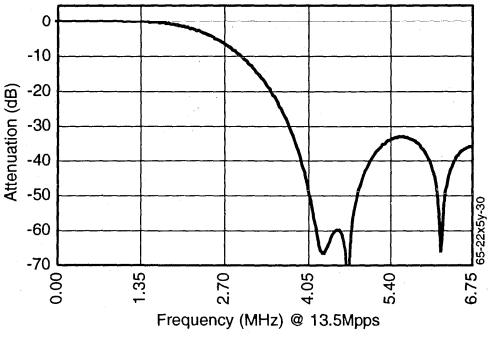
Decoder: Adaptive 3-Line Chroma Comb Filter

Register Map:

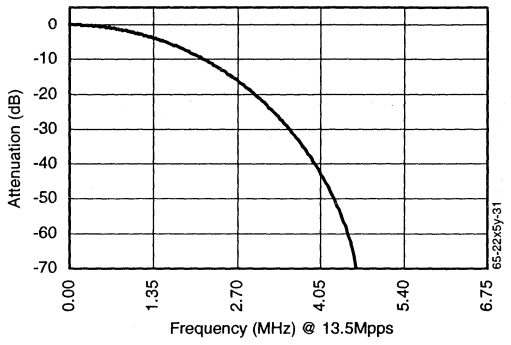
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C3	01	00	20	20	00	00	04	40	08	00	03	80	C4	24	09
1	60	53	32	BE	23	00	01	00	CA	A6	0C	5A	00	00	00	00
2	90	15	13	54	00	00	00	xx	xx	xx	xx	xx	xx	xx	xx	xx

The DRS appears on the G/Y output at the PXCK rate, luma and chroma adaptive notch disabled.

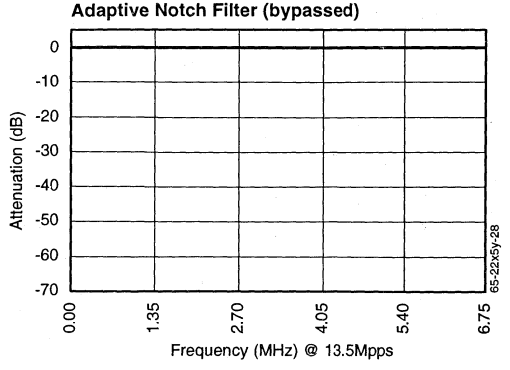
Bandsplit Filter (BSF 2)



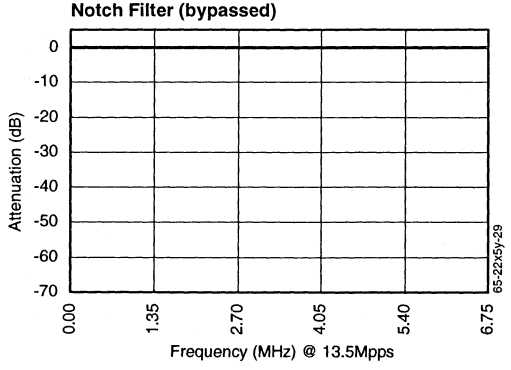
Demodulation Filter (LPF 2)



Adaptive Notch Filter (bypassed)



Notch Filter (bypassed)



Programming Examples (continued)

Standard: PAL-I

Mode: Line-Locked

Input Format: 13.5 MHz Composite Video

Output Format: RGB (0-1023)

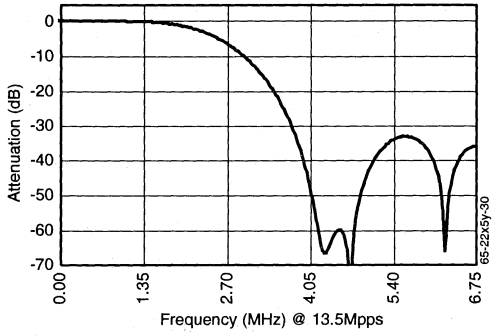
Decoder: Adaptive 3-Line Chroma Comb Filter

Register Map:

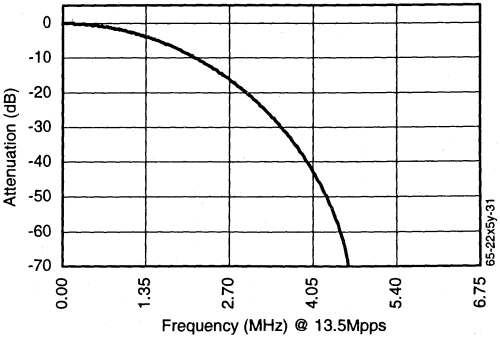
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C3	01	00	20	20	00	20	04	40	08	00	03	80	C4	24	09
1	60	53	32	BE	23	00	01	00	CA	A6	OC	5A	00	00	00	00
2	90	15	13	54	00	00	00	xx	xx	xx	xx	xx	xx	xx	xx	xx

The DRS appears on the G/Y output at the PXCK rate. Luma adaptive notch filter ANF1.

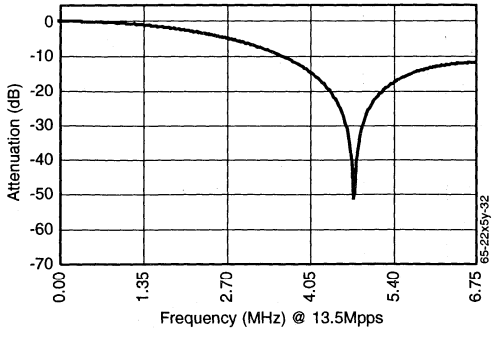
Bandsplit Filter (BSF 2)



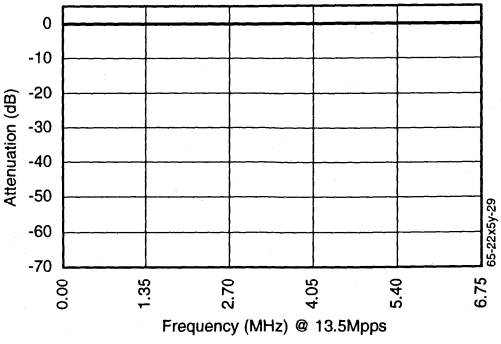
Demodulation Filter (LPF 2)



Adaptive Notch Filter (CF-1)



Notch Filter (bypassed)



Programming Examples (continued)

Standard: NTSC-M

Mode: Genlock (TMC22071)

Input Format: 13.5 MHz Composite Video

Output Format: YUV with syncs on Y

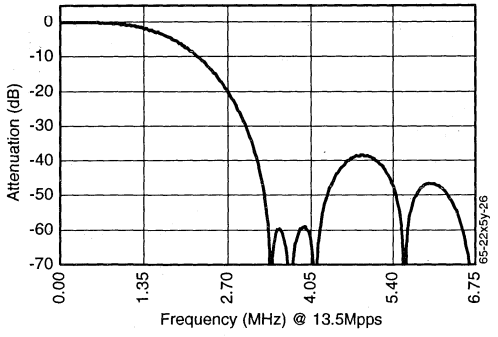
Decoder: Simple bandsplit decoder (0H delay)

Register Map:

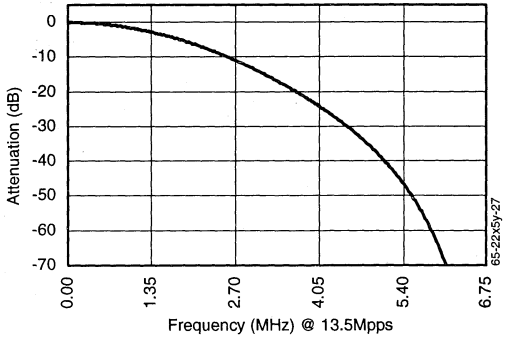
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C0	21	60	A1	20	2C	00	00	40	00	30	03	83	0C	3F	09
1	5A	50	2E	C8	23	00	00	00	00	00	00	49	F0	01	00	00
2	40	F8	E0	43	00	00	00	xx	xx	xx	xx	xx	xx	xx	xx	xx

The DRS appears on the G/Y output at the PXCK rate.

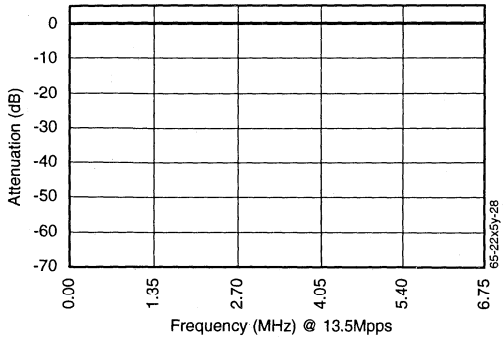
Bandsplit Filter (BSF 1)



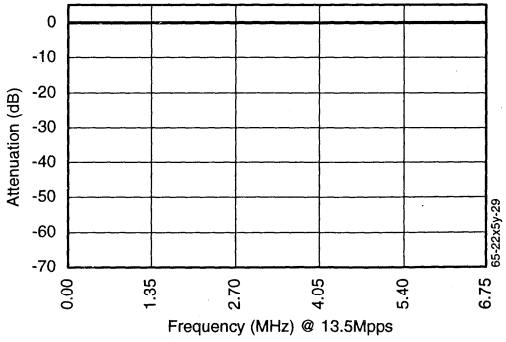
Demodulator Filter (LPF 1)



Adaptive Notch Filter (bypassed)



Notch Filter (bypassed)



Programming Examples (continued)

Standard: PAL-I

Mode: Genlock (TMC22071)

Input Format: 13.5 MHz Composite Video

Output Format: YUV outputs with syncs on Y

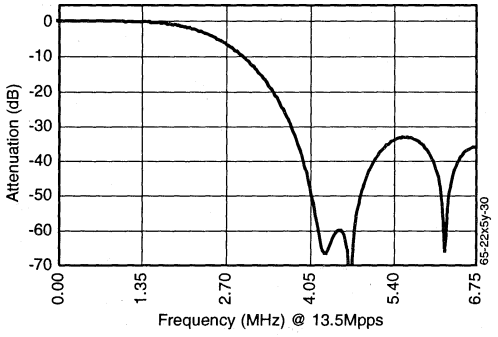
Decoder: Simple bandsplit decoder (1H delay)

Register Map:

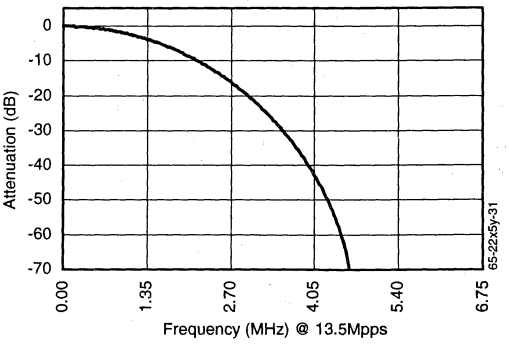
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C3	21	60	20	20	00	00	05	40	08	30	03	80	CC	3F	09
1	60	53	39	BE	23	00	01	00	00	00	00	49	00	05	00	00
2	90	15	13	54	00	00	00	xx	xx	xx	xx	xx	xx	xx	xx	xx

The DRS appears on the G/Y output at the PXCK rate.

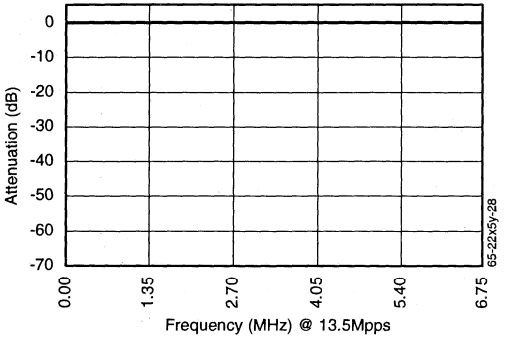
Bandsplit Filter (BSF 2)



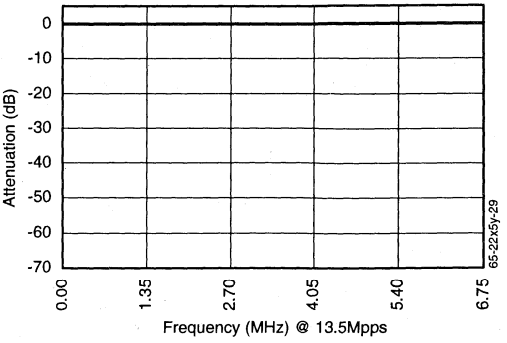
Demodulation Filter (LPF 2)



Adaptive Notch Filter (bypassed)



Notch Filter (bypassed)



Programming Examples (continued)

Standard: NTSC-M

Mode: Subcarrier mode (TRS-ID disabled)

Input Format: 14.32 MHz (4*Fsc) Composite Video

Output Format: RGB outputs with syncs on green

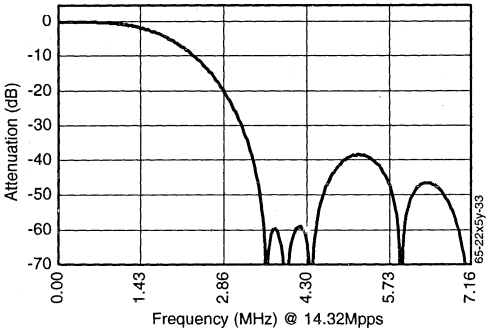
Decoder: Adaptive 3-Line Chroma Comb Filter

Register Map:

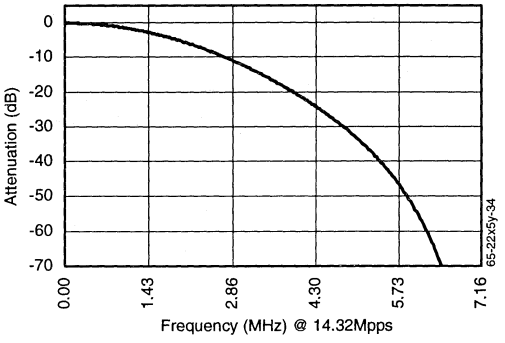
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C0	00	18	E1	20	2C	00	00	40	40	12	02	00	04	24	09
1	8E	55	7D	00	33	00	01	3F	59	C0	8B	51	24	05	00	00
2	00	00	00	40	00	00	00	xx	xx	xx	xx	xx	xx	xx	xx	xx

The DRS appears on the G/Y output at the PXCK rate. Simple color correction YBAL enabled.

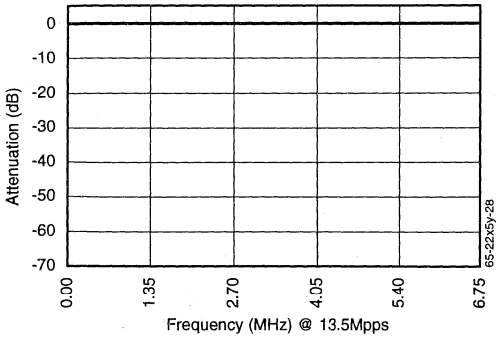
Bandsplit Filter (BSF 1)



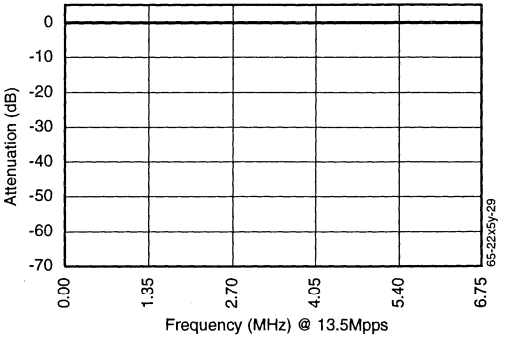
Demodulator Filter (LPF 1)



Adaptive Notch Filter (bypassed)



Notch Filter (bypassed)



Programming Examples (continued)

Standard: NTSC-M

Mode: Subcarrier mode (TRS-ID enabled)

Input Format: Deserialized D2 Composite Video signal

Output Format: RGB outputs with syncs on green

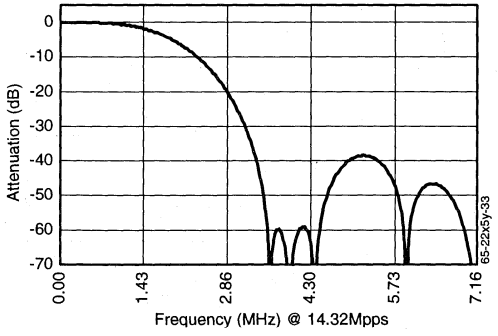
Decoder: Simple bandsplit decoder

Register Map:

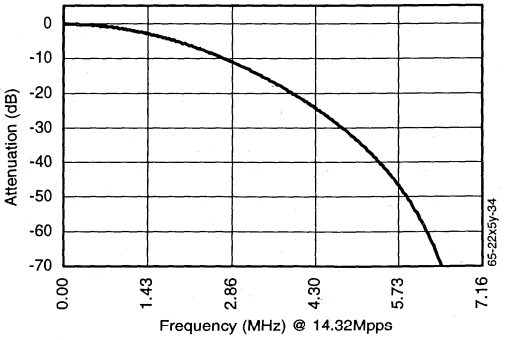
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C0	18	18	E1	20	2C	01	00	40	40	12	02	00	04	24	09
1	8E	55	7D	00	33	00	0C	3F	59	C0	8B	51	24	05	00	00
2	00	00	00	40	00	00	00	xx	xx	xx	xx	xx	xx	xx	xx	xx

The DRS appears on the G/Y output at the PXCK rate. Luminance from notched input and chrominance from the bandsplit filter.

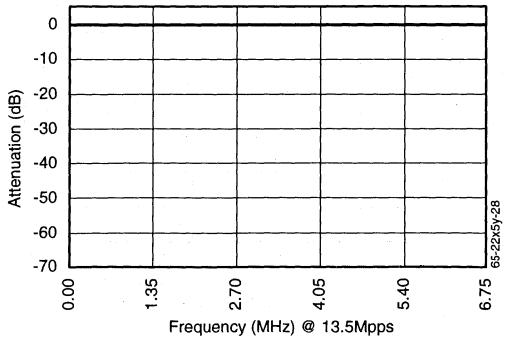
Bandsplit Filter (BSF 1)



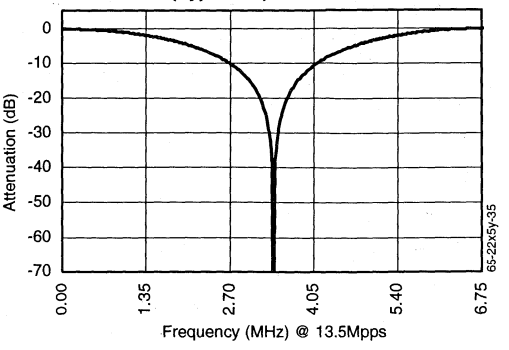
Demodulator Filter (LPF 1)



Adaptive Notch Filter (bypassed)



Notch Filter (bypassed)



Programming Examples (continued)

Standard: PAL-I

Mode: Subcarrier mode (TRS-ID enabled)

Input Format: Deserialized D2 Composite Video Signal

Output Format: RGB output with syncs on green

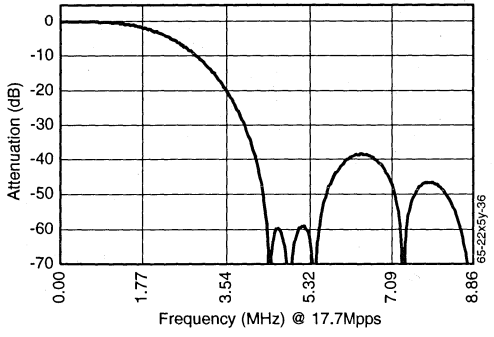
Decoder: Adaptive 3-Line Chroma Comb Filter

Register Map:

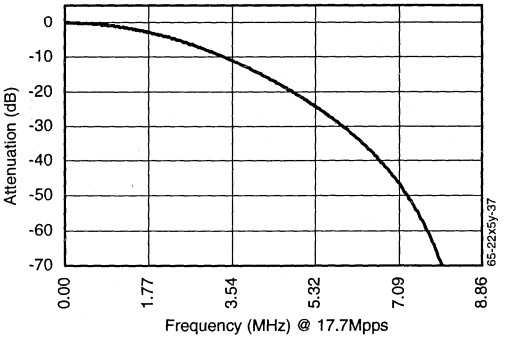
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C3	00	18	61	20	00	00	05	40	58	12	02	80	C4	24	09
1	6F	6F	4E	B4	34	00	04	50	3F	8B	6D	51	33	05	00	00
2	00	00	00	40	00	00	00	xx	xx	xx	xx	xx	xx	xx	xx	xx

The DRS appears on the G/Y output at the PXCK rate.

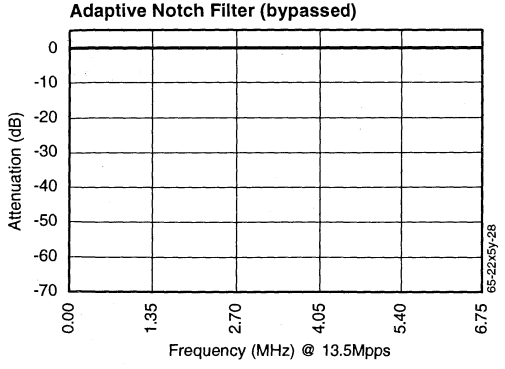
Bandsplit Filter (BSF 1)



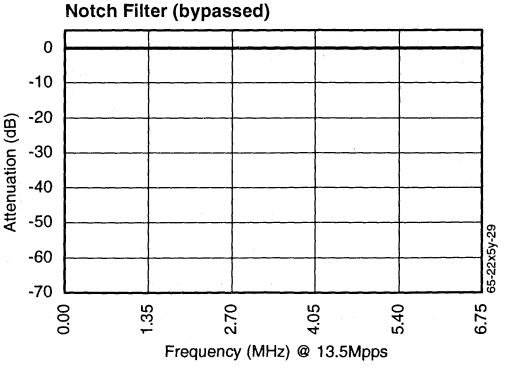
Demodulator Filter (LPF 1)



Adaptive Notch Filter (bypassed)



Notch Filter (bypassed)



Programming Examples (continued)

Standard: NTSC-M

Mode: D1 Mode

Input Format: D1, $C_BYC_R[Y]$ multiplexed data with embedded TRS words

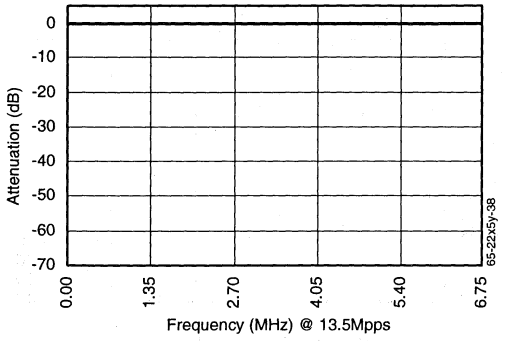
Output Format: YC_BC_R outputs

Decoder: Simple transcoder

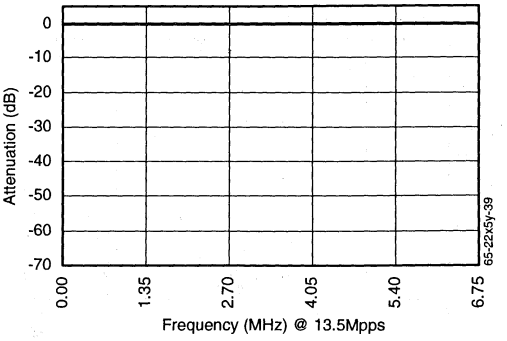
Register Map:

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C0	1F	37	02	20	00	00	08	40	00	26	E0	8D	0C	2B	0B
1	5A	50	2E	C8	23	00	0A	00	00	00	00	49	40	00	00	00
2	00	00	00	00	00	00	00	xx	xx	xx	xx	xx	xx	xx	xx	xx

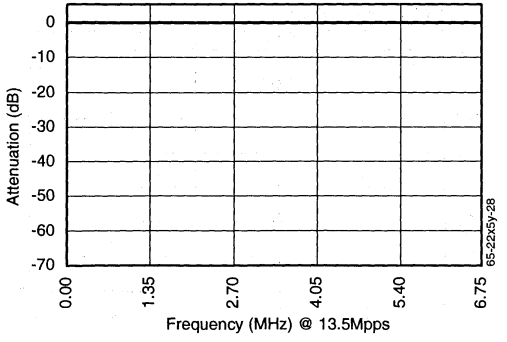
Bandsplit Filter (bypassed)



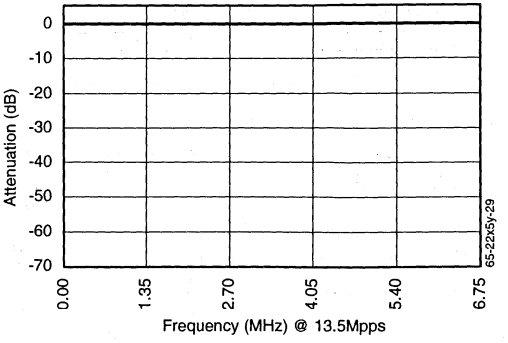
Demodulation Filter (bypassed)



Adaptive Notch Filter (bypassed)



Notch Filter (bypassed)



Programming Examples (continued)

Standard: NTSC-M

Mode: Line-Locked

Input Format: 13.5 MHz YC data, chroma externally delayed by 1H

Output Format: YUV with syncs on Y

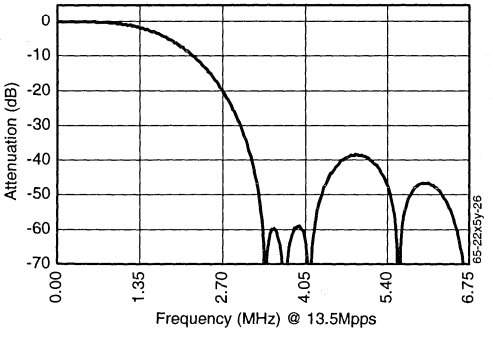
Decoder: Adaptive 3-Line Luma Comb Filter

Register Map:

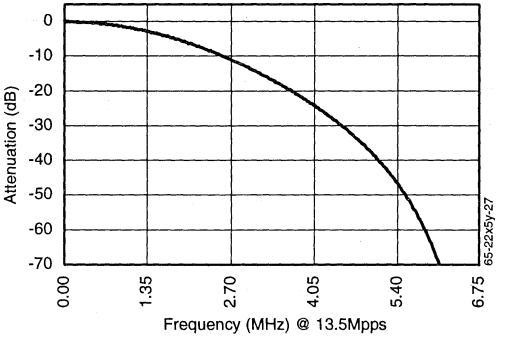
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C0	01	00	A1	20	00	00	01	40	00	12	03	10	04	22	03
1	5A	50	26	D8	23	00	01	00	00	00	00	49	F0	01	00	00
2	40	F8	E0	43	00	00	00	xx	xx	xx	xx	xx	xx	xx	xx	xx

The DRS appears on the G/Y output at the PXCK rate.

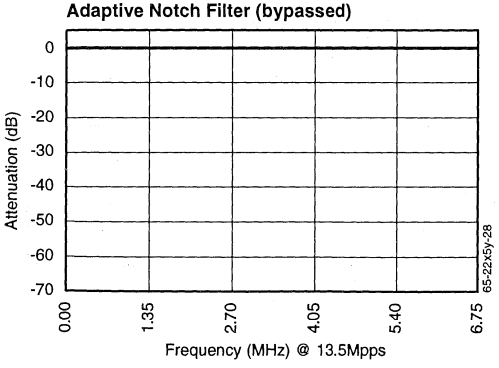
Bandsplit Filter (BSF 1)



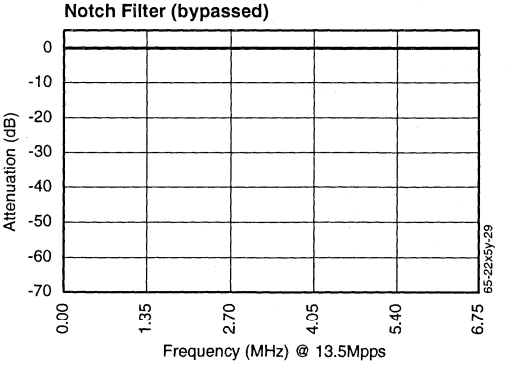
Demodulator Filter (LPF 1)



Adaptive Notch Filter (bypassed)



Notch Filter (bypassed)



Programming Examples (continued)

Standard: PAL-I

Mode: Line-Locked

Input Format: 13.5 MHz YC data, Chroma externally delayed by 1H

Output Format: YUV with syncs on Y

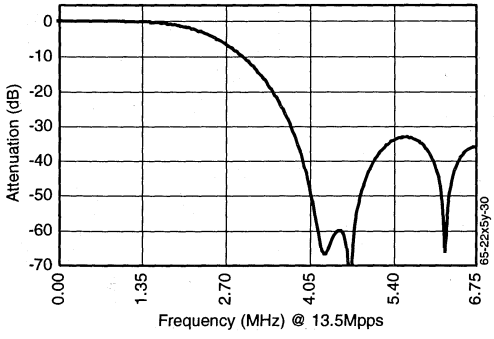
Decoder: Adaptive 3-Line Luma Comb Filter

Register Map:

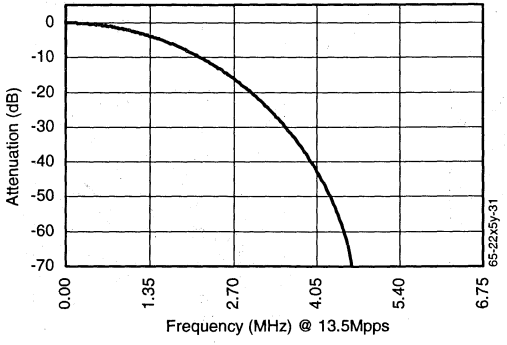
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C3	01	00	20	20	00	00	00	40	08	12	03	90	C4	22	03
1	60	53	31	CE	23	00	01	00	00	00	00	49	00	05	00	00
2	90	15	13	54	00	00	00	xx	xx	xx	xx	xx	xx	xx	xx	xx

The DRS appears on the G/Y output at the PXCK rate.

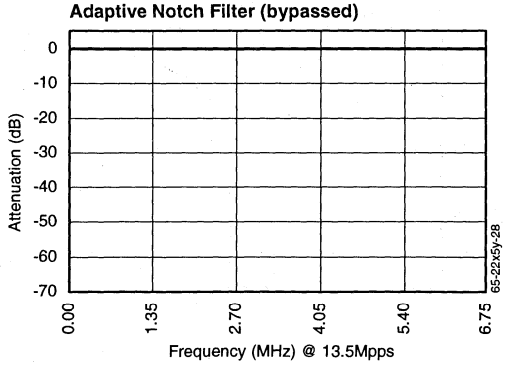
Bandsplit Filter (BSF 2)



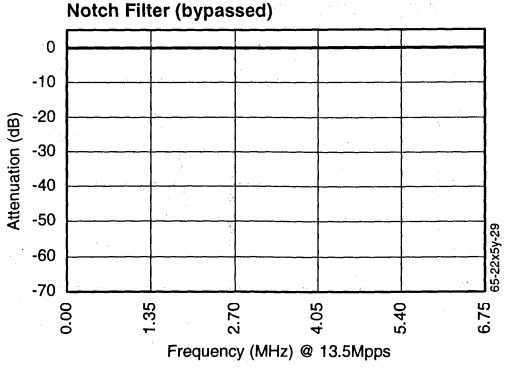
Demodulation Filter (LPF 2)



Adaptive Notch Filter (bypassed)



Notch Filter (bypassed)



Programming Worksheet

Standard:

Mode:

Input Format:

Output Format:

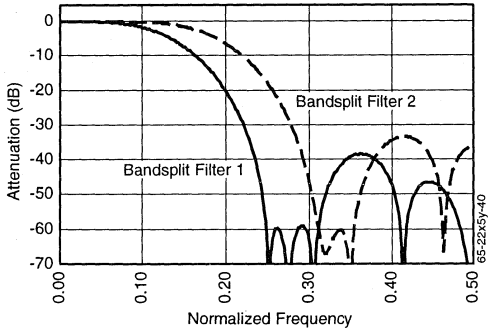
Decoder:

Register Map:

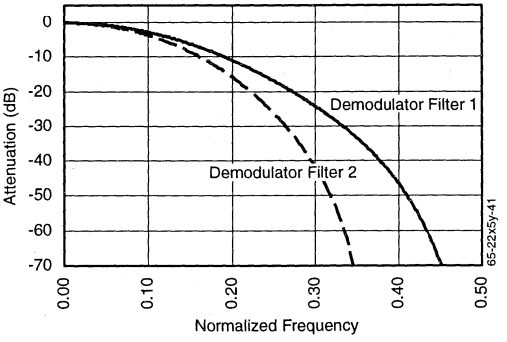
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2								XX	XX	XX	XX	XX	XX	XX	XX	XX

The DRS appears on the output at the rate.

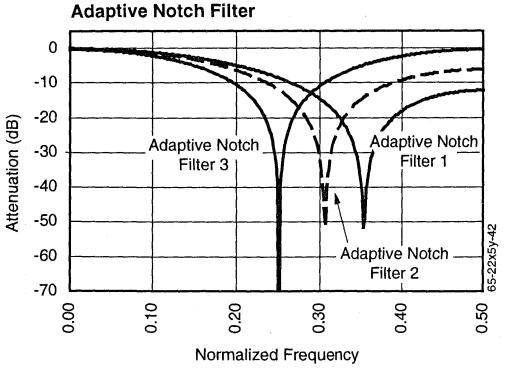
Bandsplit Filter



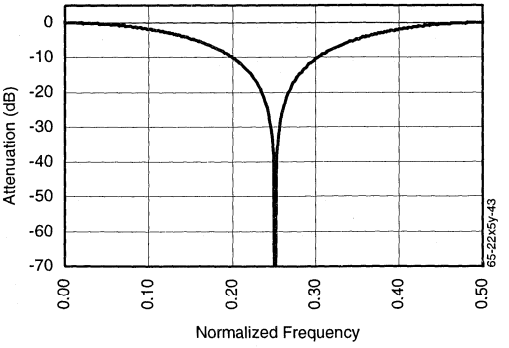
Demodulation Filter



Adaptive Notch Filter



Non-Adaptive Notch Filter



Related Products

- TMC22071 Genlocking Video Digitizer
- TMC22x9x Digital Video Encoders
- TMC2081 Digital Video Mixer
- TMC3003 Triple 10-bit D/A Converter

Ordering Information

Product Number	Temperature Range	Decoding	Resolution	Package	Package Marking
TMC22051KHC	0°C to 70°C	Simple	8 bit	100-Lead MQFP	22051KHC
TMC22052KHC	0°C to 70°C	2-Line Comb	8 bit	100-Lead MQFP	22052KHC
TMC22053KHC	0°C to 70°C	3-Line Comb	8 bit	100-Lead MQFP	22053KHC
TMC22151KHC	0°C to 70°C	Simple	10 bit	100-Lead MQFP	22151KHC
TMC22152KHC	0°C to 70°C	2-Line Comb	10 bit	100-Lead MQFP	22152KHC
TMC22153KHC	0°C to 70°C	3-Line Comb	10 bit	100-Lead MQFP	22153KHC

THIS PAGE INTENTIONALLY LEFT BLANK

TMC22091/TMC22191

Digital Video Encoders/Layering Engine

Features

- All-digital video encoding
- Internal digital oscillators, no crystals required
- Multiple input formats supported
  - 24-bit and 15-bit GBR/RGB
  - YC_BC_R422 or 444
  - Color indexed
- 30 overlay colors (TMC22191)
- Fully programmable timing
- Supports input pixel rates of 10 to 15 Mpps
- 256 x 8 x 3 color look-up tables (bypassable on TMC22191)
- 8-bit mask register
- 8-bit composite digital video input
- Hardware and 24-bit data keying
- Synchronizes with TMC22071 Genlocking Video Digitizer
- 8:8:8 video reconstruction
- SMPTE 170M NTSC or CCIR Report 624 PAL compatible
- Supports PAL-M and NTSC without pedestal
- Simultaneous S-VIDEO (Y/C) NTSC/PAL output
- 10-bit D/A conversion (three channels)
- Controlled edge rates
- 3 power-down modes
- Built-in color bars and modulated ramp test signals
- JTAG (IEEE Std 1149.1-1990) test interface
- Single +5V power supply
- 84 lead PLCC package

Description

The TMC22x91 digital video encoders convert digital computer image or graphics data (in RGB, YCBCR, or color indexed format) or a CCIR-601 signal into a standard analog baseband television (NTSC or PAL) signal with a modulated color subcarrier.

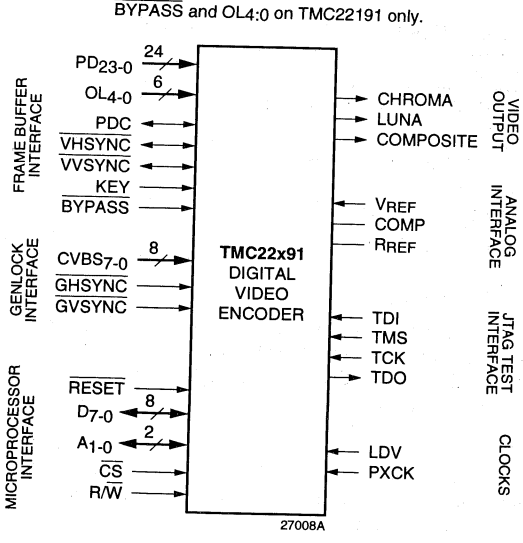
Both composite (single lead) and S-VIDEO (separate chroma and luma) formats are active simultaneously at the three analog output pins, each of which generates a standard video-level signal into doubly-terminated 75Ω load.

The TMC22x91 accepts digitized video from the companion TMC22071 Genlocking Video Digitizer. Soft switching between video sources is done under either hardware or programmable data control.

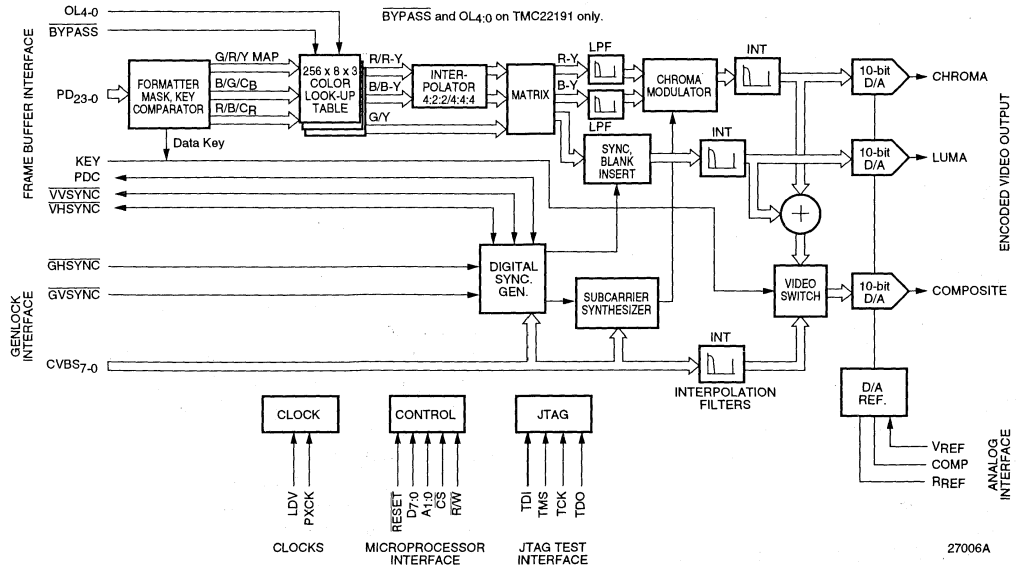
The TMC22191 offers 4-layer keying capability, bypassable CLUT, and 30 Overlay colors.

The TMC22x91 is fabricated in a submicron CMOS process and packaged in an 84 Lead Plastic Leadless Chip Carrier. Performance is guaranteed from 0°C to 70°C.

Logic Symbol



Block Diagram



Functional Description

The TMC22091 and TMC22191 are totally integrated, fully-programmable digital video encoders with simultaneous composite and Y/C (S-VIDEO) outputs. The TMC22x91 video outputs are compatible with SMPTE 170M NTSC, CCIR Report 624 PAL, PAL-M, and NTSC without pedestal television standards. No external component selection or tuning is required.

The encoders accept digital image data at the PD port in one of several formats, which are matrixed into luminance and chrominance components. The chrominance signals are modulated onto a digitally synthesized subcarrier. The luminance and chrominance signals are separately interpolated to twice the pixel rate, and converted to analog levels by 10-bit D/A converters. They are also digitally combined and the resulting composite signal is output by a third 10-bit D/A converter. This composite signal may be keyed (pixel rate switching) with a second composite digital video signal presented to the encoder.

The output video frames may be internally timed by the TMC22x91, synchronized with the external frame buffer, or slaved to the companion Genlocking Video Digitizer (TMC22071). All operational parameters are fully programmable over a standard microprocessor port.

Table 1 shows the key features that distinguish between the TMC22091 and TMC22191. All of the information presented in this data sheet applies to both products unless otherwise noted. Statements, paragraphs, tables, and figures that apply to only one or two of the encoders have notation specifying the applicable part number.

Timing

The encoder operates from a single clock at twice the system pixel rate. This frequency may be set between 20 MHz and 36 MHz (pixel rates of 10 Mpps to 18 Mpps). Within this range are included CCIR-601, D2, and square-pixel formats, as well as a variety of computer-specific pixel rates. An array of programmable timing registers allows the software selection of all pertinent signal parameters to produce NTSC (with or without 7.5 IRE pedestal) and PAL, and PAL-M outputs.

Table 1. Comparing the TMC22x91 Encoders

Feature	TMC22091	TMC22191
OL4-0 pixel inputs for 30 overlay colors	No	Yes
Number of video layers supported	2	4
BYPASS input for bypassing CLUTs	No	Yes

Input Formatting

The input section accepts a variety of video and graphics formats, including 24-bit GBR and RGB, 15-bit GBR and RGB, YCBCR422, YCBCR444, and 8-bit color-indexed data (Figure 1a and 1b).

The input section of the TMC22x91 includes a key comparator which monitors the pixel data port with three independent 8-bit comparators, and invokes a video key when the selected registers match the incoming data.

Mask Register

A Mask Register is provided which is logically ANDed with incoming color-index data to facilitate pixel animation and other special graphics effects. The Mask Register is ahead of the Data Key comparators and is enabled only when color-index input is selected. Mask Register programming and operation are similar to that of the 171/176 family of graphics RAMDACS.

Color Lookup Table

The Color Lookup Table (CLUT) is a 256 x 8 x 3 random-access memory. It provides means for offset, gain, gamma, and color correction in RGB and YC_BC_R operating modes. It provides a full 24-bit color lookup function for color-index mode. It can be loaded in the same manner as a standard VGA RAMDAC.

Colorspace Conversion Matrix and Interpolator

The matrix converts RGB data (whether from RGB inputs or color-indexed CLUT data) into Y, B-Y, R-Y format for encoding. In input configurations where the pixel input is already in Y, B-Y, R-Y format, the matrix is bypassed. When pixel data is input in YC_BC_R422 format, the interpolation filters produce YC_BC_R444 for encoding.

Sync Generator

The TMC22x91 can operate in Master, Genlock, or Slave modes. In Master and Genlock modes, the encoder internally generates all timing and sync signals, and provides Horizontal Sync, Vertical Sync, and Pixel Data Control (PDC) to the external frame buffer circuitry. PDC is independently selectable to function as an input or an output. In Genlock mode, the TMC22x91 timing is controlled by the TMC22071 Genlocking Video Digitizer over the $CVBS_{7-0}$ bus, $\overline{GVSYNC}$, and $\overline{GHSYNC}$. The encoder, in turn, produces $\overline{VHSYNC}$, $\overline{VVSYNC}$, and PDC for the frame buffer interface.

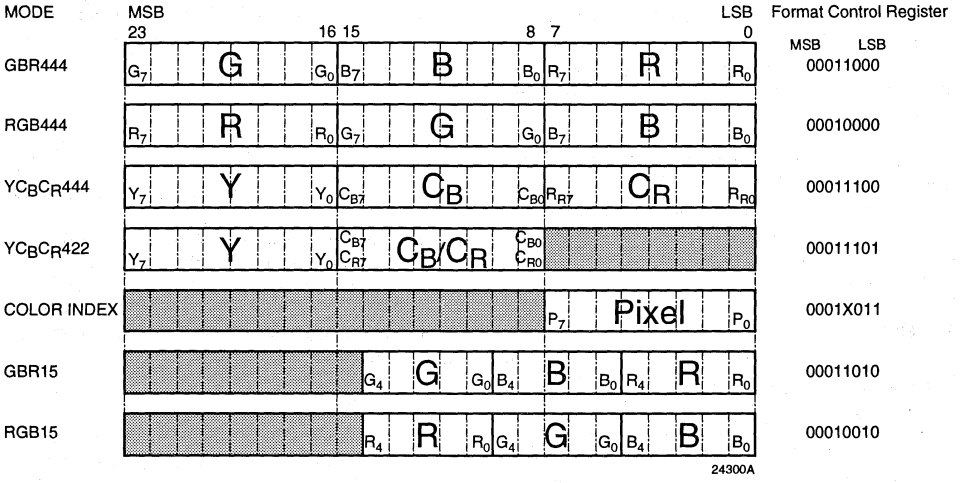


Figure 1a. Pixel Data Format

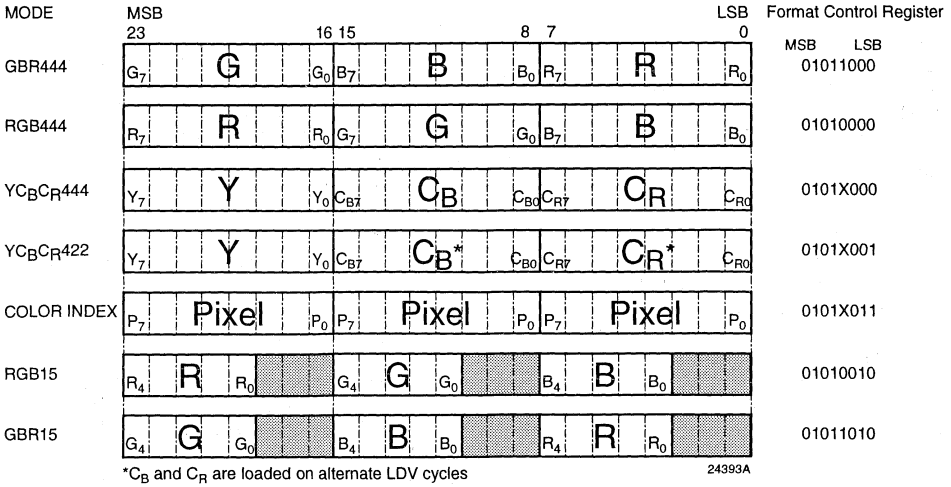


Figure 1b. Pixel Data Format (TMC22191 when CLUTs are Bypassed)

In Slave mode, $\overline{\text{VHSYNC}}$, $\overline{\text{VVSYNC}}$, and PDC (optional) are inputs to the TMC22x91. These inputs determine when new lines, frames, and active picture areas begin. The external controlling circuitry needs to establish the correct timing for these signals.

Horizontal and vertical synchronization signals are digitally generated by the TMC22x91 with controlled rise and fall times on all sync edges, the beginning and end of active video, and the burst envelope. All elements of horizontal sync timing are programmable, as are the frequency, phase, and duration of color burst.

Video Input

The TMC22x91 accepts genlocked synchronization data and digital composite video signals from the TMC22071 Genlocking Video Digitizer over the 8-bit CVBS bus. The encoder synchronizes its digital subcarrier oscillator to the video input from the TMC22071 with this data. The composite video data output from the TMC22071 is passed to the internal video switch for keying with the encoded pixel data.

Chroma Modulator

A 32-bit digital subcarrier synthesizer feeds a quadrature modulator, producing a digital chrominance signal. The relative phases of the burst and active video portions of the subcarrier can be individually adjusted to compensate for external phase errors and to effect a hue control.

Interpolation Filters

Interpolation filters on the luminance and chrominance signals double the pixel rate in preparation for D/A conversion. This band-limited process greatly simplifies the output filtering required following the D/A converters and dramatically reduces sin(x)/x distortion.

An interpolation filter on the CVBS data similarly raises the sample rate of the video signal, for mixing with the encoded pixel data.

Composite Video Switch

The Composite Video Switch selects between the composite video input (CVBS) and the composite encoded pixel data on a pixel-by-pixel basis, under the control of a key function.

Keying may be managed by hardware or software. The hardware key input (KEY pin) directly controls the video switch. The encoder may be programmed to operate with a data key, represented by three 8-bit registers that compare with the 24 input bits. They operate in all input modes and may be individually enabled or disabled.

D/A Converters

The analog outputs of the TMC22x91 are the outputs of three 10-bit D/A converters, operating at twice the pixel clock rate. The outputs are capable of driving standard video levels into a doubly-terminated 75Ω coaxial video cable (37.5Ω total load). An internal voltage reference is provided which can be used to provide reference current for the three D/A converters. For accurate video levels, an external fixed or variable voltage reference source is recommended. The video signal levels from the TMC22x91 may be adjusted to overcome the insertion loss of analog low-pass output filters.

The D/A converters on the TMC22x91 may be powered-down via Control Register 0E bits 5 and 6. The COMPOSITE D/A is controlled by bit 6 and the LUMA and CHROMA D/A converters are controlled by bit 5.

Microprocessor Interface

The microprocessor interface employs a 13 line format. The $\overline{\text{RESET}}$ pin sets all internal state machines to their initialized conditions, disables the analog outputs, sets the internal $\overline{\text{SRESET}}$ bit LOW (reset condition), and places the encoder in a power-down mode. All register and CLUT data are maintained in power-down mode. If the HRESET bit is set HIGH, line 1 field 1 is started when $\overline{\text{RESET}}$ goes HIGH, and $\overline{\text{SRESET}}$ is ignored. If HRESET is LOW, the encoder remains idle after $\overline{\text{RESET}}$ goes HIGH until Control Register bit $\overline{\text{SRESET}}$ is set HIGH, which initiates line 1 field 1.

Two address lines are provided and decoded for access to the internal Control Registers and CLUT. Control Registers and CLUT are accessed by loading a desired address through the 8-bit D_{7-0} port, followed by the desired data read or write for that address. Both the CLUT and the Control Registers are self-indexing, allowing continuous reads or writes to successive addresses.

JTAG Test Interface

The TMC22x91 includes a standard 4-line JTAG (IEEE Std 1149.1-1990) test interface port, providing access to all digital input/output data pins. This is provided to facilitate component and board-level testing.

Test/Validation Mode

The TMC22x91 may be configured to produce standard color bars or a 40 IRE modulated (or unmodulated) video ramp, independent of any pixel or video data input. Color bars are useful as an idle system output signal. The test signals may be used to verify proper operation of the analog video signal chain.

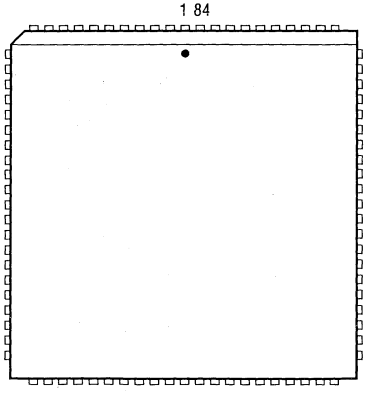
TMC22090/TMC22190 Compatibility

The TMC22090 and TMC22190 are earlier versions of the TMC22091 and TMC22191, respectively. They lack the following features of the newer versions:

1. Selectable Setup (to support NTSC EIA-J video output for Japan)
2. PAL-M format (for South American applications)
3. Extended EH and SL intervals (to support pixel rates above 15 Mpps)
4. Individual D/A power-down (to reduce total dissipation when some outputs are not required)
5. Luminance I/O processing (to reduce flicker in graphics applications)

These features are controlled by registers 0E and 0F, and enabled by setting Register OE bit 7 to ONE. If an application of the TMC22x90 is programmed with this bit set to ZERO (as recommended in the product documentation) then the corresponding TMC22x91 will perform identically. Though the earlier parts continue to be available, it is recommended that the newer devices be used in new designs for the additional flexibility. Older designs may be readily converted to the newer versions to take advantage of the added features and lower cost of the later technology.

Pin Assignments



65-3751-01

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	$CVBS_2$	22	TDO	43	V_{DDA}	64	V_{DD}
2	$CVBS_1$	23	TCK	44	$CVBS_7$	65	D_{GND}
3	$CVBS_0$	24	TMS	45	$CVBS_6$	66	PD_{11}
4	KEY	25	TDI	46	$CVBS_5$	67	PD_{10}
5	$\overline{RESET}$	26	D_{GND}	47	$CVBS_4$	68	PD_9
6	$\overline{CS}$	27	V_{DD}	48	OL_3 (TEST)	69	PD_8
7	R/W	28	BYPASS (TEST)	49	OL_2 (TEST)	70	PD_7
8	A_1	29	OL_4 (TEST)	50	OL_1 (TEST)	71	PD_6
9	A_0	30	V_{REF}	51	OL_0 (TEST)	72	PD_5
10	D_{GND}	31	R_{REF}	52	PD_{23}	73	PD_4
11	PDC	32	A_{GND}	53	PD_{22}	74	PD_3
12	$\overline{VHSYNC}$	33	COMPOSITE	54	PD_{21}	75	PD_2
13	$\overline{VVSYNC}$	34	A_{GND}	55	PD_{20}	76	PD_1
14	D_7	35	LUMA	56	PD_{19}	77	PD_0
15	D_6	36	A_{GND}	57	PD_{18}	78	LDV
16	D_5	37	CHROMA	58	PD_{17}	79	PXCK
17	D_4	38	A_{GND}	59	PD_{16}	80	D_{GND}
18	D_3	39	COMP	60	PD_{15}	81	V_{DD}
19	D_2	40	V_{DDA}	61	PD_{14}	82	$\overline{GVSYNC}$
20	D_1	41	V_{DDA}	62	PD_{13}	83	$\overline{GHSYNC}$
21	D_0	42	V_{DDA}	63	PD_{12}	84	$CVBS_3$

Note: Pin names in parentheses apply to TMC22091.

Pin Descriptions

Pin Name	Pin Number	Value	Pin Function Description
Clocks			
PXCK	79	TTL	**Master Clock Input.** This 20 to 30 MHz clock is internally divided by 2 to generate the internal pixel clock, PCK, which a LOW on $\overline{RESET}$ forces LOW. PXCK drives the entire TMC22x91, except the asynchronous microprocessor interface and the semi-synchronous LDV data input clock. All internal registers are strobed on the rising edge of PXCK.
LDV	78	TTL	**Pixel Data Load Clock.** On each rising edge of LDV, data on PD_{23-0} are latched into the input preload register, for transfer into the input demultiplexer on the next rising edge of PCK.
Frame Buffer Interface			
PD_{23-0}	52-63, 66-77	TTL	**Pixel Data Inputs.** In YC_BC_R, GBR, RGB, and color-indexed mode. pixel data enter the TMC22x91 on PD_{23-0}. The specific format is found in Figures 1a and 1b. LDV is the clock that controls the loading of pixel data.
$\overline{VHSYNC}$	12	TTL	**Horizontal Sync I/O.** In Master and Genlock modes, the TMC22x91 outputs horizontal sync on this pin. In Slave modes, the TMC22x91 accepts and locks to horizontal sync input on this pin (with vertical sync on $\overline{VVSYNC}$). $\overline{VHSYNC}$ and $\overline{VVSYNC}$ must be coincident since they are clocked into the TMC22x91 on the same rising edge of PXCK.

Pin Descriptions (continued)

Pin Name	Pin Number	Value	Pin Function Description
$\overline{VVSYNC}$	13	TTL	**Vertical Sync I/O.** In separate V and H sync Master and Genlock modes, the TMC22x91 outputs vertical block sync ($\overline{VVSYNC}$ LOW for the 2.5 (PAL) or 3 (NTSC) lines on which vertical sync pulses occur). In composite sync (H and V sync on same signal) Master and Genlock modes, the TMC22x91 outputs horizontal sync, vertical sync, and equalization over this pin. In Slave mode, the TMC22x91 accepts and locks to vertical sync input on this pin (with horizontal sync on $\overline{VHSYNC}$). $\overline{VHSYNC}$ and $\overline{VVSYNC}$ must be coincident such that they are clocked into the TMC22x91 on the same rising edge of PXCK.
PDC	11	TTL	**Pixel Data Control.** In Master mode, the TMC22x91 forces PDC HIGH when and only when it wants active video from the frame buffer. During blanking (syncs, equalization, burst, and porches), it forces PDC LOW, signaling that it will ignore any data presented over PD_{23-0}. When PDC is used as an input, forcing it HIGH allows the TMC22x91 to receive PD during the active video state.
KEY	4	TTL	**Hardware Key Input.** When the HKEN control bit is set HIGH and hardware key pin, KEY, is HIGH, video data entering on $CVBS_{7-0}$ are routed to the COMPOSITE output. This control signal is pipelined so the pixel that is presented to the PD port when the KEY signal is invoked is at the midpoint of the soft key transition. When HKEN is LOW, KEY is ignored. Like PD data, KEY is clocked into the TMC22x91 on the rising edge of LDV.
OL_{4-0}	29, 48-51	TTL	**Overlay Data Inputs (TMC22191 only).** 30 of the 256 locations of the CLUT may be reserved for overlay operation. These CLUT locations are directly accessed by five input pins, OL_{4-0}. OL_{4-0} are entered into the TMC22191 on a pixel-by-pixel basis and select which of the 30 overlay colors is to be encoded. When all five OL_{4-0} inputs are LOW, no overlay occurs.
$\overline{BYPASS}$	28	TTL	**CLUT Bypass Control (TMC22191 only).** When $\overline{BYPASS}$ is HIGH, the CLUT is in the pixel data path within the TMC22191. When $\overline{BYPASS}$ is LOW, pixel data bypasses the CLUT. $\overline{BYPASS}$ is active only for certain modes of the Layering Control Register (LCR) when the Format Control Register bit 6 is HIGH.
Genlock Interface			
$\overline{GHSYNC}$	83	CMOS	**Genlock Horizontal Sync.** In Genlock mode, the TMC22x91 will start a new horizontal line (blank-to-sync-edge transition) with each falling edge of $\overline{GHSYNC}$. In non-genlock modes, the TMC22x91 ignores $\overline{GHSYNC}$. The internal pixel clock, PCK, is aligned with the falling edge of $\overline{VHSYNC}$ or $\overline{GHSYNC}$ (Genlock mode).
$\overline{GVSYNC}$	82	CMOS	**Genlock Vertical Sync.** In Genlock mode, the TMC22x91 will start a new vertical sync sequence at line 1 field 1 whenever $\overline{GVSYNC}$ and $\overline{GHSYNC}$ are coincident such that they are clocked into the TMC22x91 on the same rising edge of PXCK. If $\overline{GVSYNC}$ falls at any other time, the TMC22x91 will assume that this marks the start of field 2, and will ignore it (in odd-field sync mode) or (in all-field sync mode) respond by generating a single vertical sync pulse, followed by 2 (PAL) or 2.5 (NTSC) lines of vertical sync, keyed to the next falling edge on $\overline{GHSYNC}$. See Interface Control Register bit 0 for odd-field and all-field operation.

Pin Descriptions (continued)

Pin Name	Pin Number	Value	Pin Function Description
$CVBS_{7-0}$	44-47, 84, 1-3	TTL	**Composite Video Inputs.** The encoder receives digitized video, subcarrier phase, and subcarrier frequency over this 8-bit bus at the PCK rate. This data may be provided by the companion TMC22071 Genlocking Video Digitizer. In Genlock mode, the TMC22x91 expects subcarrier phase and frequency data during each line's horizontal sync interval, as well as video data when keying is engaged, transferred at the PCK rate.
Microprocessor Interface			
D_{7-0}	14-21	TTL	**Data I/O Port.** All control parameters are loaded into and read back over this 8-bit port. For digital testing, the five lower bits can also serve as a two-cycle 10-bit data output port. For D/A converter testing, it can be used as a 10-bit two-cycle input port, facilitating, for example, ramp-based D/A converter linearity tests.
A_{1-0}	8-9	TTL	**µProc Port Controls.** As in a RAMDAC, this control governs whether the microprocessor interface selects a table address or reads/writes table contents. It also governs setting and verification of the TMC22x91's internal operating modes, also over port D_{7-0}.
$\overline{CS}$	6	TTL	**Chip Select.** When $\overline{CS}$ is HIGH, the microprocessor interface port, D_{7-0}, is set to HIGH impedance and ignored. When $\overline{CS}$ is LOW, the microprocessor can read or write parameters over D_{7-0}. One additional falling edge of $\overline{CS}$ is needed to move input data to its assigned working registers.
$R/\overline{W}$	5	TTL	**Bus Read/Write Control.** When $R/\overline{W}$ and $\overline{CS}$ are LOW, the microprocessor can write to the control registers or CLUT over D_{7-0}. When $R/\overline{W}$ is HIGH and $\overline{CS}$ is LOW, it can read the contents of any CLUT address or control register over D_{7-0}.
$\overline{RESET}$	7	TTL	**Master Reset Input.** Bringing $\overline{RESET}$ LOW sets the software reset control bit, $\overline{SRESET}$, LOW, forcing the internal state machines to their starting states and disabling all outputs. Bringing $\overline{RESET}$ HIGH synchronizes the internal pixel clock (PCK = PXCK / 2) to maintain a defined pipeline delay through the TMC22x91. If HRESET is set HIGH, the encoder is enabled when $\overline{RESET}$ goes HIGH. If HRESET is LOW, the host restarts the TMC22x91 by setting $\overline{SRESET}$ HIGH. $\overline{RESET}$ does not affect the CLUT or the control registers, except $\overline{SRESET}$.
Video Output			
COMPOSITE	33	1 V_{P-P}	**NTSC/PAL Video.** Analog output of composite D/A converter, nominally 1.35 volt peak-to-peak into a 37.5Ω load.
LUMA	35	1 V_{P-P}	**Luminance-only Video.** Analog output of luminance D/A converter, nominally 1.35 volt peak-to-peak into a 37.5Ω load.
CHROMA	37	1 V_{P-P}	**Chrominance-only Video.** Analog output of chrominance D/A converter, nominally 1.35 volt peak-to-peak into a 37.5Ω load.
Analog Interface			
V_{REF}	30	+1.23 V	**Voltage Reference Input.** External voltage reference input, internal voltage reference output, nominally 1.235 V.
COMP	39	0.1 µF	**Compensation Capacitor.** Connection point for 0.1µf decoupling capacitor.
R_{REF}	31	392Ω	**Current-setting Resistor.** Connection point for external current-setting resistor for D/A converters. The resistor (392Ω) is connected between R_{REF} and A_{GND}. Output video levels are inversely proportional to the value of R_{REF}.

Pin Descriptions (continued)

Pin Name	Pin Number	Value	Pin Function Description
JTAG Test Interface			
TDI	25	TTL	**Data Input Port.** Boundary scan data input port.
TMS	24	TTL	**Scan Select Input.** Boundary scan (HIGH)/normal operation (LOW) selector.
TCK	23	TTL	**Scan Clock Input.** Boundary scan clock.
TDO	22	TTL	**Data Output Port.** Boundary scan data output port.
Power Supply			
V_{DD}	40-43	+5 V	**Positive digital power supply.**
V_{DDA}	27, 64, 81	+5 V	**Positive analog power supply.**
D_{GND}	32, 34, 36, 38	0.0 V	**Digital Ground.**
A_{GND}	10, 26, 65, 80	0.0 V	**Analog Ground.**
Test			
TEST	28, 29, 48-51	0.0 V	**Factory testing (TMC22091 only).** Reserved for factory testing. These pins have no effect on the operation but do function as JTAG registers. They should be grounded directly or pulled down to ground with 1kΩ or smaller resistors.

Control Registers

The TMC22x91 is initialized and controlled by a set of registers. The registers are organized into 13 categories:

1. Global Control
2. Format Control
3. Interface Control
4. Test Control
5. Key Control
6. Misc. Control
7. Standards Control
8. Layering Control (TMC22191)
9. Key Value
10. Timing
11. Subcarrier
12. Test I/O
13. Mask Register

An external controller loads the Control Registers through a standard interface port. It also loads the CLUT and reads its contents or those of the Control Registers. The port is governed by pins $\overline{CS}$, R/$\overline{W}$, and A_{1-0}.

The Address Register for the CLUT and the Control Register pointer automatically increment to allow successive writes to sequential addresses. In the CLUT, the Address Register has two additional bits which increment in modulo-three to sequentially access the red, green, and blue portions. All three colors must be written when any CLUT address is changed.

The control register autoincrement follows the sequence indicated in the Control Register Map. When it reaches address 40, it stops incrementing, allowing multiple reads or writes of test data from/to the TESTDAT register. To exit the test mode, reset the Control Register pointer by setting A_{1-0}, D_{7-0}, and R/$\overline{W}$ LOW and then bring $\overline{CS}$ LOW. Address 1F is a read-only status register. It is addressed by the autoincrement sequencer. Any data may be written into this port at that time but it will not be stored. When address 50 is accessed, no autoincrement takes place, allowing multiple writes to the Mask Register.

Table 2. Microprocessor Port Control

A_{1-0}	R/$\overline{W}$	Action
00	0	Write D_{7-0} into Control Register pointer
00	1	Read Control Register pointer on D_{7-0}
01	0	Write D_{7-0} into CLUT Address Pointer
01	1	Read CLUT Address Pointer on D_{7-0}
10	0	Write D_{7-0} to addressed Control Register
10	1	Read addressed Control Register on D_{7-0}
11	0	Write D_{7-0} to addressed CLUT location
11	1	Read addressed CLUT location on D_{7-0}

Table 3. Control Register Map

Reg	Bit	Name	Function
Global Control Register			
00	7-5		Reserved
00	4	$\overline{\text{SRESET}}$	Software reset
00	3	PAL	Standard select, NTSC or PAL
00	2	LUMDIS	Luminance input disable
00	1	CHRDIS	Chrominance input disable
00	0	HRESET	Software reset disable
Format Control Register			
01	7		Reserved
01	6	LCREN	Layering Control Register enable (TMC22191)
01	5	RAMPEN	Modulated ramp test
01	4	$\overline{\text{CB}}$	Color bar test
01	3-2	FORMAT	PD_{23-0} input format select
01	1-0	INMODE	PD_{23-0} input mode select
Interface Control Register			
02	7	VITSEN	VITS lines enable
02	6	SHCY	Short-cycle test mode
02	5-4	TBASE	Time-base source select
02	3	SOUT	Sync output mode select
02	2	FBDIS	Frame buffer signals disable
02	1	PDCDIR	PDC master, slave select
02	0	FLDLK	Field lock select
Test Control Register			
03	7		Reserved
03	6	LIMEN	Luminance limiter enable
03	5	TESTEN	Test enable
03	4	HOLDEN	MSBs/LSBs hold select
03	3	TSTMSB	LSBs, MSBs in/out select
03	2	LUMTST	LUMA channel test
03	1	8FSUBR	8-field subcarrier reset enable
03	0	CHRTST	CHROMA channel test
Key Control Register			
04	7		Reserved
04	6	HKEN	Hardware key enable
04	5	BUKEN	Burst key enable
04	4	SKEXT	Data key operation select
04	3	DKDIS	Green/red/Y data key disable
04	2	EKDIS	Blue/green/C_B data key disable
04	1	FKDIS	Red/blue/C_R data key disable
04	0	SKEN	Data key enable
Layering Control Register (TMC22191)			
04	7	LAYMODE	MSB of Layer Assignments select
04	6	HKEN	Hardware key enable
04	5	BUKEN	Burst key enable
04	4	SKEXT	Data key operation select
04	3-1	LAYMODE	LSBs of Layer Assignments select
04	0	SKEN	Data key enable
Key Value Registers			
05	7-0	DKEY	Green/red/Y data key value
06	7-0	EKEY	Blue/green/C_B data key value

Table 3. Control Register Map (continued)

Reg	Bit	Name	Function
07	7-0	FKEY	Red/blue/C_R data key value
08-0D			Reserved
Misc. Control Register			
0E	7	EFEN	Register 0E and 0F enable
0E	6	COMPD/A	COMPOSITE D/A disable
0E	5	SVIDD/A	LUMA/CHROMA D/A disable
0E	4	FKREN	Luminance processing enabled
0E	3	RATIO	Luminance ratio select
0E	2	TFLK	Luminance pass threshold select
0E	1	T512	EH/SL offset select
0E	0	CB100	NTSC/PAL Color Bars
Standards Control Register			
0F	7	EFEN	Same as Reg 0E bit 7 but read-only
0F	6	SIX25	625/525 line per frame select
0F	5	PALID	Phase alternate line select
0F	4	SETUP	7.5 IRE Pedestal Enable
0F	3-2	YGAIN	Luminance gain settings
0F	1-0	CGAIN	Chrominance gain settings
Timing Registers			
10	7-0	SY	Horizontal sync tip length
11	7-0	BR	Breezeway length
12	7-0	BU	Burst length
13	7-0	CBP	Color back porch length
14	7-0	XBP	Extended color back porch 8 LSB
15	7-0	VA	Active video 8 LSB
16	7-0	VC	Active video start 8 LSB
17	7-0	VB	Active video end 8 LSB
18	7-6	XBP	Extended color back porch 2 MSB
18	5-4	VA	Active video 2 MSB
18	3-2	VC	Active video start 2 MSB
18	1-0	VB	Active video end 2 MSB

Table 3. Control Register Map (continued)

Reg	Bit	Name	Function
19	7-0	FP	Front porch length
1A	7-0	EL	Equalization pulse LOW length
1B	7-0	EH	Equalization pulse HIGH length
1C	7-0	SL	Vertical sync LOW length
1D	7-0	SH	Vertical sync HIGH length
1E	7-0	CBL	Color bar length
1F	7-5	FIELD	Field identification
1F	4-0	LTYPE	Line type identification
Subcarrier Registers			
20	7-0	FREQL	Subcarrier frequency 4th byte (LSBs)
21	7-0	FREQ3	Subcarrier frequency 3rd byte
22	7-0	FREQ2	Subcarrier frequency 2nd byte
23	7-0	FREQM	Subcarrier frequency 1st byte (MSBs)
24	7-0	SYSPHL	Video phase offset LSBs
25	7-0	SYSPHM	Video phase offset MSBs
26	7-0	BURPHL	Burst phase offset LSBs
27	7-0	BURPHM	Burst phase offset MSBs
28-3F			Reserved
Test I/O Register			
40	7-0	TESTDAT	Test data input/output
Mask Register			
50	7-0	MASK	Mask register
Y-Component Register			
60	7-0	Y	Y-component input/ output

Notes:

1. Functions are listed in the order used for reading and writing.
2. For each register listed above, all bits not listed are reserved and should be set to zero to ensure proper operation.
3. The meaning of Register 04 (Key Control Register/Layering Control Register) is determined by Format Control Register bit 6 (TMC22191).

Control Register Definitions

Global Control Register (00)

7	6	5	4	3	2	1	0
Reserved			$\overline{\text{SRESET}}$	PAL	LUMDIS	CHRDIS	HRESET

Reg	Bit	Name	Function
00	7-5		Reserved.
00	4	$\overline{\text{SRESET}}$	Software reset. When LOW, resets and holds internal state machines and disables outputs. When HIGH (normal), starts and runs state machines and enables outputs.
00	3	PAL	Video standard select. When LOW, the NTSC standard is generated with 7.5 IRE pedestal. When HIGH, PAL standard video is generated. This bit is ignored if Register 0E bit 7 is HIGH, enabling the 0E and 0F registers.
00	2	LUMDIS	Luminance input disable. When LOW (normal), luminance (Y) data from external frame buffer is enabled. When HIGH, luminance (Y) data into the TMC22x91 is forced to 0 IRE but sync pulses continue from the LUMA output.
00	1	CHRDIS	Chrominance input disable. When LOW (normal), burst and frame buffer data into the TMC22x91 are enabled. when HIGH, burst and frame buffer data are suppressed, enabling monochrome operation.
00	0	HRESET	Software reset enable. $\overline{\text{SRESET}}$ is forced LOW when the $\overline{\text{RESET}}$ pin is taken LOW. State machines are reset and held. When HRESET is LOW, $\overline{\text{RESET}}$ may be taken HIGH at any time. The TMC22x91 is enabled and a new frame is begun with line 1, field 1 on the next PXCK after $\overline{\text{SRESET}}$ is set HIGH. The D/A converters are powered down while $\overline{\text{RESET}}$ is LOW. When HRESET is HIGH, a new frame is begun with line 1, field 1 on the next PXCK after $\overline{\text{RESET}}$ is taken HIGH. $\overline{\text{SRESET}}$ is ignored. The D/A converters remain active during the reset sequence.

Control Register Definitions (continued)

Format Control Register (01)

7	6	5	4	3	2	1	0
Reserved	LCREN	RAMPEN	$\overline{CB}$	FORMAT		INMODE	

Reg	Bit	Name	Function
01	7		Reserved.
01	6	LCREN	(TMC22191) Layering Control Register enable. When LOW, the Layering Control Register is not available and Key Control Register functions are enabled. In this mode, the TMC22191 functions like the TMC22091. When HIGH, the Layering Control Register takes the place of the Key Control Register and enables the layering functions. Data loaded into the Key or Layering Control Registers will remain but have a different meaning if this bit is changed.
01	5	RAMPEN	Modulated ramp test. When LOW (normal), the TMC22x91 encodes and outputs video corresponding to input data. When RAMPEN and $\overline{CB}$ are both HIGH, an internally generated 40 IRE modulated ramp is produced, preempting input data.
01	4	$\overline{CB}$	Color bar test. When HIGH (normal), the TMC22x91 encodes and outputs video corresponding to input data. When $\overline{CB}$, RAMPEN, and Format Control Register bit 0 are LOW, internally generated color bars are produced, preempting input data.
01	3-2	FORMAT	PD_{23-0} input format select. Two bits select RGB, GBR, or YC_BC_R input data. When bits 3 and 2 are: 0 0 the CLUT output is interpreted as RGB and is converted to YC_BC_R. 0 1 is reserved. Bits 3 and 2 must be 00 or 10 when the Layering Control Register is enabled (TMC22191). 1 0 the CLUT output is interpreted as GBR, and is converted to YC_BC_R. 1 1 the CLUT output is interpreted as YC_BC_R.
01	1-0	INMODE	PD_{23-0} input mode select. These two bits set up the TMC22x91 for either 444, 422, 15-bit, or 8-bit input modes. 0 0 24-bit/pixel GBR, RGB, or YC_BC_R444 data enters from PD_{23-0} 0 1 YC_BC_R422 data enters from PD_{23-8}; C_R and C_B alternate from PD_{15-8} 1 0 15-bit/pixel GBR or RGB data from PD_{14-0} 1 1 8-bit/pixel color indexed data enters from PD_{7-0}. Bits 1 and 0 must be 00, 01, or 11 when the Layering Control Register is enabled (TMC22191).

Control Register Definitions (continued)

Interface Control Register (02)

7	6	5	4	3	2	1	0
VITSEN	SHCY	TBASE		SOUT	FBDIS	PDCDIR	FLDLK

Reg	Bit	Name	Function
02	7	VITSEN	VITS lines enable. When LOW, all UBB lines in the vertical interval are black burst regardless of input data. When HIGH, all UBB lines in the vertical interval become UVV active video and are dependent upon input data.
02	6	SHCY	Short-cycle test mode. When LOW, normal operation is enabled. when HIGH, EH (equalization pulse HIGH length) and SL (vertical sync LOW length) are shortened by 256.
02	5-4	TBASE	Time-base source select. These two bits set up the TMC22x91 for either genlock or frame buffer control of timing. When bits 5 and 4 are: 0 0 the encoder counts out its own time-base from input clock PXCK. 0 1 the encoder locks to synchronizing signals from external genlock. 1 0 the encoder locks to synchronizing signals from frame buffer controller.
02	3	SOUT	Sync output mode select. When LOW, $\overline{\text{VHSYNC}}$ and $\overline{\text{VVSYNC}}$ output separate horizontal and vertical sync pulses. When HIGH, composite sync (H and V) is output on $\overline{\text{VVSYNC}}$ while horizontal sync is output on $\overline{\text{VHSYNC}}$.
02	2	FBDIS	Frame buffer signals enable. When LOW, $\overline{\text{VVSYNC}}$ and $\overline{\text{VHSYNC}}$ outputs to frame buffer are enabled. When HIGH, $\overline{\text{VVSYNC}}$ and $\overline{\text{VHSYNC}}$ outputs to frame buffer are disabled.
02	1	PDCDIR	PDC master/slave select. When LOW, PDC is an output where the encoder is requesting data from the frame buffer. When HIGH, PDC is an input, and directs the encoder to accept data from the frame buffer.
02	0	FLDLK	Field lock select. When LOW, (in Slave mode) the encoder locks to each new field. When HIGH, the encoder locks to field 1 only.

Control Register Definitions (continued)

Test Control Register (03)

7	6	5	4	3	2	1	0
Reserved	LIMEN	TESTEN	HOLDEN	TSTMSB	LUMTST	8FSUBR	CHRTST

Reg	Bit	Name	Function
03	7		Reserved.
03	6	LIMEN	Luminance limiter enable. When LOW, all luminance values are passed to modulator. when HIGH, luminance values are limited to 101 IRE.
03	5	TESTEN	Test enable. When LOW, normal operation is enabled. When HIGH, $TESTDAT_{7-0}$ (Register 40) is connected to the composite output (READ) and D/A converters (WRITE) for test.
03	4	HOLDEN	MSBs/LSBs hold select. When LOW, alternates MSBs and LSBs in test, at PXCK rate. When HIGH, reads/writes only MSBS or LSBS in test (per TSTMSB, bit 3)
03	3	TSTMSB	LSBS,MSBS hold select. When LOW, connects 2 LSBs to $TESTDAT_{1-0}$ for testing when TESTEN is HIGH. When HIGH, connects 8 MSBs to $TESTDAT_{7-0}$ for testing when TESTEN is HIGH.
03	2	LUMTST	LUMA channel test. When LOW (normal), the luminance D/A converter is driven from luminance channel. When HIGH, the luminance D/A converter is driven from TESTDAT for testing when TESTEN is HIGH.
03	1	8FSUBR	8-field subcarrier reset enable. When LOW, the internal subcarrier generator is reset with frequency and phase data from FREQ, SYSPH, and BURPH registers every eight fields. When HIGH, the internal subcarrier generator free-runs on the basis of frequency and phase data from the last time it was reset. When $\overline{RESET}$ goes LOW, the subcarrier frequency and phase will be reset from FREQ, SYSPH, and BURPH after field 8.
03	0	CHRTST	CHROMA channel test. When LOW (normal), the chrominance D/A converter is driven from chrominance channel. When HIGH, the chrominance D/A converter is driven from TESTDAT when TESTEN is HIGH.

Control Register Definitions (continued)

Key Control Register (04)

7	6	5	4	3	2	1	0
Reserved	HKEN	BUKEN	SKEXT	DKDIS	EKDIS	FKDIS	SKEN

Reg	Bit	Name	Function
04	7		Reserved.
04	6	HKEN	Hardware key enable. When LOW, the KEY input pin ignored. When HIGH, the KEY input pin is enabled.
04	5	BUKEN	Burst key enable. When LOW, output video burst is generated on TMC22x91. When HIGH, output burst is taken from genlock input data.
04	4	SKEXT	Data key operation select. When LOW, data keying is allowed only during active video. When HIGH, keying is allowed during active video and blanking.
04	3	DKDIS	Green/red/Y data key disable. When LOW, green/red/Y input data is enabled for data keying. When HIGH, green/red/Y input data is ignored for data keying. This function is enabled when Layering Control Register is enabled (TMC22191).
04	2	EKDIS	Blue/green/C_B data key disable. When LOW, Blue/green/C_B input data is enabled for data keying. When HIGH, Blue/green/C_B input data is ignored for data keying. This function is enabled when Layering Control Register is enabled (TMC22191).
04	1	FKDIS	Red/blue/C_R data key disable. When LOW, red/blue/C_R input data is enabled for data keying. When HIGH, red/blue/C_R input data is ignored for data keying. This function is enabled when Layering Control Register is enabled (TMC22191).
04	0	SKEN	Data key enable. When LOW, data keying is disabled. When HIGH, data keying is enabled.

Control Register Definitions (continued)

Layering Control Register (04) (TMC22191)

7	6	5	4	3	2	1	0
LAYMODE	HKEN	BUKEN	SKEXT	LAYMODE			SKEN

Reg	Bit	Name	Function
04	7	LAYMODE	MSB of Layer Assignments select.
04	6	HKEN	Hardware key enable. When LOW, the KEY input pin ignored. When HIGH, the KEY input pin is enabled.
04	5	BUKEN	Burst key enable. When LOW, output video burst is generated on TMC22191. When HIGH, output burst is taken from genlock input data.
04	4	SKEXT	Data key operation select. When LOW, data keying is allowed only during active video. When HIGH, data keying is allowed during active video and blanking.
04	3-1	LAYMODE	Three LSBs of Layer Assignments select.
04	0	SKEN	Data key enable. When LOW, data keying is disabled. When HIGH, data keying is enabled.

Key Value Registers (05-07)

Reg	Bit	Name	Function
05	7-0	DKEY	Green/red/Y data key value. Eight bits hold the match value which triggers keying on red/Y.
06	7-0	EKEY	Blue/green/U data key value. Eight bits hold the match value which triggers keying on green/U.
07	7-0	FKEY	Red/blue/V key value. Eight bits hold the match value which triggers keying on blue/V.

Control Register Definitions (continued)

Miscellaneous Control Register (0E)

7	6	5	4	3	2	1	0
EFEN	COMPD/A	SVIDD/A	FKREN	RATIO	TFLK	T512	CB100

Reg	Bit	Name	Function
0E	7	EFEN	Register 0E and 0F enable. When LOW, the functions of Register 0E and 0F are disabled. When HIGH, Registers 0E and 0F are active. When Registers 0E and 0F are enabled, Register 00 bit 3 is ignored. Register 0E bit 7 will read back whatever value was written.
0E	6	COMPD/A	COMPOSITE D/A disable. When HIGH, the COMPOSITE D/A converter is powered-down. When LOW, the D/A is enabled.
0E	5	SVIDD/A	LUMA/CHROMA D/A disable. When HIGH, the LUMA and CHROMA D/A converters are powered-down. When LOW, they are enabled.
0E	4	FKREN	Luminance processing enable. When FKREN is HIGH, the KEY input defines the function of CVBS input data. When the KEY input is HIGH, CVBS data is keyed over PD input data. When KEY is LOW, CVBS data is assumed to be luminance data delayed by one When FKREN is LOW, the KEY input operates normally, switching between CVBS and PD data.
0E	3	RATIO	Luminance ratio control bit. When LOW, 1/2 of current luminance and 1/2 of field delayed luminance from the CVBS input are added to yield a new combined luminance value. When RATIO is HIGH, 3/4 of current luminance is added to 1/4 of the delayed luminance to produce a new luminance value.
0E	2	TFLK	Luminance-pass threshold. The difference between current luminance and delayed luminance (from the CVBS inputs) is compared against a preset threshold set by TFLK. When TFLK is LOW, the high threshold must be exceeded to trigger the combining of current and delayed luminance (according to RATIO). If the higher threshold is not exceeded, current luminance is passed without modification. When TFLK is HIGH, a lower threshold is used to trigger the combining of current and delayed luminance.
0E	1	T512	EH/SL offset control bit. When LOW, the true value of EH and SL is offset by 256. When HIGH, the true value for EH and SL is offset by 512.
0E	0	CB100	NTSC/PAL color bars select. When HIGH, color bars with 100% white level are selected. When LOW, color bars will have 75% white level.

Control Register Definitions (continued)

Standards Control Register (0F)

7	6	5	4	3	2	1	0
EFEN	SIX25	PALID	SETUP	YGAIN		CGAIN	

Reg	Bit	Name	Function
0F	7	EFEN	Same as Register 0E bit 7, but read-only.
0F	6	SIX25	Select 625 lines per frame. When HIGH, the encoder assumes 625 line per frame. When LOW, 525 lines per frame are assumed.
0F	5	PALID	PAL select. When HIGH, Phase alternate line (PAL) operation is selected. When LOW, operation conforms to NTSC standards.
0F	4	SETUP	Setup enable. When HIGH, a 7.5 IRE Pedestal is added to the output video. when LOW, no pedestal is added.
0F	3-2	YGAIN	Luminance gain settings are adjusted to conform to the following NTSC and PAL standards: 0 0 NTSC without SETUP 0 1 NTSC-A and PAL-M 1 0 PAL-I and PAL-N 1 1 Reserved
0F	1-0	CGAIN	Chrominance gain settings are adjusted to conform to the following NTSC and PAL standards: 0 0 NTSC without SETUP 0 1 NTSC-A and PAL-M 1 0 PAL-I and PAL-N 1 1 Reserved

Timing Registers (10-17)

Reg	Bit	Name	Function
10	7-0	SY	Horizontal sync tip length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
11	7-0	BR	Breezeway length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
12	7-0	BU	Burst length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
13	7-0	CBP	Color back porch length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
14	7-0	XBP	Extended color back porch 8 LSBs. This 8-bit register holds the LSBs of a 10-bit value extending from 0 to 1023 PCK cycles. The two MSBs are located in control register 18.
15	7-0	VA	Active video 8 LSBs. This 8-bit register holds the LSBs of a 10-bit value extending from 0 to 1023 PCK cycles. The two MSBs are located in control register 18.
16	7-0	VC	Active video start 8 LSBs. This 8-bit register holds the LSBs of a 10-bit value which is the initial half active video length extending from 0 to 1023 PCK cycles. The two MSBs are located in control register 18.
17	7-0	VB	Active video end 8 LSBs This 8-bit register holds the LSBs of a 10-bit value which is the end half active video length extending from 0 to 1023 PCK cycles. The two MSBs are located in control register 18.

Control Register Definitions (continued)

Timing Register (18)

7	6	5	4	3	2	1	0
XBP		VA		VC		VB	

Reg	Bit	Name	Function
18	7-6	XBP	Extended color back porch 2 MSBs. These two bits hold the MSBs of a 10-bit value extending from 0 to 1023 PCK cycles. The LSBs are located in control register 14.
18	5-4	VA	Active video 2 MSB. These two bits hold the MSBs of a 10-bit value extending from 0 to 1023 PCK cycles. The LSBs are located in control register 15.
18	3-2	VC	Active video start 2 MSBs. These two bits hold the MSBs of a 10-bit value which is the initial half active video length extending from 0 to 1023 PCK cycles. The LSBs are located in control register 16.
18	1-0	VB	Active video end 2 MSBs. These two bits hold the MSBs of a 10-bit value which is the end half active video length extending from 0 to 1023 PCK cycles. The LSBs are located in control register 17.

Timing Registers (19-1E)

Reg	Bit	Name	Function
19	7-0	FP	Front porch length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
1A	7-0	EL	Equalization pulse LOW length. This 8-bit register holds a value from 0 to 255 PCK cycles.
1B	7-0	EH	Equalization pulse HIGH length. This 8-bit register holds a value extending from 0 to 255 PCK cycles. This value, when added to 256 (or 512), determines the final pulse length in the range of 256 to 511 (or 767) PCK cycles.
1C	7-0	SL	Vertical sync LOW length. This 8-bit register holds a value from 0 to 255 PCK cycles. This value, when added to 256 (or 512), determines the final pulse length in the range of 256 to 511 (or 767) PCK cycles.
1D	7-0	SH	Vertical sync HIGH length. This 8-bit register holds a value extending from 0 to 255 PCK cycles.
1E	7-0	CBL	Color bar length. This 8-bit register holds a value which is the length of each color bar displayed extending from 0 to 255 PCK cycles.

Timing Register (1F)

7	6	5	4	3	2	1	0
FIELD			LTYPE				

Reg	Bit	Name	Function
1F	7-5	FIELD	Field identification (read only). These three bits are updated 12 PXCK periods after each $\overline{\text{VHSYNC}}$. They allow the user to determine field type on a continuous basis.
1F	4-0	LTYPE	Line type identification (read only). These five bits are updates 5 PXCK periods after each $\overline{\text{VHSYNC}}$. They allow the user to determine line type on a continuous basis.

Control Register Definitions (continued)

Subcarrier Registers (20-27)

Reg	Bit	Name	Function
20	7-0	FREQL	Subcarrier frequency 4th byte (LSBs). This 8-bit register holds the LSB (bits 7-0) of the 32-bit subcarrier frequency value (non-genlock modes). The next eight most significant bits are held in Register 21.
21	7-0	FREQ3	Subcarrier frequency 3rd byte. This 8-bit register holds bits 15:8 of the subcarrier frequency value (non-genlock modes). The next eight most significant bits are held in Register 22.
22	7-0	FREQ2	Subcarrier frequency 2nd byte. This 8-bit register holds bits 23-16 of the subcarrier frequency value (non-genlock modes). The eight MSBs are held in Register 23.
23	7-0	FREQM	Subcarrier frequency 1st byte (MSBs). This 8-bit register holds the MSBs (bits 31-24) of the 32-bit subcarrier frequency value (non-genlock modes).
24	7-0	SYSPHL	Video phase offset LSBs. This 8-bit register holds the 8 LSBs of color subcarrier phase offset during active video.
25	7-0	SYSPHM	Video phase offset MSBs. This 8-bit register holds the 8 MSBs of color subcarrier phase offset during active video.
26	7-0	BURPHL	Burst phase offset LSBs. This 8-bit register holds the 8 LSBs of burst phase offset for color adjustment.
27	7-0	BURPHM	Burst phase offset MSBs. This 8-bit register holds the 8 MSBs of burst phase for color adjustment.

Test I/O Register (40)

Reg	Bit	Name	Function
40	7-0	TESTDAT	Test data input/output. This 8-bit register holds MSBs or LSBs, as determined by the Test Control Register. This control address does not auto-increment during read or write operations. To exit the test mode, reset the Control Register pointer by setting A_{1-0} and R/$\overline{W}$ LOW and then bring $\overline{CS}$ LOW.

Mask Register (50)

Reg	Bit	Name	Function
50	7-0	MASK	Mask register. This 8-bit register holds an 8-bit word that is logically ANDed with the incoming data presented to the three CLUTs in color-index mode. This register is a write-only register.

Y-Component Register (60)

Reg	Bit	Name	Function
60	7-0	Y	Y-component register. This register holds the contents of the luminance value before the Sync and Blank Insert circuitry of the encoder. Loading the Control Register pointer with 60_h brings 8-bit Y values out on the D_{7-0} port.

Color Lookup Table

The CLUT can be used in a variety of ways, depending on the data format and source presented to the PD port.

The CLUT is loaded like a RAMDAC, sequentially writing one byte to each of the three locations associated with the selected CLUT address. These three locations are referred to as Tables D, E, and F as shown in table 16 (not R,G, and B because they may or may not contain RGB information). and are loaded in that sequence. The address will increment automatically after the three values at one address are written or read.

Color-index Modes

In color-index (CI) mode, the CLUT is used to store the color look-up data, translating the 8-bit source pixel data into 24-bit RGB colors. Table D holds red data, Table E is green data, and Table F holds blue Data. The incoming data are presented to the three tables in parallel, and a 24-bit output is produced.

When the encoder is connected in parallel with a RAMDAC in a VGA system, the CLUT can be loaded simultaneously with the CLUT in the output RAMDAC. If a 6-bit RAMDAC is employed, 6 bits can be loaded via data pins D_{7-2} (MSB justified). The two LSBs should be set to 00 for optimal black level representation, but the largest error introduced by extraneous data in the LSBs is 3/4 LSB (at 6 bits). The encoder will produce the closest possible translation of the VGA colors in the encoded video environment.

GBR/RGB Modes

The nominal configuration for GBR/RGB modes is unity gain (CLUT data = CLUT address) for PAL and NTSC. Other transfer functions, such as gain adjustment, offset, and gamma correction, are easily loaded. The color data is loaded into the tables in G-B-R sequence in GBR mode, and R-G-B sequence in RGB mode.

Luminance/Color Difference Modes

The TMC22x91 expects Y, B-Y, and R-Y signals at the input to its modulator section. When presenting CCIR-601 YC_BC_R or digitized Y, B-Y, R-Y data to the CLUT, gain and offset factors are needed. Table 4 specifies the recommended transfer functions. The CLUT is loaded in $Y\text{-}C_B\text{-}C_R$ sequence.

Overlay Operation

For the TMC22091 and TMC22191 (when Format Control Register Bit 6 = LOW), the OL_{4-0} inputs are inactive. In CCIR-601 operation, the nominal data range for Y is from 16 to 235 and for C_B and C_R is from 16 to 240. This means that CLUT locations 0 to 15 and 241 to 255 are available for overlay colors. When the overlay locations are addressed (by forcing CLUT addresses outside the normal CCIR-601 data range), the addressed CLUT data is encoded resulting in the specific color found in that CLUT location. Overlay colors information stored in the unused CLUT locations must be Y, B-Y, R-Y values. Y, B-Y, and R-Y values are found from RGB values by:

$$\begin{aligned} Y &= 0.299\,R + 0.587\,G + 0.114\,B \\ B\text{-}Y &= -0.299\,R - 0.587\,G + 0.886\,B \\ R\text{-}Y &= 0.701\,R - 0.587\,G - 0.114\,B \end{aligned}$$

For the TMC22191, when the Format Control Register Bit 6 = HIGH, Overlay is controlled by the OL_{4-0} inputs which directly access CLUT locations, 01 thru 0F and F1 thru FF, as shown in Table 5. The values stored in these CLUT locations must be in RGB format.

Table 4. CLUT Transfer Functions for NTSC and PAL

Input Format (CLUT Address)			Output Format (CLUT Data)	
Component	Data Range	Transfer Equations	Component	Data Range
R	0 to 255	$R_O=R$	R_O	0 to 255
G	0 to 255	$G_O=G$	G_O	0 to 255
B	0 to 255	$B_O=B$	B_O	0 to 255
Y	16 to 235	$Y_O = Y * 1.1644 - 18.63$	Y_O	0 to 255
C_B	±112	$(B\text{-}Y)_O = C_B * 1.0126$	$(B\text{-}Y)_O$	±113
C_R	±112	$(R\text{-}Y)_O = C_R * 0.8011$	$(R\text{-}Y)_O$	±90
Y	0 to 255	$Y_O=Y$	Y_O	0 to 255
B-Y	±127	$(B\text{-}Y)_O = (B\text{-}Y) * 0.893$	$(B\text{-}Y)_O$	±113
R-Y	±127	$(R\text{-}Y)_O = (R\text{-}Y) * 0.7065$	$(R\text{-}Y)_O$	±90

Table 5. CLUT Locations Addressed by Overlay Inputs (TMC22191)

OL4-0	CLUT location
00	No Overlay
01	01
02	02
•	•
•	•
0E	0E
0F	0F
10	No Overlay
11	F1
12	F2
•	•
•	•

Table 5. CLUT Locations Addressed by Overlay Inputs (TMC22191) (continued)

OL4-0	CLUT location
1E	FE
1F	FF

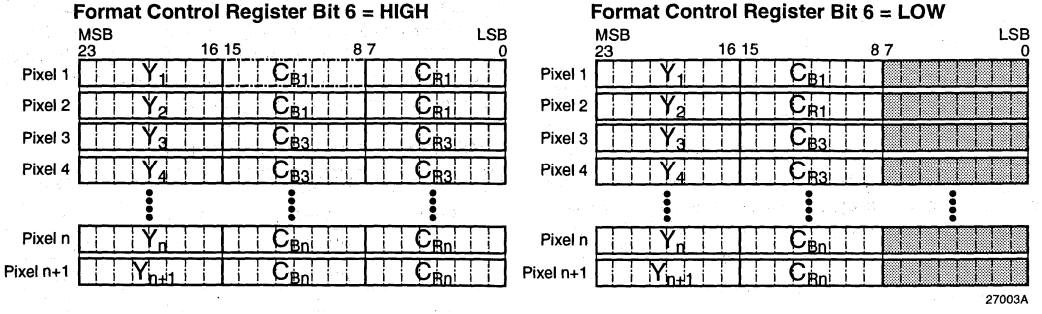
Color-space Conversion in the Matrix

When the input pixels are in RGB, GBR, or color-index format and the CLUT is bypassed (TMC22191), the Matrix remains enabled, converting RGB data to color-difference format. When the input pixels are in 444 format (YC_BC_R444, RGB, GBR, CI), the Interpolator (which converts 422 to 444) is not active. When the input pixels are in YC_BC_R format, the CLUT is enabled to scale the data to color-difference values and the Matrix is inactive. In color-index mode, the Matrix is active, converting the RGB CLUT output data to color-difference values.

BROADCAST VIDEO

Table 6. Pixel Input Operation for Format Control Register bit 6 = HIGH (TMC22191)

Format Control Register		Pixel Data Format	
FORMAT Bit 3,2	INMODE Bit 1,0	$\overline{BYPASS}$ = LOW CLUT bypassed	$\overline{BYPASS}$ = HIGH CLUT enabled
00 (RGB)	00 (444)	RGB	YC_BC_R444
00	01 (422)	RGB	YC_BC_R422
00	10 (15-bit)	RGB	RGB15
00	11 (CI)	RGB	CI
01	xx	reserved	reserved
10 (GBR)	00 (444)	GBR	YC_BC_R444
10	01 (422)	GBR	YC_BC_R422
10	10 (15-bit)	GBR	GBR15
10	11 (CI)	GBR	CI
11	xx	not allowed	not allowed



Note: The pixel input sequence begins on the first LDV pulse after PDC goes HIGH. n = Odd number

Figure 2. Pixel Data (PD_{23-0}) Sequence for YC_BC_R422

Gamma Correction

Gamma is built into broadcast television systems as a correction factor for nonlinearity in image acquisition (nonlinear conversion of light into current in a vidicon) and at the display (phosphor nonlinearity in converting current into light).

A Gamma corrector transfer function takes the form of

$$\text{Output} = k\,(\,\text{Input}\,)^{1/\gamma}$$

where a typical Gamma is 2.2 for NTSC, 2.8 for PAL.

Computer systems usually ignore Gamma in driving a display monitor. Each R, G, and B channel is treated as linear. When encoding a computer display output to video, the user must decide whether to apply a gamma correction factor and, if so, what value. It is a good assumption that, since the digital video input over the CVBS bus is in composite form, it has been Gamma corrected.

Gamma correction is applied in the RGB domain. When operating in YC_BC_R, for example when encoding a CCIR-601 signal, Gamma should have already been applied. Gamma correction is readily added to the RGB transfer equations shown in Table 4.

Video Timing

The TMC22x91 can be programmed to accommodate a wide range of system timing requirements. With a line locked pixel rate of 10 to 15 Mpps, the digitally synthesized horizontal waveforms and subcarrier frequency and phase are determined from 24 registers that are loaded by a controller.

Horizontal Programming

Horizontal interval timing is fully programmable, and is established by loading the timing registers with the durations of each horizontal element. The duration is expressed in PCK clock cycles. In this way, any pixel clock rate between 10 MHz and 15 MHz can be accommodated, and any desired standard or non-standard horizontal video timing may be produced. Figure 3 illustrates the horizontal blanking interval with timing register identification.

Horizontal timing parameters can be calculated as follows:

t = N x (PCK period)
= N x (2 x PXCK period)

where N is the value loaded into the appropriate timing register, and PCK is the pixel clock period.

Horizontal timing resolution is two PXCK periods. PXCK must be chosen such that it is an even integer multiple of the horizontal line frequency. This ensures that the horizontal line period, H, contains an integer number of pixels. The horizontal line comprises the sum of appropriate elements.

H = FP + SY + BR + BU + CBP + VA

When programming horizontal timing, subtract 5 PCK periods from the calculated values of CBP and add 5 PCK periods to the calculated value for VA.

Table 7. Horizontal Timing Specifications

Parameter	NTSC-M (µs)	PAL-I (µs)	PAL-M (µs)
FP	1.5	1.65	1.9
SY	4.7	4.7	4.95
BR	0.6	0.9	0.9
BU	2.5	2.25	2.25
CBP	1.6	2.55	1.8
VA	52.6556	51.95	51.692
H	63.5556	64.0	63.492

Vertical Programming

Vertical interval timing is also fully programmable, and is established by loading the timing registers with the durations of each vertical timing element, the duration expressed in PCK clock cycles. In this way as with horizontal programming, any pixel rate between 10 and 15 Mpps can be accommodated, and any desired standard or non-standard vertical video timing may be produced.

Like horizontal timing parameters, vertical timing parameters are calculated as follows:

t = N x (PCK period)
= N x (2 x PXCK period)

where N is the value loaded into the appropriate timing register, and PCK is the pixel clock period.

The Vertical Interval comprises several different line types based upon H, the Horizontal line time.

H = (2 x SL) + (2 x SH) [Vertical sync pulses]
= (2 x EL) + (2 x EH) [Equalization pulses]

The VB and VC lines are added to produce the half-lines needed in the vertical interval at the beginning and end of some fields. These must properly mate with components of the normal lines.

VB = CBP + VA - XBP = H/2 – CBPVC
= VA – (EL + EH) = VA – H/2

where Equalization HIGH and LOW pulses (EL + EH) = H/2 and the Extended Color Back Porch, XBP = VA + CBP – VB. XBP begins after the end of burst, BU, taking the place of CBP in vertical interval UBV lines. Figure 5 shows the vertical sync and equalization pulse detail

Table 8. Vertical Timing Specifications

Parameter (µs)	NTSC-M (µs)	PAL-I (µs)	PAL-M (µs)
H	63.5556	64	63.492
EH	29.4778	29.65	29.45
EL	2.3	2.35	2.3
SH	4.7	4.7	4.65
SL	27.1	27.3	27.1

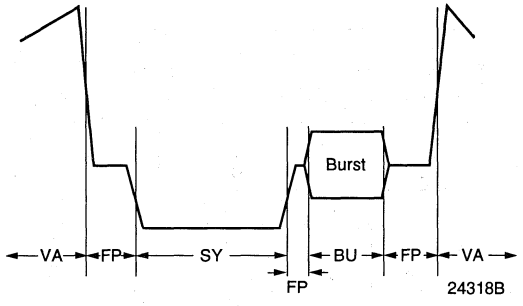


Figure 3. Horizontal Blanking Interval Timing

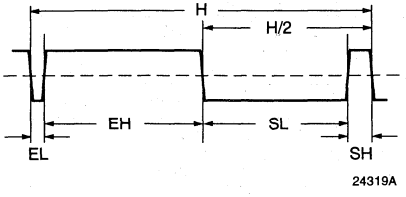


Figure 4. Sync and Equalization Pulse Detail Timing

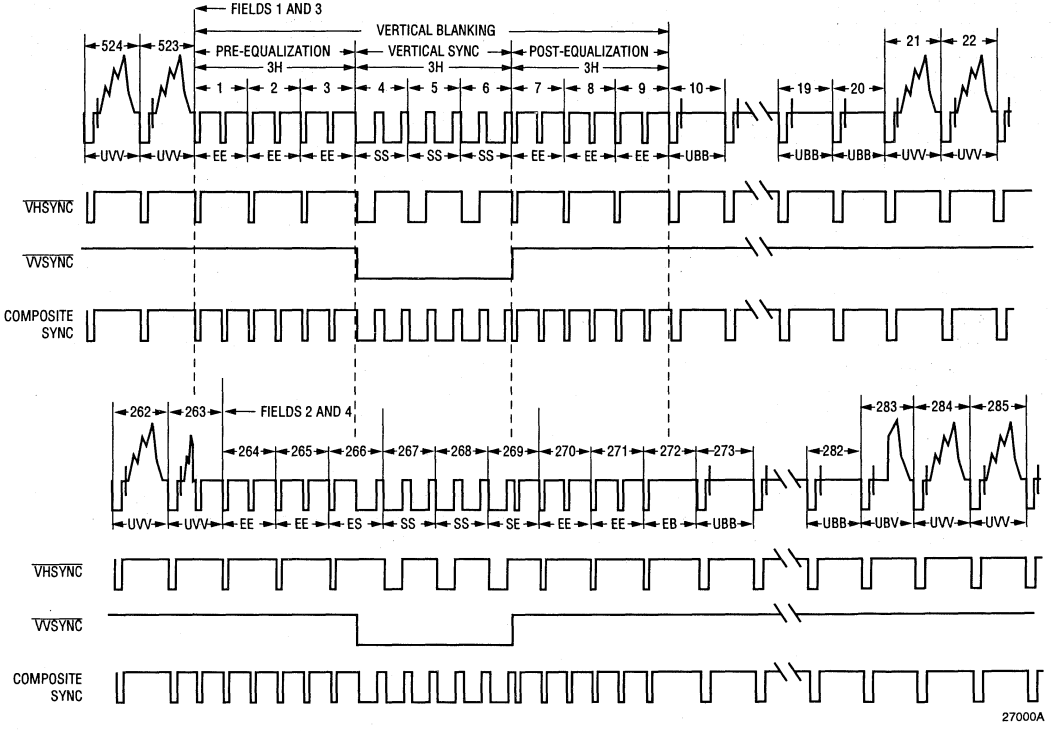


Figure 5. NTSC Vertical Interval

Table 9. NTSC Field/Line Sequence and Identification

Field 1 FIELD ID = x00			Field 2 FIELD ID = x01			Field 3 FIELD ID = x10			Field 4 FIELD ID = x11		
Line	ID	LTYPE	Line	ID	LTYPE	Line	ID	LTYPE	Line	ID	LTYPE
1	EE	00	264	EE	00	1	EE	00	264	EE	00
2	EE	00	265	EE	00	2	EE	00	265	EE	00
3	EE	00	266	ES	01	3	EE	00	266	ES	01
4	SS	03	267	SS	03	4	SS	03	267	SS	03
5	SS	03	268	SS	03	5	SS	03	268	SS	03
6	SS	03	269	SE	02	6	SS	03	269	SE	02
7	EE	00	270	EE	00	7	EE	00	270	EE	00
8	EE	00	271	EE	00	8	EE	00	271	EE	00
9	EE	00	272	EB	10	9	EE	00	272	EB	10
10	UBB	0D	273	UBB	0D	10	UBB	0D	273	UBB	0D
•••	•••	•••	•••	•••	•••	•••	•••	•••	•••	•••	•••
20	UBB	0D	282	UBB	0D	20	UBB	0D	282	UBB	0D
21	UVV	0F	283	UBV	0E	21	UVV	0F	283	UBV	0E
22	UVV	0F	284	UVV	0F	22	UVV	0F	284	UVV	0F
•••	•••	•••	•••	•••	•••	•••	•••	•••	•••	•••	•••
262	UVV	0F	524	UVV	0F.	262	UVV	0F	524	UVV	0F
263	UVE	0C	525	UVV	0F	263	UVE	0C	525	UVV	0F

EE Equalization pulse
SS Vertical sync pulse
EB Equalization broad pulse
UVV Active video
UBV Half-line black, half-line video
SE Half-line vertical sync pulse, half-line equalization pulse
ES Half-line equalization pulse, half-line vertical sync pulse
UBB Black burst
UVE Half-line video, half-line equalization pulse

Master and Genlock mode details of $\overline{\text{VHSYNC}}$, $\overline{\text{VVSYNC}}$, and composite $\overline{\text{VVSYNC}}$ (SOUT = HIGH) outputs are shown in Figures 5 and 6. When $\overline{\text{VHSYNC}}$ and $\overline{\text{VVSYNC}}$ are used as inputs (Slave mode), their falling edges mark the beginning of the sync interval and the width of the input pulse is specified under Operating Conditions.

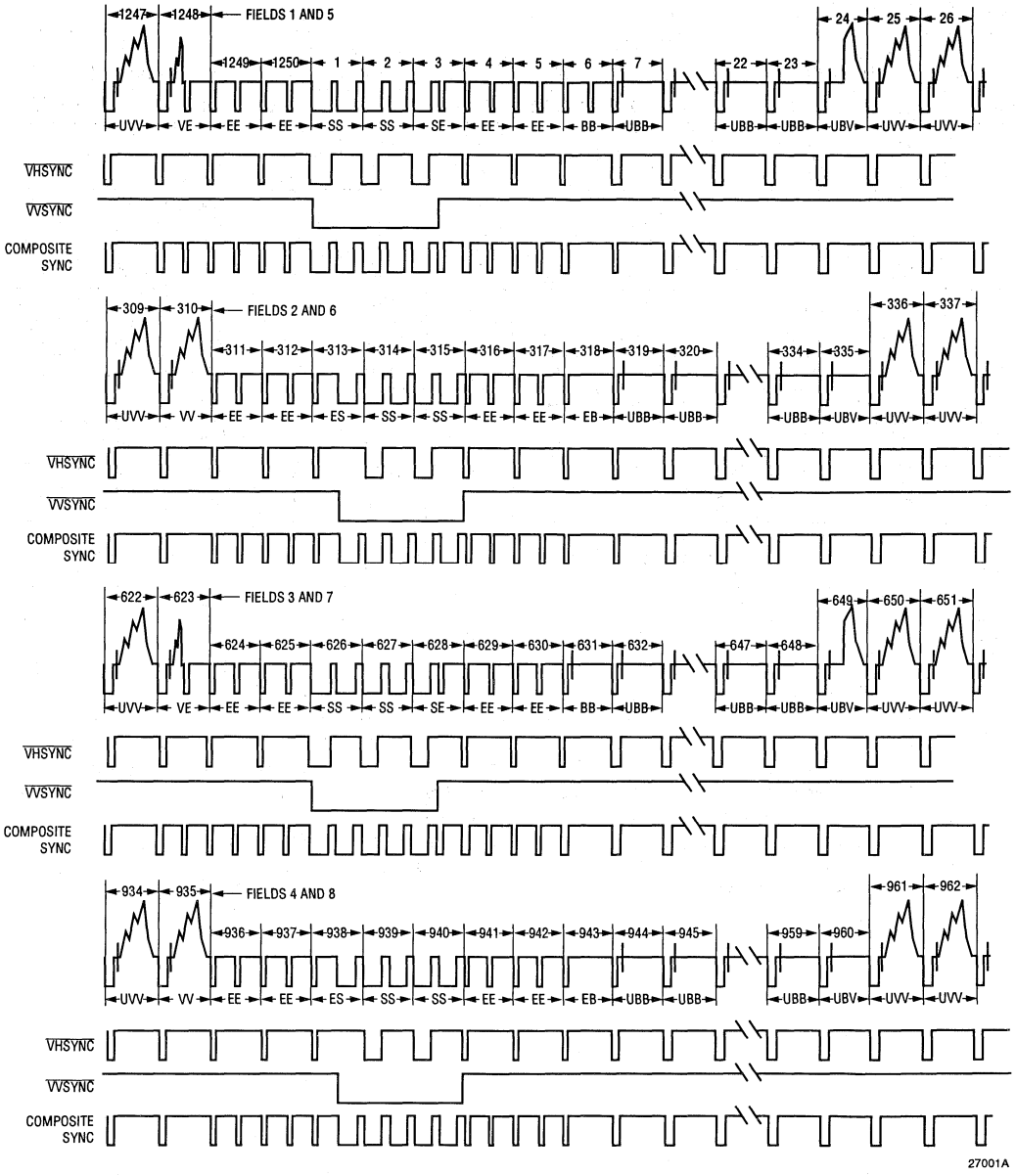


Figure 6. PAL Vertical Interval

Table 10. PAL Field/Line Sequence and Identification

Field 1 FIELD ID = 000, 100			Field 2 FIELD ID = 001, 101			Field 3 FIELD ID = 010, 110			Field 4 FIELD ID = 011, 111		
Line	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**	**Line**	**ID**	**LTYPE**
1	SS	03	313	ES	01	626	SS	03	938	ES	01
2	SS	03	314	SS	03	627	SS	03	939	SS	03
3	SE	02	315	SS	03	628	SE	02	940	SS	03
4	EE	00	316	EE	00	629	EE	00	941	EE	00
5	EE	00	317	EE	00	630	EE	00	942	EE	00
6	-BB	05	318	EB	10	631	UBB	0D	943	EB	10
7	UBB	0D	319	UBB	0D	632	UBB	0D	944	-BB	05
8	UBB	0D	320	UBB	0D	633	UBB	0D	945	UBB	0D
•••	•••	•••	•••	•••	•••	•••	•••	•••	•••	•••	•••
22	UBB	0D	335	UBB	0D	647	UBB	0D	960	UBB	0D
23	UBV	0E	336	UVV	0F	648	UBV	0E	961	UVV	0F.
24	UVV	0F	337	UVV	0F	649	UVV	0F	962	UVV	0F
•••	•••	•••	•••	•••	•••	•••	•••	•••	•••	•••	•••
308	UVV	0F	621	UVV	0F	933	UVV	0F	1246	UVV	0F
309	UVV	0F	622	-VV	07	934	UVV	0F	1247	UVV	0F
310	-VV	07	623	-VE	04	935	UVV	0F	1248	-VE	04
311	EE	00	624	EE	00	936	EE	00	1249	EE	00
312	EE	00	625	EE	00	937	EE	00	1250	EE	00

EE Equalization pulse
SS Vertical sync pulse
EB Equalization broad pulse
-BB Black burst with color burst suppressed
-VV Active video with color burst suppressed
-VE Half-line video, half-line equalization pulse, color burst suppressed.
SE Half-line vertical sync pulse, half-line equalization pulse
ES Half-line equalization pulse, half-line vertical sync pulse
UBB Black burst
UVV Active video
UVE Half-line video, half-line equalization pulse
UBV half-line black, half-line video

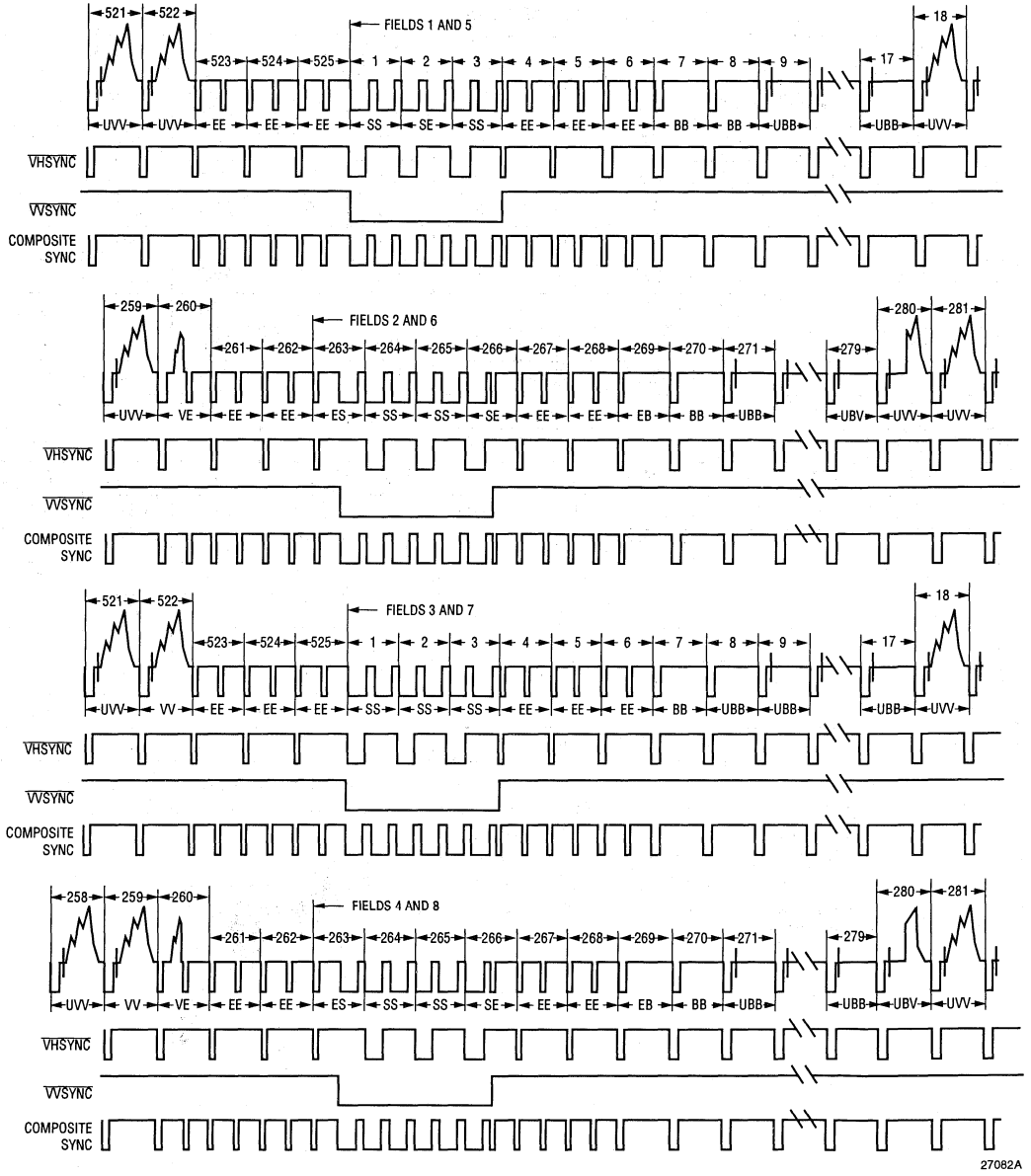


Figure 7. PAL-M Vertical Interval

Table 11. PAL-M Field/Line Sequence and Identification

Field 1 FIELD ID = 000, 100			Field 2 FIELD ID = 001, 111			Field 3 FIELD ID = 010, 110			Field 4 FIELD ID = 011, 111		
Line	ID	LTYPE	Line	ID	LTYPE	Line	ID	LTYPE	Line	ID	LTYPE
1	SS	03	263	ES	01	1	SS	03	263	ES	01
2	SS	03	264	SS	03	2	SS	03	264	SS	03
3	SS	03	265	SS	03	3	SS	03	265	SS	03
4	EE	00	266	SE	02	4	EE	00	266	SE	02
5	EE	00	267	EE	00	5	EE	00	267	EE	00
6	EE	00	268	EE	00	6	EE	00	268	EE	00
7	-BB	05	269	EB	10	7	-BB	05	269	EB	10
8	-BB	05	270	-BB	05	8	UBB	05	270	-BB	05
9	UBB	0D	271	UBB	1D	•••	•••	•••	271	UBB	1D
•••	•••	•••	•••	•••	•••	17	UBB	0D.	•••	•••	•••
17	UBB	0D	279	UBB	0D	18	UVV	0F	279	UBB	0D
18	UVV	0F	280	UBV	0E.	•••	•••	•••	280	UBV	0E.
...	...	...	281	UVV	0F	258	UVV	0F	281	UVV	0F
259	UVV	0F	•••	•••	•••	259	-VV	07	•••	•••	•••
260	-VE	04	521	UVV	0F	260	-VE	04	521	UVV	0F
261	EE	00	522	-VV	07	261	EE	00	522	UVV	0F
262	EE	00	523	EE	00.	262	EE	00	523	EE	00
			524	EE	00				524	EE	00
			525	EE	00				525	EE	00

EE Equalization pulse
SS Vertical sync pulse
EB Equalization broad pulse
-BB Black burst with color burst suppressed
-VV Active video with color burst suppressed
-VE Half-line video, half-line equalization pulse, color burst suppressed.
SE Half-line vertical sync pulse, half-line equalization pulse
ES Half-line equalization pulse, half-line vertical sync pulse
UBB Black burst
UVV Active video
UVE Half-line video, half-line equalization pulse
UBV half-line black, half-line video

Table 12. Standard Timing Parameters

Standard	Field Rate (Hz)	Horizontal Freq. (kHz)	Pixel Rate (Mpps)	PXCK Freq. (MHz)	Timing Register (hex)														
					SY 10	BR 11	BU 12	CBP 13	XBP 14	VA 15	VC 16	VB 17	Note 1 18	FP 19	EL 1A	EH[2] 1B	SL[2] 1C	SH 1D	CBL 1E
NTSC sqr. pixel	59.94	15.734266	12.27	24.54	3A	07	1F	0F	23	8B	05	77	65	12	1C	6A	4C	3A	52
NTSC CCIR-601	59.94	15.734266	13.50	27.00	40	08	22	11	40	CB	1E	90	65	14	1F	8E	6D	3F	59
NTSC 4x FSC	59.94	15.734266	14.32	28.64	43	09	24	12	54	F7	30	B5	65	15	21	A6	84	43	5F
PAL sqr. pixel	50.00	15.625000	14.75	29.50	45	0D	21	21	6D	03	2B	B7	75	19	23	B5	93	45	61
PAL CCIR-601	50.00	15.625000	13.50	27.00	40	0C	1E	1D	4D	C3	13	93	65	16	20	90	71	3F	58
PAL 15 Mpps	50.00	15.625000	15.00	30.00	46	0D	22	21	73	11	31	BF	75	19	23	BD	9A	47	62
PAL-M sqr.pixel	60.00	15.750000	12.50	25.01	3E	0B	1C	13	26	86	FE	8B	61	18	1D	70	53	3A	52
PAL-M CCIR-601	60.00	15,750000	13.50	27.00	44	0C	1E	13	26	Bf	12	99	65	1A	1F	8E	6E	3F	57
PAL-M 4x FSC	60.00	15,750000	14.30	28.60	47	0D	20	15	4C	E8	22	AC	65	1B	21	A5	84	42	5D

Notes:

1. XBP, VA, VC, and VB are 10-bit values. The 2 MSBs for these four variables are in Timing Register 18. See Table 3.
2. EH and SL are 9-bit values. A most significant "1" is forced by the TMC22x91 since EH and SL must range from 256 to 511. EH and SL may be extended to 767. Only the eight LSBs are stored in Timing Registers 1B and 1C.
3. Every calculated timing parameter has a minimum value of 5 except EH and SL which have minimum values of 256.

VITS Insertion

In both NTSC and PAL, the TMC22x91 can be set up to allow Vertical Interval Test Signals (VITS) in the vertical interval in place of normal black burst lines (UBB). This is controlled by Interface Control Register bit 7. If this bit is LOW, UBB lines are black burst and are independent of TMC22x91 input data. If the bit is HIGH, all vertical interval UBB lines become UVV. UVV lines are active video and depend upon data input to the TMC22x91. VITS lines may carry special test signals or pass captioning data through the encoder.

Edge Control

SMPTE 170M NTSC and Report 624 PAL video standards call for specific rise and fall times on critical portions of the video waveform. The TMC22x91 does this automatically. The TMC22x91 digitally defines slopes compatible with SMPTE 170M NTSC or CCIR Report 624 PAL on:

1. H and V Sync leading and trailing edges.
2. Burst envelope.
3. Active video leading and trailing edges.

Subcarrier Programming

The color subcarrier is produced by an internal 32-bit digital frequency synthesizer which is completely programmable in frequency and phase. Separate registers are provided for phase adjustment of the color burst and of the active video, permitting external delay compensation and color adjustment.

In Master or Slave mode, the subcarrier is internally synchronized to establish and maintain a specified relationship between the falling edge of horizontal sync and color burst phase (SCH). In NTSC and PAL, SCH synchronization is performed every eight fields, on field 1 of the eight-field sequence. Proper subcarrier phase is maintained through the entire eight fields, including the 25 Hz offset in PAL systems. See the description of 8FSUBR under Test Control Register bit 1 for the subcarrier reset function.

In Genlock mode, the phase and relative frequency of the incoming video are transmitted by the TMC22071 Genlocking Video Digitizer over the CVBS bus at the beginning of each line, which synchronize the digital subcarrier synthesizer. When key control register bit BUKEN is HIGH and digitized burst from the TMC22071 is passed through to the reconstruction D/A converter, the reference subcarrier for the chrominance modulator is still synthesized within the encoder.

NTSC Subcarrier

For NTSC encoding, the subcarrier synthesizer frequency has a simple relationship to the pixel clock period, repeating over 2 lines: The decimal value is:

$$FREQ = \frac{(455/2)}{(\text{pixels/line})} \times 2^{32}$$

This value must be converted to binary and split into four 8-bit registers, FREQM, FREQ2, FREQ3, and FREQL. The number of pixels/line is:

Pixels/line = (2/PXCK frequency) (H period)

SYSPH establishes the appropriate phase relationship between the internal synthesizer and the chroma modulator. The nominal value for SYSPH is zero.

Other values for SYSPH must be converted to binary and split into two 8-bit registers, SYSPHM and SYSPHL.

Burst Phase (BURPH) sets up the correct relative NTSC modulation angle. The value for BURPH is:

BURPH = SYSPH + 8,192

This value must be converted to binary and split into two 8-bit registers, BURPHM and BURPHL. The decimal number 8,192 advances the burst phase by 45°.

PAL Subcarrier

The PAL relationship is more complex, repeating only once in 8 fields (the well-known 25 Hz offset):

$$FREQ = \frac{(1135/4) + (1/625)}{(\text{pixels/line})} \times 2^{32}$$

This value must be converted to binary and split as described previously for NTSC.

For PAL, the decimal value for SYSPH is found from:

$$SYSPH = \frac{FREQ}{2^{17}} = BURPH$$

This value must be converted to binary and split into two 8-bit registers, SYSPHM and SYSPHL. Burst Phase in PAL is identical to SYSPH. Therefore, the same values for SYSPHM and SYSPHL must be used for BURPHM and BURPHL.

PAL-M Subcarrier

$$FREQ = \frac{(909/4)}{(\text{pixels/line})} \times 2^{32}$$

$$SYSPH = \frac{FREQ}{2^{17}} = BURPH$$

Table 13. Standard Subcarrier Parameters

Standard	Field Rate (Hz)	Horizontal Freq. (kHz)	Pixel Rate (MHz)	PXCK Freq. (MHz)	Sub-carrier Freq. (MHz)	Subcarrier Register (hex)							
						BURPHM 27	BURPHL 26	SYSPHM 25	SYSPHL 24	FREQM 23	FREQ2 22	FREQ3 21	FREQL 20
NTSC sqr. pixel	59.94	15.734266	12.27	24.54	3.57954500	20	00	00	00	4A	AA	AA	AB
NTSC CCIR-601	59.94	15.734266	13.50	27.00	3.57954500	20	00	00	00	43	E0	F8	3E
NTSC 4x fSC	59.94	15.734266	14.32	28.64	3.57954500	20	00	00	00	40	00	00	00
PAL sq. pixel	50.00	15.625000	14.75	29.50	4.43361875	00	00	00	00	4C	F3	18	19
PAL CCIR-601	50.00	15.625000	13.50	27.00	4.43361875	00	00	00	00	54	13	15	96
PAL 15 Mpps	50.00	15.625000	15.00	30.00	4.43361875	00	00	00	00	4B	AA	C6	A1
PAL-M sq. pixel	60	15.750	12.50	25.01	3.57561149	00	00	00	00	49	45	00	51
PAL-M CCIR-601	60	15,750	13.50	27.00	3.57561149	00	00	00	00	43	DF	3F	D7
PAL-M 4x fSC	60	15,750	14.30	28.60	3.57561149	00	00	00	00	40	10	66	F5

SCH Phase Error Correction

SCH refers to the timing relationship between the 50% point of the leading edge of horizontal sync and the positive or negative zero-crossing of the color burst subcarrier reference. SCH error is usually expressed in degrees of subcarrier phase. In PAL, SCH is defined for line 1 of field 1, but since there is no color burst on line 1, SCH is usually measured at line 7 of field 1. The need to specify SCH relative to a particular line in PAL is due to the 25 Hz offset of PAL subcarrier frequency. Since NTSC has no such 25 Hz offset, SCH applies to all lines.

The SCH relationship is only important in the TMC22x91 when two video sources are being combined or if the composite video output is externally combined with another video source. In these cases, improper SCH phasing will result in a noticeable horizontal jump of one image with respect to another and/or a change in hue proportional to the SCH error between the two sources.

SCH phasing can be adjusted by modifying BURPH and SYSPH values by equal amounts. SCH is advanced/delayed by one degree by increasing/decreasing the value of BURPH and SYSPH by approximately $B6_h$. An SCH error of 15° is corrected with SYSPH and BURPH offsets of AAA_h.

Video Test Signals

The TMC22x91 has two standard video test waveforms for evaluating video signal integrity. They are selected and controlled by the Format Control Register.

Setting the Format Control Register bits 0, 4, and 5 LOW generates standard color bars at the COMPOSITE output (Figure 11), the luminance component stair-step signal at the LUMA output, and the chrominance component on the CHROMA output. The six colors are 100% saturated PAL and 75% saturated for NTSC.

The percentage color saturation is selectable via Misc. Control Register 0E, bit 0.

The color bar test pattern comprises eight equal-width bars during VA, the active video period. The Timing Register value for CBL is found from:

$$CBL = \frac{VA + 7}{8}$$

If CBL is larger than this, the color bars are truncated at the end of VA. If CBL is smaller than VA/8, the color bar sequence will repeat, starting with another white bar. From left to right color bars 1 to 8 should be white, yellow, cyan, green, magenta, red, blue, and black.

The modulated ramp waveform is enabled by setting the Format Control Register to 30_h. It comprises constant-amplitude and constant-phase subcarrier modulation superimposed on a linear ramp which slews from black to white during the active video portion of each horizontal line (Figure 12). This waveform is useful in making differential gain and differential phase measurements. Differential gain is a measure of the variation in saturation of a color as the luminance component is varied from black to white. Differential phase is a measure of the variation in hue of a color as the luminance component is varied from black to white.

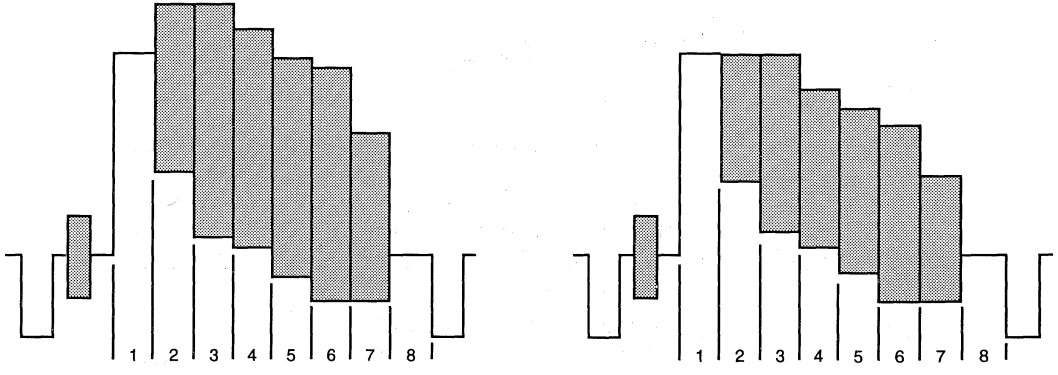


Figure 8. 100% Color Bars With 100% and 75% Chrominance Saturation

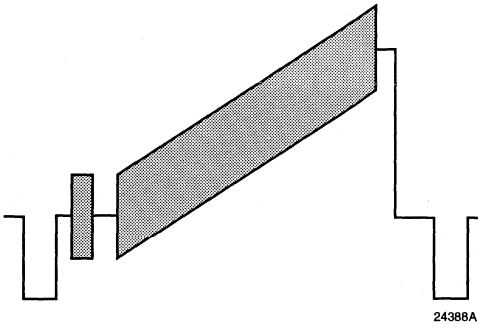


Figure 7. Modulated Ramp Waveform

Microprocessor Interface

The microprocessor interface comprises 13-lines. Two address bits provide four addresses for device programming and CLUT/register management. Address bit 0 selects between control registers and CLUT memory. Address bit 1 selects between reading/writing the register addresses and reading/writing register or CLUT data.

When writing, the address is presented along with a LOW on the R/$\overline{W}$ pin during the falling edge of $\overline{CS}$. Eight bits of data are presented on D_{7-0} during the subsequent rising edge of $\overline{CS}$.

One additional falling edge of $\overline{CS}$ is needed to move input data to the assigned working registers.

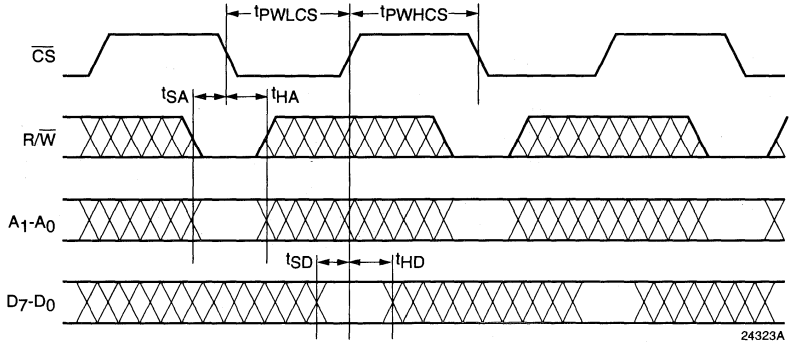


Figure 10. Microprocessor Port – Write Timing

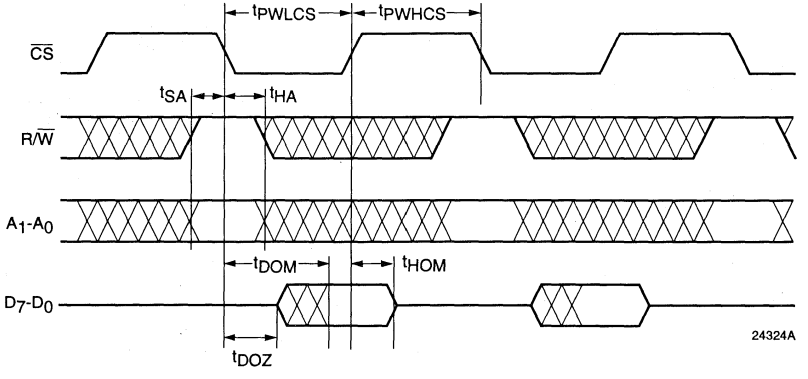


Figure 11. Microprocessor Port – Read Timing

In read mode, the address is accompanied by a HIGH on the R/$\overline{W}$ pin during a falling edge of $\overline{CS}$. The data output pins go to a low-impedance state t_{DOZ} ns after $\overline{CS}$ falls. Valid data is present on D_{7-0} t_{DOM} after the falling edge of $\overline{CS}$. Because this port operates asynchronously with the pixel timing, there is an uncertainty in this data valid output delay of one PXCK period. This uncertainty does not apply to t_{DOZ}.

The $\overline{RESET}$ pin restores the TMC22x91 to field 1 line 1 and places the encoder in a power-down state (if $\overline{HRESET}$ is LOW). Bit 4 of the Global Control Register ($\overline{SRESET}$) is set LOW. All other control words and CLUT contents are left unchanged. Returning $\overline{RESET}$ HIGH synchronizes the internal clock with PXCK and restores the device outputs to active states.

Reading Pixel Data from the D_{7-0} Port

The microprocessor port of the TMC22x91 may be used to monitor digital video outputs. The eight MSBs of the upsampled and interpolated pixel data that go to the COMPOSITE D/A converter can also be accessed via the D_{7-0} port. When the Test Control Register is loaded with 28_h and the Control Register pointer is loaded with 40_h, the D_{7-0} port will output the 8-bit composite pixels synchronous with PXCK. To halt the pixel flow from D_{7-0}, simply bring $\overline{CS}$ HIGH.

Luminance pixel data may also be read from D_{7-0}. In this case, the eight MSBs of luminance at the input of the Sync and Blank Insert block are monitored. When the Control Register pointer is loaded with 60_h, the D_{7-0} port will output 8-bit luminance pixels synchronous with respect to PXCK. To halt the pixel flow from D_{7-0}, bring $\overline{CS}$ HIGH.

Operational Timing

The TMC22x91 operates in three distinct modes:

1. Master mode. The encoder independently produces all internal timing and provides digital sync to the host controller.
2. Slave mode. The encoder accepts horizontal and vertical sync from the controller and synchronizes the video output accordingly.
3. Genlock mode. The encoder accepts horizontal and vertical sync from the companion TMC22071 Genlocking Video Digitizer, synchronizes itself to the incoming video, and provides appropriate H Sync and V Sync to the host. It synchronizes Pixel Data input in two ways:
   a. Internal PDC. The encoder internally generates the Pixel Data Control (PDC) signal which calls for data input from the external pixel source.
   b. External PDC. The encoder receives a PDC signal from the host and accepts Pixel Data based on that input.

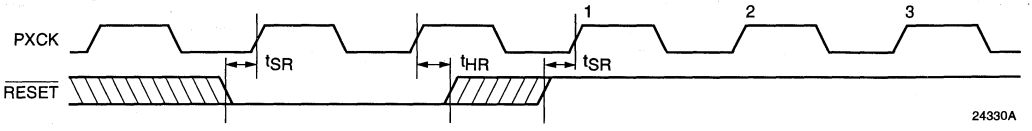


Figure 12. Reset Timing – PCK Synchronization

Reset Timing

The TMC22x91 operates from a master clock (PXCK) at twice the pixel rate. In Master mode, the PCK to PXCK timing relationship is set on the rising edge of $\overline{RESET}$. In Figure 12, PCK is denoted by odd PXCK counts.

When $\overline{RESET}$ is taken LOW with sufficient setup time (t_{SR}) before a rising edge of PXCK, the internal state machines are reset and the device is put into a mode as dictated by the Global Control Register bits 0 and 4. In Master mode, when the $\overline{RESET}$ pin is taken HIGH, the internal clock timing is established. In Slave and Genlock mode, this timing is established by $\overline{VHSYNC}$ and $\overline{GHSYNC}$ respectively. The first PXCK following this $\overline{RESET}$ rising edge is designated as PXCK 1. Where it is significant, reference PXCK timing will be shown with numbered rising edges. A designation of 2N clocks refers to an even number of PXCK rising edges from device reset. If $\overline{RESET}$ is not shown and clock numbering does not refer to 2N, timing is relative to signals shown in the diagram only.

Pixel Data Input Timing

PXCK is internally divided by 2 to generate an internal pixel clock, PCK which is not accessible from the pins of the TMC22x91. To ensure the correct phase relationship between PCK and pixel data, PCK is locked to $\overline{VHSYNC}$ or $\overline{GHSYNC}$ (Slave or Genlock mode, respectively). In Master mode, $\overline{VHSYNC}$ is produced on the rising edge of PCK allowing external circuitry to synchronize the generation of pixel data and LDV which also operates at the rate of PCK.

The rising edge of LDV clocks the 24-bit pixel data into three 8-bit registers while PCK clocks that data through the pixel data path within the TMC22x91. It is therefore necessary to meet the set-up and hold timing between pixel data and LDV as well as LDV and PCK as shown in Figure 13.

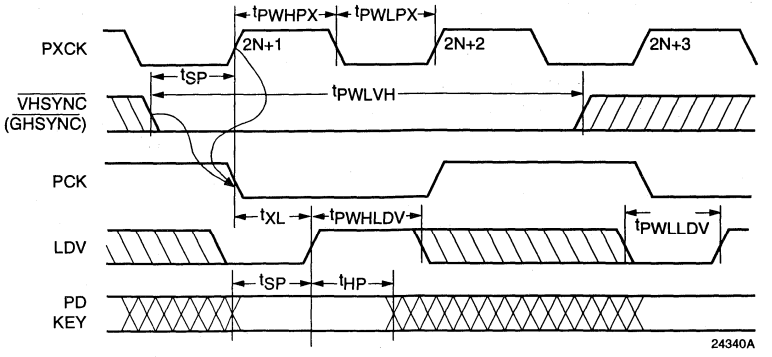


Figure 13. Slave Mode PD Port Interface Timing (Genlock Mode)

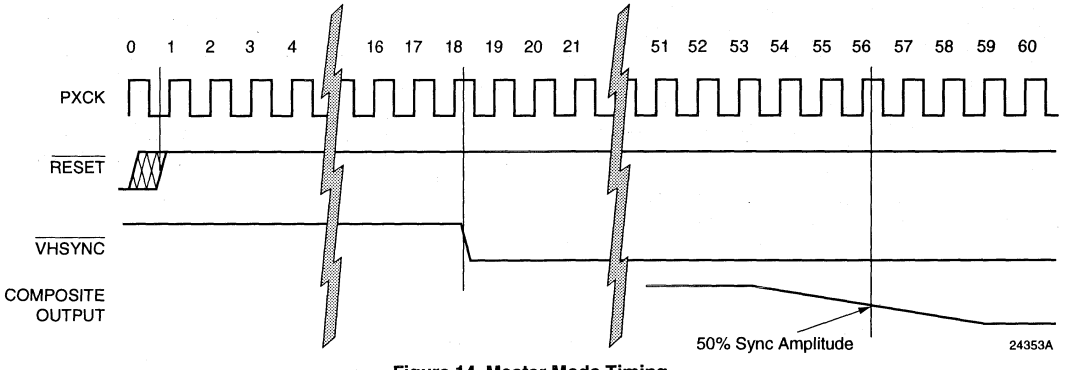


Figure 14. Master Mode Timing

Master Mode

In Master mode, initial timing is determined from the RESET input, and subsequent cycles result from programmed values in the Timing Control Registers. The Horizontal Sync output, VHSYNC, goes LOW 18 PXCK clock cycles after the device is reset. The 50% point of the falling edge of sync LOW on line 4 of field 1 (NTSC) or line 1 of field 1 (PAL) occurs at the COMPOSITE and LUMA outputs 56 clocks after reset, or 38 clocks after VHSYNC. See Figure 14, Master Mode Timing.

Slave Mode

In Slave mode, the 50% point of the falling edge of sync occurs 46 PXCK clocks after the falling edge of VHSYNC, which is an input signal to the TMC22x91. This must be provided by the host to begin every line. If it is early, the line will be started early, maintaining the 52 clock delay to output. If it comes late, the front porch portion of the output waveform will be extended as necessary. See Figure 15, Slave Mode Timing.

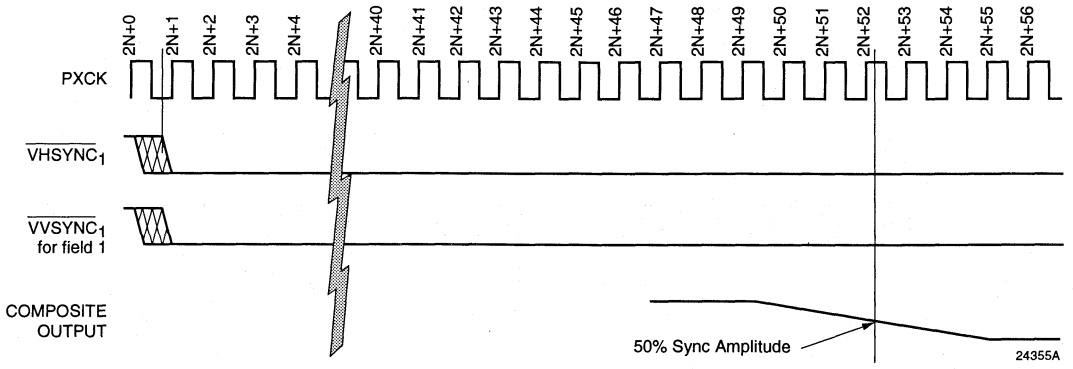


Figure 15. Slave Mode Timing

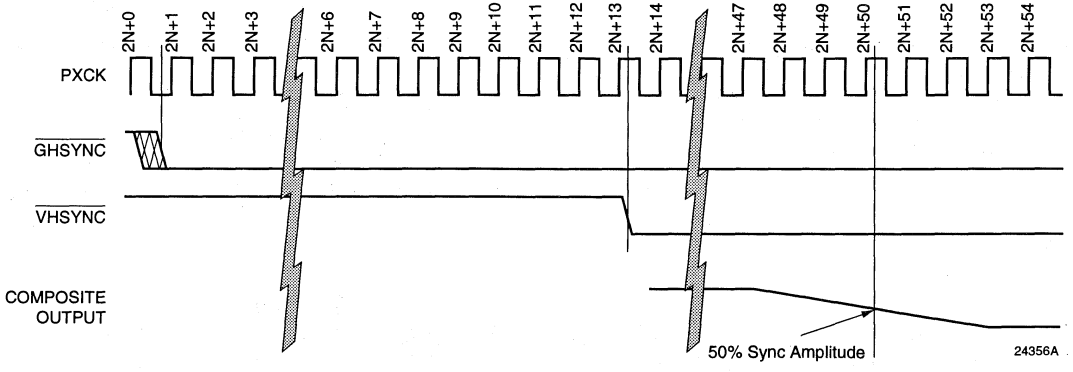


Figure 16. Genlocked Mode Timing

Genlocked Mode

In Genlocked mode, the encoder receives sync signals over the $\overline{\text{GHSYNC}}$ and $\overline{\text{GVSYNC}}$ inputs, and provides $\overline{\text{VHSYNC}}$ and $\overline{\text{VVSYNC}}$ to the host. The 50% sync amplitude point occurs 50 PXCK clocks after $\overline{\text{GHSYNC}}$ goes LOW, while $\overline{\text{VHSYNC}}$ is produced at clock 13. If $\overline{\text{GHSYNC}}$ is late, the front porch is lengthened, if is is early, front porch is shortened. See Figure 16, Genlock Mode Timing.

Pixel Data Control

The Pixel Data Control (PDC) signal determines the active picture area. It may be an input or an output, as determined by the Interface Control Register bit 1.

The position (number of PCK cycles) of the rising edge of PDC relative to the falling edge of $\overline{\text{VHSYNC}}$ can be found by summing SY, BU, BR, and CBP. See Figure 17.

External Pixel Data Control

When used as an input, PDC goes HIGH four PXCK cycles before the first valid pixel of a line is presented to the PD input port. If this signal is late (with respect to the horizontal blanking interval programmed in the timing control registers), the Color Back Porch (CBP) will be extended. If it is early, incoming pixel data will be ignored until the end of the CBP.

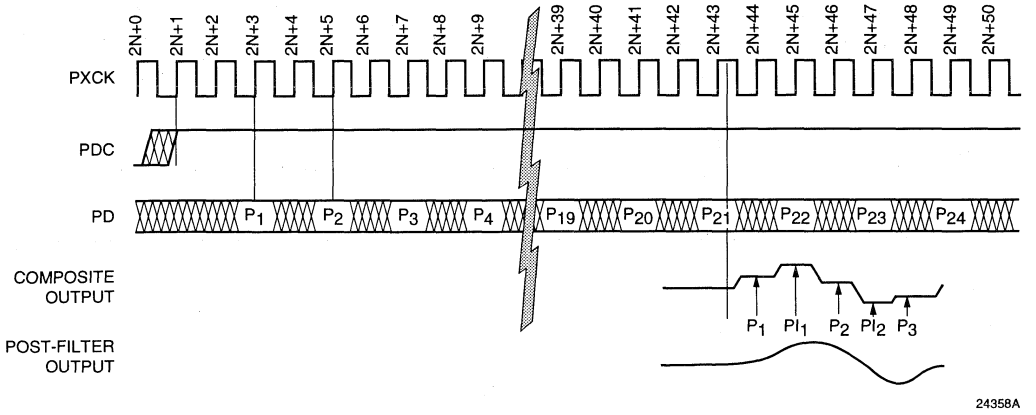


Figure 17. External Pixel Data Control

Internal Pixel Data Control

When programmed as an output, PDC goes HIGH four PXCK periods prior to the end of CBP (as programmed in the horizontal timing registers) which is also four PXCK cycles prior to required input of the first pixel of a line.

Pixels produced by the encoder appear at the analog outputs (COMPOSITE, LUMA, CHROMA) 40 clocks after they are registered into the PD port. Note that the pixels enter at one-half the PXCK rate. The encoded signal passes through interpolation filters which generate intermediate output values, improving the output frequency response and greatly simplifying the external reconstruction filter. The interpolated pixels are designated PI in the diagram.

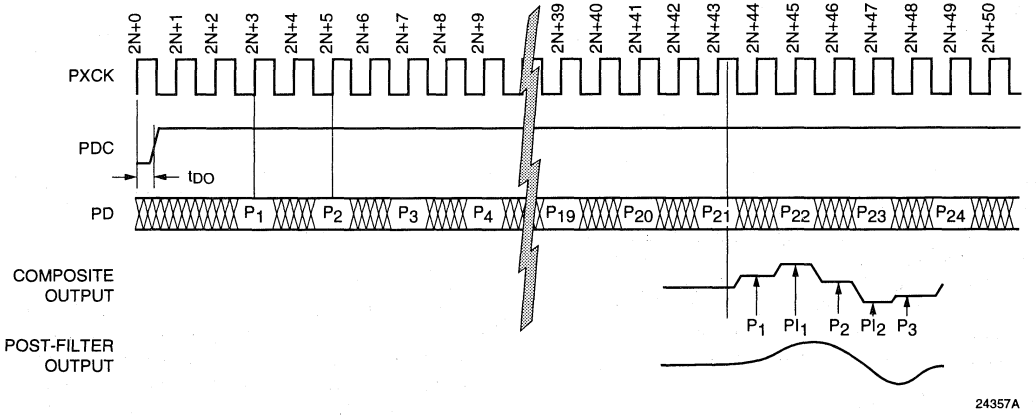


Figure 18. Internal Pixel Data Control

Layering with the TMC22191

Layering is a video production process where various images or patterns are superimposed (keyed) over each other to form a layered composite of the input images. Four layers with the following priority are provided by the TMC22191:

1. The DOWNSTREAM KEY layer keys over all other layers.
2. The FOREGROUND layer keys over MIDGROUND and BACKGROUND, but not over DOWNSTREAM KEY.
3. The MIDGROUND layer keys over BACKGROUND, but not over FOREGROUND or DOWNSTREAM KEY.
4. The BACKGROUND layer never keys over any other layer.

It is important not to confuse layers with sources. The TMC22191 can be programmed to assign any of its input sources (RGB, YC_RC_B, CVBS bus, Overlay bits) to any of the four layers.

The ability to combine various video sources into a 4-layer composite image is a very powerful tool in the production of live video. The TMC22191 performs layering operations entirely in the digital domain, enabling precise digital control.

A 4-Layer Example

For this layering example, a BACKGROUND image is generated. This image comprises shaded matte levels varying from black at the top of the screen to white at the bottom. This could just as well be a color image which will be seen wherever no other image appears through the layering process.

The MIDGROUND image comprises a happy face superimposed over a white rectangle. Only the happy face and the white rectangle are of interest for this image and therefore, the portion of the image outside that area will be replaced by the BACKGROUND image when MIDGROUND is keyed over BACKGROUND. A key signal is generated on a pixel-by-pixel basis. It indicates which image is active. The key signal for keying MIDGROUND over BACKGROUND is shown to the right of the MIDGROUND image. This represents a single bit signal mapped over the image. When the signal is black (logic LOW), the MIDGROUND image is active, when it is white (logic HIGH), the BACKGROUND is active.

The results of layering MIDGROUND over BACKGROUND images are shown in the 2-layer composite image Figure 19.

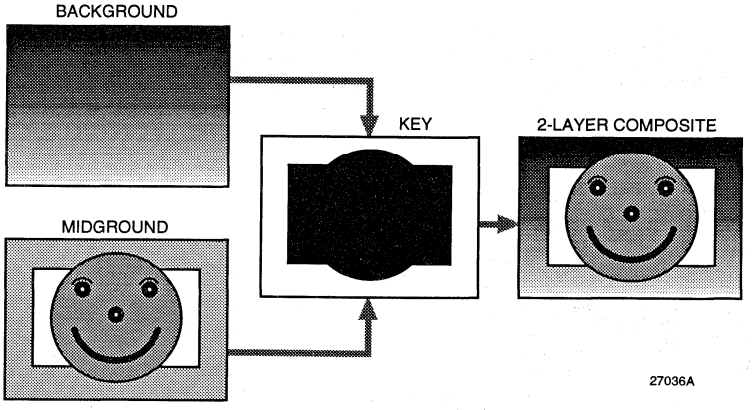


Figure 19. 2-Layer Image Construction

A FOREGROUND image comprises a shaded matte rectangle with "HI KIDS !" alpha characters in its center. This is to be superimposed over the previous 2-layer composite image. The key signal needed for superimposing FOREGROUND over other images is shown to the right of the FOREGROUND image. This represents a single bit signal mapped over the image. When the signal is black (logic LOW), the FOREGROUND image is active, when it is white (logic HIGH), the composite image is active.

A new 3-layer composite image, FOREGROUND over MIDGROUND over BACKGROUND, is shown in Figure 20.

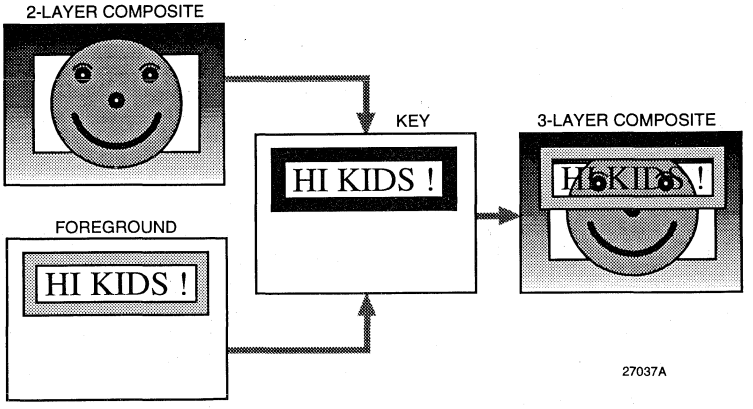


Figure 20. Adding a 3rd Layer

A DOWNSTREAM KEY image comprises the white alpha characters "HAPPY FACE", and black alpha characters "Time". This is to be superimposed over the previous 3-layer composite image. The key signal needed for superimposing DOWNSTREAM KEY image over the other composite images is shown to the right. This represents a single bit signal mapped over the image. When the signal is black (logic LOW), the DOWNSTREAM KEY image is active, when it is white (logic HIGH), the previous composite image is active.

The final 4-layer composite image, DOWNSTREAM KEY over FOREGROUND over MIDGROUND over BACKGROUND, is shown in Figure 21.

In this illustration, all four source images are static (not moving). The images input to the TMC22191 can just as well be "live" (from video camera or VCR sources) as long as:

1. Data from those sources is in an input format that the TMC22191 can accept, and
2. The sources either synchronize the TMC22191 (Genlock mode) or are synchronized by the TMC22191 (Master or Slave mode).

Key signals may be generated external to the TMC22191 (Hardware Keying) and use the KEY input pin for control. Key signals may also be generated within the TMC22191 (Data Keying) by the comparison of input color data with color data stored in the TMC22191.

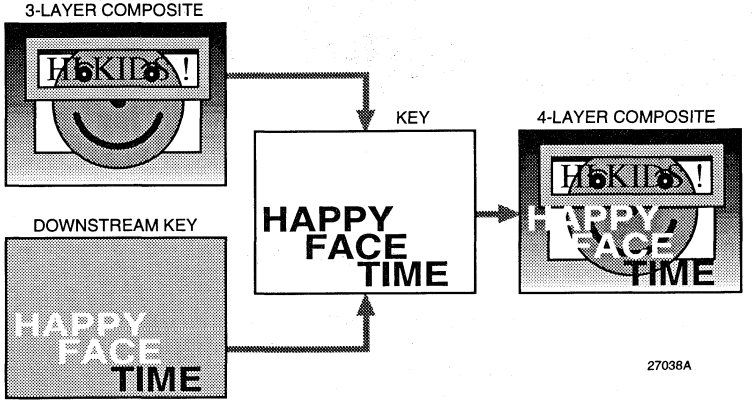


Figure 21. Adding a 4th Layer

2-Layer Keying with the TMC22091

The TMC22091 facilitates the keying of PD port input data over the CVBS bus input data. Keying is controlled on a pixel-by-pixel basis by either the KEY input pin or the internal Data Key. The first two layers in the previous 4-Layer Example apply to the TMC22091. The result of keying is an effect where a MIDGROUND source image (i.e. Happy Face from PD data) is superimposed over a BACKGROUND source image (i.e. variable matte color from CVBS data).

Assigning Video Sources to Layers with the TMC22191

Digital video inputs to the TMC22191 (PD, CVBS, Overlay) are assigned to the four layers by choosing one of the 16 modes of the Layering Control Register. OVERLAY is always keyed (switched on a pixel-by-pixel basis from active to transparent) by the OL_{4-0} inputs. OVERLAY can not be programmed to the BACKGROUND layer. The CVBS digital video bus can be assigned to any of the four layers and is keyed by the KEY input signal or internal Data Key. In modes 0 thru 7, the CLUTs are not bypassed and the $\overline{BYPASS}$ input is ignored.

Table 14. Layer Assignments, Image Sources, and Keying Controls (TMC22191)

LCR 04	Background	Midground		Foreground		Downstream Key	
LAYMODE	Image Source	Image Source	Keying Control	Image Source:	Keying Control	Image Source:	Keying Control
0	PD(YC_BC_R, RGB, CI)	CVBS	KEY or Data Key	—	—	—	—
1	PD(YC_BC_R, RGB, CI)	CVBS	KEY or Data Key	OVERLAY	OL_{4-0}	—	—
2	PD(YC_BC_R, RGB, CI)	CVBS	KEY	PD(YC_BC_R, RGB, CI)	$\overline{\text{Data Key}}$	OVERLAY	OL_{4-0}
3	PD(YC_BC_R, RGB, CI)	CVBS	KEY	PD(YC_BC_R, RGB, CI)	Data Key	OVERLAY	OL_{4-0}
4	CVBS	OVERLAY	OL_{4-0}	PD(YC_BC_R, RGB, CI)	KEY or Data Key	—	—
5	CVBS	PD(YC_BC_R, RGB, CI)	KEY or Data Key	OVERLAY	OL_{4-0}	—	—
6	PD(YC_BC_R, RGB, CI)	CVBS	KEY	OVERLAY	OL_{4-0}	PD(YC_BC_R, RGB, CI)	$\overline{\text{Data Key}}$
7	PD(YC_BC_R, RGB, CI)	CVBS	KEY	OVERLAY	OL_{4-0}	PD(YC_BC_R, RGB, CI)	Data Key
8	PD(YC_BC_R, CI)	CVBS	KEY or Data Key		—	—	—
9	PD(RGB)	PD(YC_BC_R, CI)	$\overline{\text{BYPASS}}$	CVBS	KEY or Data Key	OVERLAY	OL_{4-0}
A	PD(RGB)	CVBS	KEY or Data Key	PD(YC_BC_R, CI)	$\overline{\text{BYPASS}}$	OVERLAY	OL_{4-0}
B	PD(RGB)	CVBS	KEY or Data Key	OVERLAY	OL_{4-0}	PD(YC_BC_R, CI)	$\overline{\text{BYPASS}}$
C	PD(RGB)	PD(YC_BC_R, CI)	$\overline{\text{BYPASS}}$	OVERLAY	OL_{4-0}	CVBS	KEY or Data Key
D	CVBS	PD(RGB)	KEY	PD(YC_BC_R, CI)	$\overline{\text{BYPASS}}$	OVERLAY	OL_{4-0}
E	CVBS	OVERLAY	OL_{4-0}	PD(RGB)	KEY	PD(YC_BC_R, CI)	$\overline{\text{BYPASS}}$
F	PD(RGB)	OVERLAY	OL_{4-0}	CVBS	KEY or Data Key	PD(YC_BC_R, CI)	$\overline{\text{BYPASS}}$

Notes:

1. For LAYMODE = 0 to 7, Pixel Data always passes through the CLUTs. FORMAT, INMODE, and the $\overline{BYPASS}$ pin selects the input format for PD_{23-0} according to Table 6.
2. For LAYMODE = 8 to F and $\overline{BYPASS}$ = HIGH, Data Key is disabled.
3. Asserting the signal listed under "Keying Control:" enables the corresponding "Signal Source:". Signals with "$\overline{\ }$" are asserted by a logic LOW.

Hardware Keying

The KEY input switches the COMPOSITE D/A converter input from the luminance and chrominance combiner output to the CVBS data bus on a pixel-by-pixel basis. This is a "soft" switch, executed over four PXCK periods to minimize out-of-band spurious signals. The video signal from the CVBS bus can only present on the COMPOSITE output. The CHROMA and LUMA outputs continue to present encoded PD port data when CVBS is active.

Hardware keying is enabled by the Key Control Register bit 6. Normally, keying is only effective during the Active Video portion of the waveform as determined by the VA registers 15 and 18. The Horizontal Blanking interval is generated by the encoder state machine even if the KEY signal is held HIGH through Horizontal Blanking. However, it is possible to allow digital Horizontal Blanking to be passed through from the CVBS bus to the COMPOSITE output by setting Key Control Register bit 5 HIGH. In this mode, KEY is always active, and may be exercised at will.

The KEY input is registered into the encoder just like Pixel Data is clocked into the PD port. It may be considered a 25th Pixel Data bit. It is internally pipelined, so the midpoint of the key transition occurs at the output of the pixel that was input at the same time as the KEY signal.

Data Keying

Data Keying internally generates a Key signal that acts exactly as the external KEY signal. There are three Key Value Registers 05, 06, and 07 that are matched against the input data to the three tables in the CLUT. These tables are designated D, E, and F. They contain different information depending on the input mode selected as shown in Table 16.

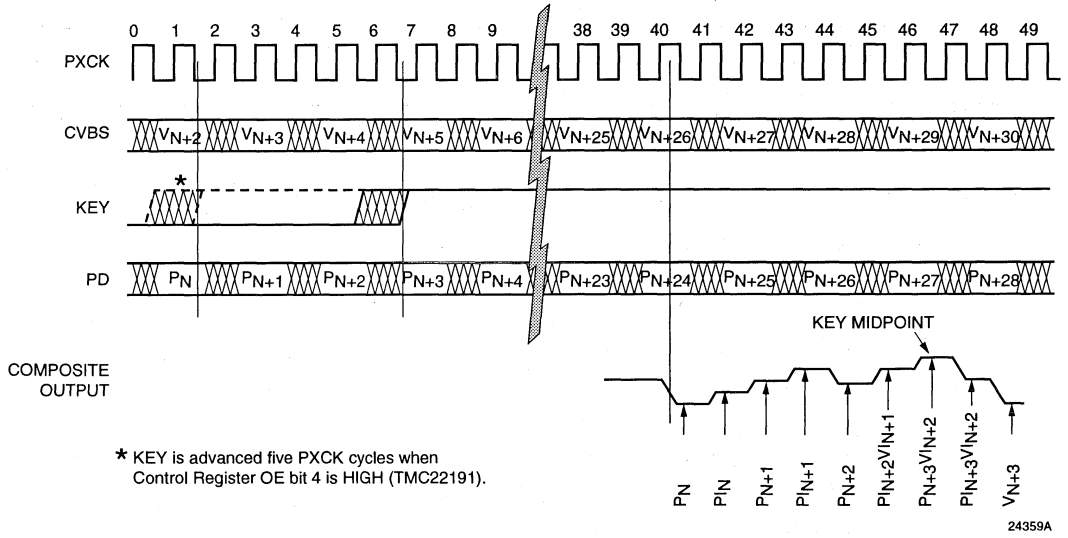


Figure 22. Hardware Keying

The key registers may be individually enabled using bits 3,2,1 of the Key Control Register. Bit 4 of the same register enables/disables Data Keying in its entirety. Data Keying and Hardware Keying are logically ORed: when both are enabled, either one will result in a key switch to the CVBS channel.

The key comparison is based on the input data to the tables in the CLUT. When operating in color-index mode, all three tables receive the same input value, so any one of the three registers is sufficient to identify a key value. The outputs of all enabled key registers are ANDed to produce the KEY signal. If more than one key register are enabled and their key values are not identical, no key will be generated.

Table 16. Table D, E, F Contents

Mode	Table D	Table E	Table F
GBR	Green	Blue	Red
RGB	Red	Green	Blue
YC_BC_R	Y	C_B	C_R
CI	CI	CI	CI

Genlock Interface

The TMC22x91 can process digital composite video connected to its CVBS port. It has been designed to couple tightly with the companion TMC22071 Genlocking Video Digitizer, but it will work with other sources as well.

The digital composite video has to be in standard 8-bit binary format at a PXCK/2 rate. Synchronization with the internal PXCK/2 is established by the phasing of the $\overline{\text{GHSYNC}}$ input, as shown in Figures 24 and 25.

Subcarrier frequency and phase data are transmitted to the encoder over the CVBS bus as 4-bit nibbles on $\text{CVBS}_{3\text{-}0}$ during the horizontal sync period. Field identification is also required for the TMC22x91 internal sync generator. The 14th nibble of the sequence contains no relevant data.

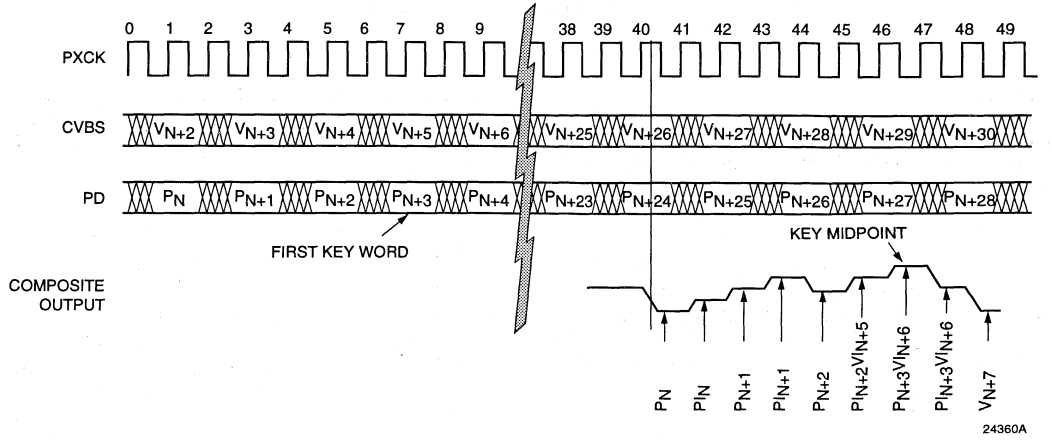


Figure 23. Data Keying

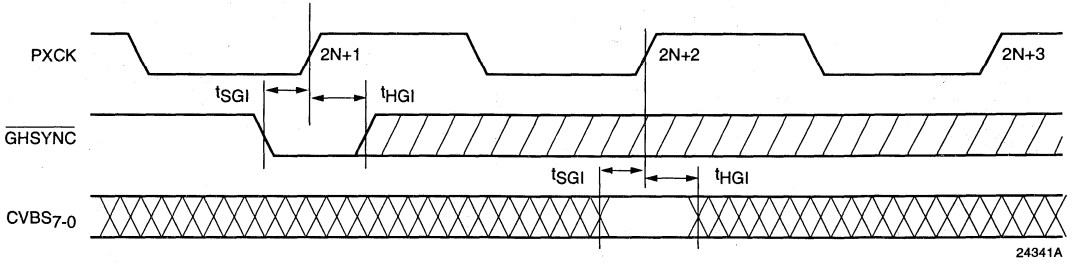


Figure 24. Genlock Interface Timing

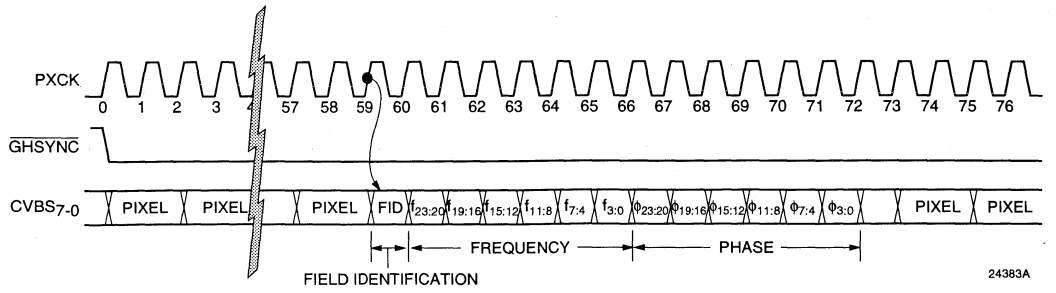


Figure 25. Frequency/Phase Data Transfer

Filtering

The TMC22x91 incorporates internal digital filters to establish appropriate bandwidths and simplify external analog filter designs.

Color-Difference Low-Pass Filters

The color-difference low-pass filters in the TMC22x91 establish chrominance bandwidths which meet the specifications outlined in CCIR Report 624-3, Table II, Item 2.6, for system I over a range of pixel rates from 12.27 Mpps to 14.75 Mpps. Equal bandwidth is established for both color-difference channels.

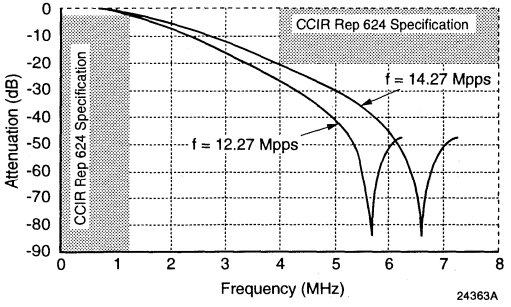


Figure 26. Color-Difference Low-Pass Filter Response

Interpolation Filters

The Chroma Modulator output and the luminance data path are digitally filtered with sharp-cutoff low-pass interpolation filters. These filters ensure that aliased subcarrier, chrominance, and luminance frequencies are sufficiently suppressed in the frequency band above base-band video and below the pixel frequency ($f_S/4$ to $3f_S/4$, where f_S is the PXCK frequency).

Since these are fixed-coefficient digital filters, their filter characteristics depend upon clock rate. Figures 26 and 27 show the frequency response for two pixel rates, 12.27 MHz and 14.75 MHz.

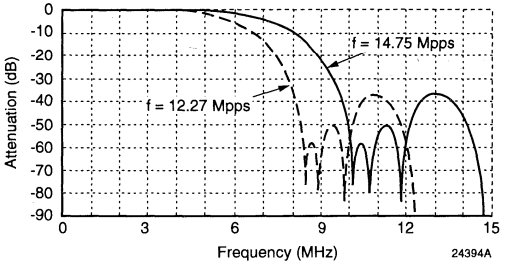


Figure 27. Chroma Modulator and Luminance Interpolation Filter Full Spectrum Response

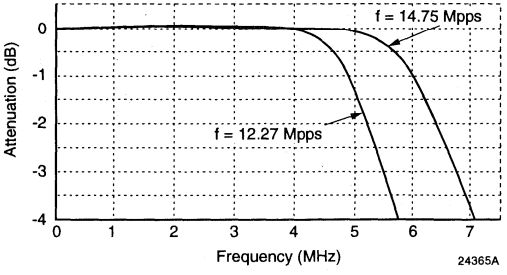


Figure 28. Chroma Modulator and Luminance Interpolation Filter Passband Detail

All digital-to-analog reconstruction systems exhibit a high frequency roll-off as a result of the zero-order hold characteristic of D/A converters. This response is commonly referred to as a sin(x)/x response. It is a function of the sampling rate of the output D/A.

The digital interpolation filters in TMC22x91 convert the data stream to a sample rate of twice the pixel rate. As shown in Figures 27 and 28, the filters decrease the sin(x)/x rolloff and the output spectrum between $f_S/4$ and $3f_S/4$ contains very little energy. Since there is so little signal energy in this frequency band, the demands placed on the output reconstruction filter are greatly reduced. The output filter needs to be flat to $f_S/4$ and have good rejection at $3f_S/4$. The relaxed requirements greatly simplify the design of a filter with good phase response and low group delay distortion. A small amount of peaking may be used to compensate residual sin(x)/x rolloff.

JTAG Test Interface

The JTAG test port accesses registers at every digital I/O pin except the JTAG test port pins. Table 16 shows the sequence of the test registers. The register number (Reg) indicates the order in which the register data is loaded and read (Reg 1 is loaded and read first, therefore it is at the end of the serial path). The scan path is 59 registers long. The six TEST pins of the TMC22091 function as JTAG registers.

The JTAG port is a 4-line interface, following IEEE Std. 1149.1-1990 specifications. The Test Data Input (TDI) and Test Mode Select (TMS) inputs are referred to the rising edge of the Test ClocK (TCK) input. The Test Data Output (TDO) is referred to the falling edge of TCK.

Table 16. JTAG Interface Connections

Reg	Pin	Signal	Reg	Pin	Signal	Reg	Pin	Signal
1	28	$\overline{\text{BYPASS}}$ (TEST)	21	62	PD_{13}	41	2	$CVBS_1$
2	29	OL_4 (TEST)	22	63	PD_{12}	42	3	$CVBS_0$
3	44	$CVBS_7$	23	66	PD_{11}	43	4	KEY
4	45	$CVBS_6$	24	67	PD_{10}	44	5	$\overline{\text{RESET}}$
5	46	$CVBS_5$	25	68	PD_9	45	6	$\overline{\text{CS}}$
6	47	$CVBS_4$	26	69	PD_8	46	7	R/$\overline{\text{W}}$
7	48	OL_3 (TEST)	27	70	PD_7	47	8	A_1
8	49	OL_2 (TEST)	28	71	PD_6	48	9	A_0
9	50	OL_1 (TEST)	29	72	PD_5	49	11	PDC
10	51	OL_0 (TEST)	30	73	PD_4	50	12	$\overline{\text{VHSYNC}}$
11	52	PD_{23}	31	74	PD_3	51	13	$\overline{\text{VVSYNC}}$
12	53	PD_{22}	32	75	PD_2	52	14	D_7
13	54	PD_{21}	33	76	PD_1	53	15	D_6
14	55	PD_{20}	34	77	PD_0	54	16	D_5
15	56	PD_{19}	35	78	LDV	55	17	D_4
16	57	PD_{18}	36	79	PXCK	56	18	D_3
17	58	PD_{17}	37	82	$\overline{\text{GVSYNC}}$	57	19	D_2
18	59	PD_{16}	38	83	$\overline{\text{GHSYNC}}$	58	20	D_1
19	60	PD_{15}	39	84	$CVBS_3$	59	21	D_0
20	61	PD_{14}	40	1	$CVBS_2$			

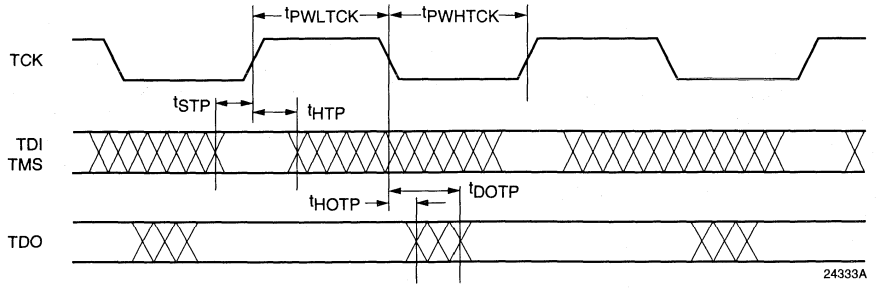


Figure 29. JTAG Test Port Timing

Equivalent Circuits

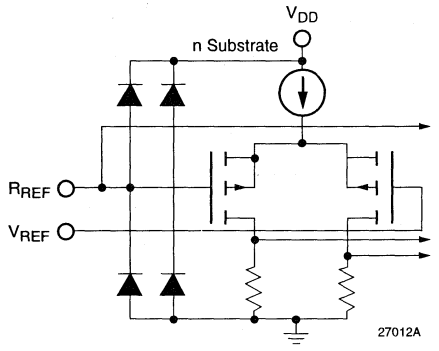


Figure 30. Equivalent Analog Input Circuit

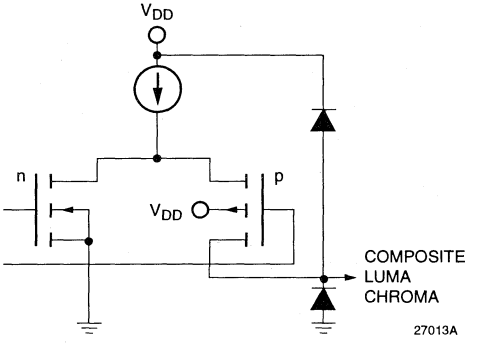


Figure 31. Equivalent Analog Output Circuit

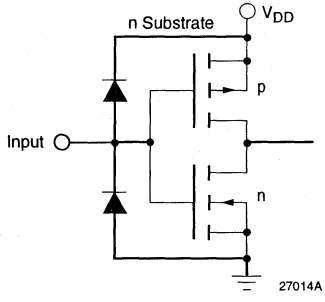


Figure 32. Equivalent Digital Input Circuit

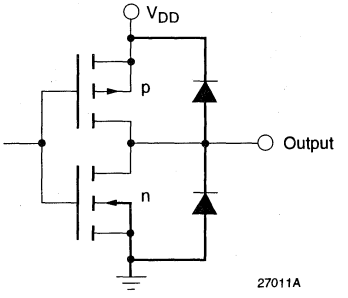


Figure 33. Equivalent Digital Output Circuit

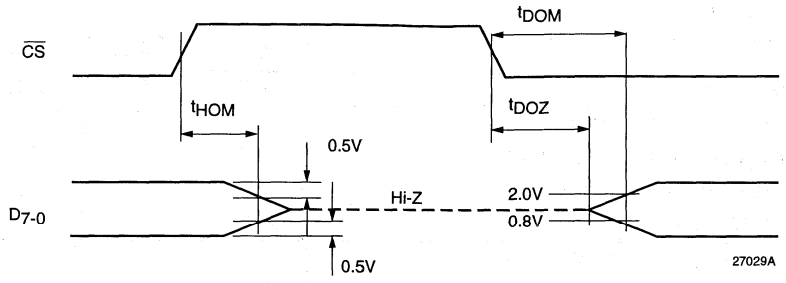


Figure 34. Transition Levels for Three-State Measurements

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Max	Unit
Power Supply Voltage	-0.5	7.0	V
Digital Inputs			
Applied Voltage[2]	-0.5	V_{DD}+0.5	V
Forced Current[3,4]	-20.0	20.0	mA
Digital Outputs			
Applied Voltage[2]	-0.5	V_{DD}+0.5	V
Forced Current[3,4]	-20.0	20.0	mA
Short Circuit Duration (Single output in HIGH state to GND)		1	second
Analog Output Short Circuit Duration (Single output to GND)		infinite	
Temperature			
Operating, ambient	-20	110	°C
Operating, junction, plastic package		140	°C
Lead, soldering (10 seconds)		300	°C
Vapor phase soldering (1 minute)		220	°C
Storage	-65	150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH				
	TTL Compatible Inputs, all but TCK	2.0		V_{DD}	V
	TTL Compatible Input TCK	2.5		V_{DD}	V
	CMOS Compatible Inputs	(2/3)V_{DD}		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW				
	TTL Compatible Inputs	GND		0.8	V
	CMOS Compatible Inputs	GND		(1/3)V_{DD}	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
V_{REF}	External Reference Voltage		1.235		V
I_{REF}	D/A Converter Reference Current, V_{REF} = Nom.	2.1	3.15	4.4	mA
	(I_{REF} = V_{REF} / R_{REF}, flowing out of the R_{REF} pin)				
R_{REF}	Reference Resistor, V_{REF} = Nom.	281	392	588	Ω
R_{OUT}	Total Output Load Resistance		37.5		Ω
T_A	Ambient Temperature, Still Air	0		70	°C
Pixel Interface					
f_{PXL}	Pixel Rate	12.27		15	Mpps
f_{PXCK}	Master Clock Rate, 2x pixel rate	24.54		30	MHz
t_{PWHPX}	PXCK Pulse Width, HIGH	10			ns
t_{PWLPX}	PXCK Pulse Width, LOW	10			ns
For PD, $\overline{VVSYNC}$, $\overline{VHSYNC}$, PDC, KEY					
t_{SP}	Setup Time	12			ns
t_{HP}	Hold Time, PD and KEY	0			ns
t_{HP}	Hold Time, PDC, $\overline{VHSYNC}$, $\overline{VVSYNC}$	5			ns
t_{XL}	Delay Time, LDV	10			ns
t_{PWHLDV}	LDV Pulse Width, HIGH	15			ns
t_{PWLLDV}	LDV Pulse Width, LOW	10			ns
t_{PWLVH}	$\overline{VHSYNC}$ Pulse Width, LOW	6		15	PXCK periods
t_{PWHVV}	$\overline{VVSYNC}$ Pulse Width, LOW	0.5		3	H
Genlock Interface					
t_{SGI}	Setup Time, $\overline{GHSYNC}$, $\overline{GVSYNC}$, CVBS	10			ns
t_{HGI}	Hold Time, $\overline{GHSYNC}$, $\overline{GVSYNC}$, CVBS	0			ns
Microprocessor Interface					
t_{PWLCS}	$\overline{CS}$ Pulse Width, LOW	55			ns
t_{PWHCS}	$\overline{CS}$ Pulse Width, HIGH	30			ns
t_{SA}	Address Setup Time	10			ns
t_{HA}	Address Hold Time	0			ns
t_{SD}	Data Setup Time (write)	15			ns
t_{HD}	Data Hold Time (write)	0			ns

Operating Conditions (continued)

Parameter		Min	Nom	Max	Units
t_{SR}	Reset Setup Time	24			ns
t_{HR}	Reset Hold Time	2			ns
JTAG Interface					
f_{TCK}	Test Clock (TCK) Rate			20	MHz
t_{PWLTCK}	TCK Pulse Width, LOW	10			ns
t_{PWHTCK}	TCK Pulse Width, HIGH	25			ns
t_{STP}	Test Port Setup Time, TDI, TMS	10			ns
t_{HTP}	Test Port Hold Time, TDI, TMS	3			ns

Note:
1. Timing reference points are at the 50% level.

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Current[1]	V_{DD} = Max, f_{PXCK} = 30MHz		250	300	mA
I_{DDQ}	Power Supply Current[1] (D/A disabled)	V_{DD} = Max, f_{PXCK} = 30MHz			60	mA
V_{RO}	Voltage Reference Output		0.988	1.235	1.482	V
I_{BR}	Input Bias Current, V_{REF}	V_{REF} = Nom		100		µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}			10	µA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V			-10	µA
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, Logic LOW	I_{OL} = Max			0.4	V
I_{OZH}	Hi-Z Leakage current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			10	µA
I_{OZL}	Hi-Z Leakage current, LOW	V_{DD} = Max, V_{IN} = GND			-10	µA
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		4	10	pF
C_O	Digital Output Capacitance	T_A = 25°C, f = 1MHz		10		pF
V_{OC}	Video Output Compliance Voltage		-0.3		2.0	V
R_{OUT}	Video Output Resistance			15		kΩ
C_{OUT}	Video Output Capacitance	I_{OUT} = 0 mA, f = 1 MHz		15	25	pF

Note:
1. Typical I_{DD} with V_{DD} = +5.0 Volts and T_A = 25°C, Maximum I_{DD} with V_{DD} = +5.25 Volts and T_A = 0°C.

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
PIPES	Pipeline Delay[3]	PD to Analog Out	44	44	44	PXCK periods
t_{DOZ}	Output Delay, $\overline{CS}$ to low-Z		6		23	ns
t_{DOM}	Output Delay, $\overline{CS}$ to Data Valid[4]				100	ns
t_{HOM}	Output Hold Time, $\overline{CS}$ to hi-Z		10			ns
t_{DOTP}	Output Delay, TCK to TDO Valid				30	ns
t_{HOTP}	Output Hold Time, TCK to TDO Valid			5		ns
t_{DOS}	Output Delay	PXCK to $\overline{VHSYNC}$, $\overline{VVSYNC}$, PDC			25	ns
t_R	D/A Output Current Risetime	10% to 90% of full-scale		2		ns
t_F	D/A Output Current Falltime	90% to 10% of full-scale		2		ns
t_{DOV}	Analog Output Delay			20		ns

Notes:

1. Timing reference points are at the 50% level.
2. Analog C_{LOAD} < 10 pF, D_{7-0} load < 40 pF.
3. Pipeline delay, with respect to PXCK, is a function of the phase relationship between the internally generated PCK (PXCK/2) and PXCK, as established by the hardware reset.
4. t_{DOM} = 1 PXCK + 54 ns = 100 ns worst-case at PXCK = 24.54 MHz.

System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Units
RES	D/A Converter Resolution		10	10	10	Bits
ELI	Integral Linearity Error				0.25	%
ELD	Differential Linearity Error				0.20	%
EG	Gain Error				±10	% FS
dp	Differential Phase	PXCK = 24.54 MHz, 40 IRE Ramp[3]		0.5		degree
dg	Differential Gain	PXCK = 24.54 MHz, 40 IRE Ramp[3]		0.9		%
SKEW	CHROMA to LUMA Output Skew			0	2	ns
PSRR	Power Supply Rejection Ratio	CCOMP = 0.1 µF, f = 1kHz		0.5		%/ %VDD

Notes:

1. TTL input levels are 0.0 and 3.0 Volts, 10%-90% rise and fall times <3 ns.
2. Analog C_{LOAD} < 10 pF, D_{7-0} load < 40 pF.
3. NTSC

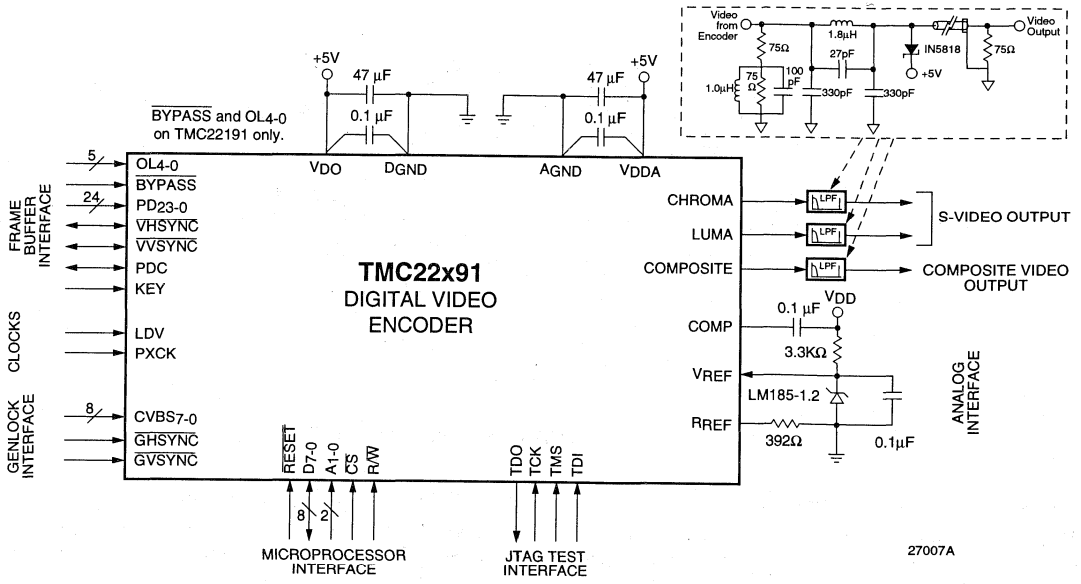


Figure 35. Recommended Interface Circuit

Application Notes

The TMC22x91 is a complex mixed-signal VLSI circuit. It converts digital video signals at clock rates of up to 30 MHz to analog video outputs. A recommended circuit connection is shown in Figure 35.

References

The circuit shown in Figure 35 uses a stable external 1.235V voltage reference. To use the internal voltage reference, simply delete the 3.3kΩ resistor and the LM185-12. A simple voltage divider from the power supply should NOT be used, as any variations in power supply voltage would appear directly on the video outputs.

Filtering

An simple low-pass output reconstruction filter is shown in Figure 36. This filter is located in the video signal path after the COMPOSITE, LUMA, and CHROMA outputs. The value of R_{REF} may be varied to make up for the filter loss.

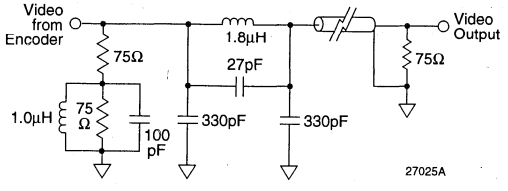


Figure 36. Recommended Output Reconstruction Filter

Interface to the TMC22071 Genlocking Video Digitizer

The TMC22x91 Digital Video Encoder has been designed to directly interface to the TMC22071 Genlocking Video Digitizer. An interface circuit is shown in Figure 37. The microprocessor interface for TMC22x91 and TMC22071 are similar. The R/$\overline{W}$, $\overline{RESET}$, D_0 and A_0 signals from the host microprocessor are shared by the TMC22x91 and TMC22071. The $\overline{CS}$ signals are separately driven from the microprocessor bus.

Grounding Strategy

The TMC22x91 has distinctly separate analog and digital circuits. To minimize digital crosstalk into the analog signals, the power supplies and grounds are provided over separate pins. In general, the best results are obtained by connecting all grounds to a ground plane. Power supply pins should be individually decoupled at the pin.

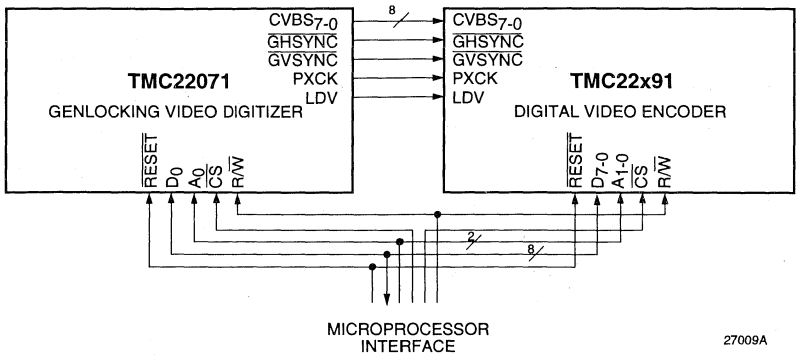


Figure 37. TMC22x91-to-TMC22071 Interface Circuit

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor picture quality. Consider the following suggestions when doing the layout:

1. Keep analog traces (COMP, V_{REF}, R_{REF}) as short and as far from all digital signals as possible.
2. The power plane for the TMC22x91 should be separate from that which supplies other digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC22x91 is the same for the system's digital circuitry, power to the TMC22x91 should be filtered with ferrite beads and 0.1µF capacitors to reduce noise.
3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should be very short.
4. Decoupling capacitors should be applied liberally to V_{DD} pins. For best results, use 0.1µF capacitor in parallel with 47µF capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.
5. The PXCK should be handled carefully. Jitter and noise on this clock or its ground reference will translate to noise on the video outputs. Terminate the clock line carefully to eliminate overshoot and ringing.

Microprocessor I/O Operations

Various CLUT Read/Write operations are shown in Table 17. Each step in the table requires a $\overline{CS}$ pulse (falling edge followed by a rising edge) to execute.

For Write operations, R/$\overline{W}$ and A_{1-0} must conform to setup and hold timing with respect to the falling edge of $\overline{CS}$. D_{7-0} must meet setup and hold timing with respect to the rising edge of $\overline{CS}$. These timing relationships are illustrated in Figure 10. When writing data into an internal register (i.e. CLUT Address Register) an extra $\overline{CS}$ falling edge is required to transfer the input data to that register. This requirement is usually accomplished by executing the next step in the sequence. If there is no planned next step in the sequence, executing a Control Register Read step will meet the requirement and terminate the sequence.

For Read operations, R/$\overline{W}$ and A_{1-0} must conform to setup and hold timing with respect to the falling edge of $\overline{CS}$. Read data on D_{7-0} is initiated by the falling edge of CS\ and terminated by the rising edge of $\overline{CS}$ as shown in Figure 11. When reading Control Registers, valid data appears t_{DOM} after the falling edge of $\overline{CS}$. When reading CLUT locations, an extra CLUT Read step is needed to set up the CLUT Read sequence. This is accomplished in the table by executing an extra CLUT Read step just before the CLUT Read sequence which returns successive d, e, and f data. CLUT Read sequences must be terminated an extra $\overline{CS}$ falling edge. This requirement is usually accomplished by executing the next I/O step. If there is no planned next step in the sequence, executing a Control Register Read step will meet the requirement and terminate the sequence.

Table 17. CLUT Read/Write Sequences

Step	R/W\	A_{1-0}	D_{7-0}	Function
Write Entire CLUT Starting at Address 00				
1	0	01	00	Write 00 into CLUT Address Register.
1	0	01	00	Write 00 into CLUT Address Register.
2	0	11	d1	d1 written into D, CLUT address 00.
3	0	11	e1	e1 written into E, CLUT address 00.
4	0	11	f1	f1 written into F, CLUT address 00.
•••	•••	•••	•••	repeat steps 3, 4, 5 until CLUT is full.
767	0	11	d256	d256 written into D, CLUT address FF.
768	0	11	e256	e256 written into E, CLUT address FF.
769	0	11	f256	f256 written into F, CLUT address FF.
770	1	00	xx	Sequence termination.
Write CLUT Location address				
1	0	01	addr	Write addr into the CLUT Address Register.
2	0	11	d1	d1 written into D, CLUT address addr.
3	0	11	e1	e1 written into E, CLUT address addr.
4	0	11	f1	f1 written into F, CLUT address addr.
5	1	00	xx	Sequence termination.
Read CLUT Location address				
1	0	01	addr	Write addr into the CLUT Address Register.
2	1	11	xx	Set up for CLUT Read sequence.
3	1	11	d1	d1 read from D, CLUT address addr.
4	1	11	e1	e1 read from E, CLUT address addr.
5	1	11	f1	f1 read from F, CLUT address addr.
6	1	00	xx	Sequence termination.
Read CLUT Address Register Then Write				
1	1	01	addr	Read CLUT Address Register.
2	0	11	d1	d1 written into D, CLUT address addr.
3	0	11	e1	e1 written into E, CLUT address addr.
4	0	11	f1	f1 written into F, CLUT address addr.
5	1	01	addr+1	Read CLUT Address Register. (terminates Write sequence)
6	0	11	d2	d2 written into D, CLUT address addr+1.
7	0	11	e2	e2 written into E, CLUT address addr+1.
8	0	11	f2	f2 written into F, CLUT address addr+1.
9	1	00	xx	Sequence termination.

Table 17. CLUT Read/Write Sequences (continued)

Step	R/W\	A_{1-0}	D_{7-0}	Function
Read/Modify/Write CLUT Location address				
1	0	01	addr	Write addr into the CLUT Address Register.
2	1	11	xx	Set up for CLUT Read.
3	1	11	d1	d1 read from D, CLUT address addr.
4	1	11	e1	e1 read from E, CLUT address addr.
5	1	11	f1	f1 read from F, CLUT address addr.
•••	•••	•••	•••	System Modifies d1, e1, f1 to d1', e1', f1'.
6	0	01	addr	Write addr into the CLUT Address Register. (terminates Read sequence)
7	0	11	d1'	d1' written into D, CLUT address addr.
8	0	11	e1'	e1' written into E, CLUT address addr.
9	0	11	f1'	f1' written into F, CLUT address addr.
10	1	00	xx	Sequence termination.

Related Products

- TMC22071 Genlocking Video Digitizer
- TMC2242/2243/2246 Video Filters
- TMC2249 Video Mixer
- TMC2255 Convolver
- TMC2272 Colorspace Converter
- TMC2302 Image Manipulation Sequencer

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC22091R0C	T_A = 0°C to 70°C	Commercial	84-Lead PLCC	22091R0C
TMC22191R0C	T_A = 0°C to 70°C	Commercial	84-Lead PLCC	22191R0C

TMC2011A/TMC2111A

Variable-Length Shift Register

Features

- Low power CMOS
- TMC2011A is a pin compatible replacement for the TDC1011 and TMC2011
- TMC2211A is a pin compatible replacement for the TMC2111
- Inputs and outputs are TTL compatible
- DC–40MHz clock rate
- Selectable delay lengths (TMC2011A: 3 to 18 stages, TMC2111A: 1 to 16 stages)
- Special 4-bit wide mixed-delay mode (TMC2011A)
- Available in 24-pin CERDIP and plastic DIP and 28-lead Plastic Leadless Chip Carrier

Applications

- Video filtering
- High speed data registers
- Local storage registers
- Digital delay lines
- Television special effects
- Pipeline register

Description

The TMC2011A and TMC2111A are high-speed, byte-wide shift registers with programmable delay lengths.

The TMC2011A can be programmed to any length between 3 and 18 stages. It offers a special split-word mode which allows for mixed delay lengths. The TMC2011A, constructed in low-power CMOS, is pin and function compatible with the bipolar TDC1011.

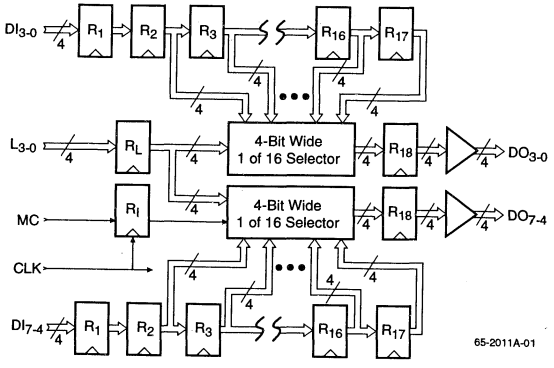
The TMC2111A is a byte-wide shift register that can be programmed to lengths of 1 to 16 stages.

The TMC2011A and TMC2111A are fully synchronous, with all operations controlled by a single master clock. Input and output registers are positive-edge triggered D-type flip-flops. The length and mode controls are also registered. Both devices operate with a maximum clock rate of 40 MHz.

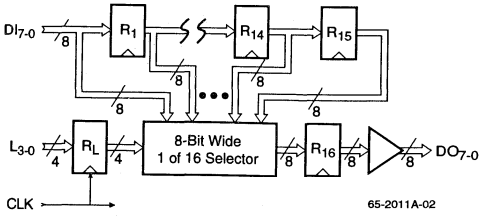
Fabricated in a submicron CMOS process, the TMC2011A and TMC2111A are TTL-compatible, and are available in 24-pin CERDIP and Plastic DIP packages as well as a 28-lead Plastic Leadless Chip Carrier.

Block Diagrams

TMC2011A



TMC2111A

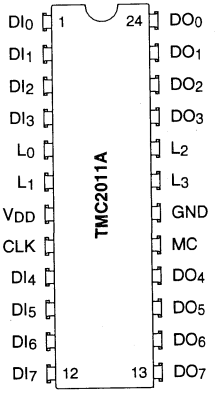


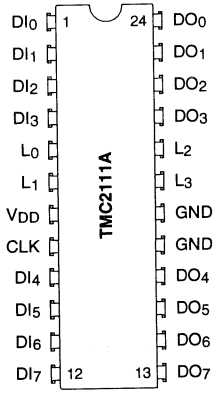
Functional Description

The TMC2011A consists of two 4-bit wide, programmable length shift registers. The TMC2111A consists of a single 8-bit wide, programmable length shift register. The internal registers of each device share control signals and a common clock.

Pin Assignments

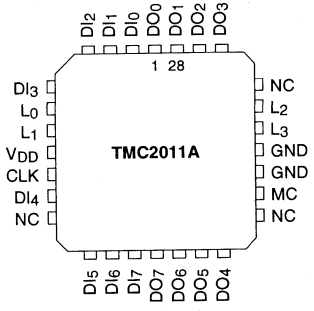
24 Lead DIP (B2, N2) Packages

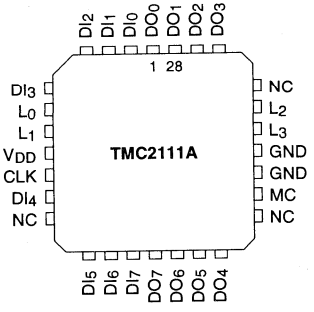




65-2011A-03

28 Lead PLCC (R3) Package





65-2011A-04

Pin Descriptions – TMC2011A

Pin Name	Pin Number DIP	Pin Number PLCC	Pin Function Description
Power			
V_{DD}	7	8	**Supply Voltage.** The TMC2011A and operates from a single +5V supply. All power and ground lines must be connected.
GND	18	21,22	**Ground.** The TMC2011A operates from a single +5V supply. All power and ground lines must be connected.
Data Inputs			
DI_{7-0}	12,11,10, 9,4,3,2,1	14,13,12, 10,5,4,3,2	**Data Input.** Eight inputs are provided for the data, which pass through the shift register unchanged. The eight inputs on the TMC2011A are divided into two groups of four bits to allow mixed delay operation. The lengths of these two groups are different when the Mode Control (MC) is HIGH (see Table 1). When MC is LOW both groups have equal delays.
Data Outputs			
DO_{7-0}	13,14,15, 16,21,22, 23,24	15,16,17, 18,26,27, 28,1	**Data Output.** The outputs of the shift register are delayed relative to the input signals. The amount of the delay is programmable (see Table 1). The outputs remain valid for a minimum of t_{HO} nanoseconds after the leading edge of CLK. This allow the data to be latched into circuits with non-zero hold time requirements.
Controls			
CLK	8	9	**Master Clock.** All inputs and outputs are synchronous and operate from a single master clock. All operations occur on the rising edge of the master clock.
L_{3-0}	19,20,6,5	23,24,7,6	**Length Select.** The length select input is used to determine the register delay of the TMC2011A. This input is registered and affects the output t_{DO} after the clock edge after it is input to the device (see Timing Diagram). Delay lengths are specified in Table 1.
MC	17	20	**Mode Control.** The Mode Control is used to select the special 4-bit wide split mode. When HIGH, the delay on DO_{7-4} is fixed at 18 stages, while DO_{3-0} have the delay specified by the length select. When MC is LOW, all eight bits have equal delays as specified by the length select.

Pin Descriptions – TMC2111A

Pin Name	Pin Number DIP	Pin Number PLCC	Pin Function Description
Power			
V_{DD}	7	8	**Supply Voltage.** The TMC2111A operates from a single +5V supply. All power and ground lines must be connected.
GND	17,18	20,21,22	**Ground.** The TMC2111A operates from a single +5V supply. All power and ground lines must be connected.
Data Inputs			
DI_{7-0}	12,11,10, 9,4,3,2,1	14,13,12, 10,5,4,3,2	**Data Input.** Eight inputs are provided for the data, which pass through the shift register unchanged. The TMC2111A consists of a single group of eight bits with all data bits having equal delays.
Data Outputs			
DO_{7-0}	13,14,15, 16,21,22, 23,24	15,16,17, 18,26,27, 28,1	**Data Output.** The outputs of the shift register are delayed relative to the input signals. The amount of the delay is programmable (see Table 1). The outputs remain valid for a minimum of t_{HO} nanoseconds after the leading edge of CLK. This allow the data to be latched into circuits with non-zero hold time requirements.
Controls			
CLK	8	9	**Master Clock.** All inputs and outputs are synchronous and operate from a single master clock. All operations occur on the rising edge of the master clock.
L_{3-0}	19,20,6,5	23,24,7,6	**Length Select.** The length select input is used to determine the register delay of the TMC2111A. This input is registered and affects the output t_{DO} after the clock edge after it is input to the device (see Timing Diagram). Delay lengths are specified in Table 1.

Table 1. Programming Length Controls

Input Code				TMC2011A				TMC2111A
				Mode (MC) =0		Mode (MC) =1		
L_3	L_2	L_1	L_0	DO_{3-0} Length	DO_{7-4} Length	DO_{3-0} Length	DO_{7-4} Length	DO_{7-0} Length
0	0	0	0	3	3	3	18	1
0	0	0	1	4	4	4	18	2
0	0	1	0	5	5	5	18	3
0	0	1	1	6	6	6	18	4
0	1	0	0	7	7	7	18	5
0	1	0	1	8	8	8	18	6
0	1	1	0	9	9	9	18	7
0	1	1	1	10	10	10	18	8
1	0	0	0	11	11	11	18	9
1	0	0	1	12	12	12	18	10
1	0	1	0	13	13	13	18	11
1	0	1	1	14	14	14	18	12
1	1	0	0	15	15	15	18	13
1	1	0	1	16	16	16	18	14
1	1	1	0	17	17	17	18	15
1	1	1	1	18	18	18	18	16

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage	-0.5		7.0	V
Input Voltage	-0.5		V_{DD} + 0.5	V
Output, Applied Voltage[2]	-0.5		V_{DD} + 0.5	V
Output, Externally Forced Current[3,4]	-3.0		6.0	mA
Output, Short Circuit Duration (single output in HIGH state to ground)			1	sec
Operating, Ambient Temperature	-20		110	°C
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering (10 seconds)			300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2011A, 2111A			30	MHz
		TMC2011A-1, 2111A-1			40	
t_{PWH}	CLK pulse width, HIGH		12			ns
t_{PWL}	CLK pulse width, LOW		12			ns
t_S	Input Data Set-up Time		6			ns
t_H	Input Data Hold Time		1			ns
V_{IH}	Input Voltage, Logic HIGH	DI_{7-0}, L_{3-0}, MC	2.0			V
		CLK	2.6			
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, f_{CLK}=30 MHz V_{DD} = Max, f_{CLK}=40 MHz			30 40	mA mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			0.5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current				-100	mA
V_{OH}	Output Voltage, HIGH	DO_{7-0}, I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	DO_{7-0}, I_{OL} = Max			0.4	V

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			16	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	3			ns

Timing Diagrams

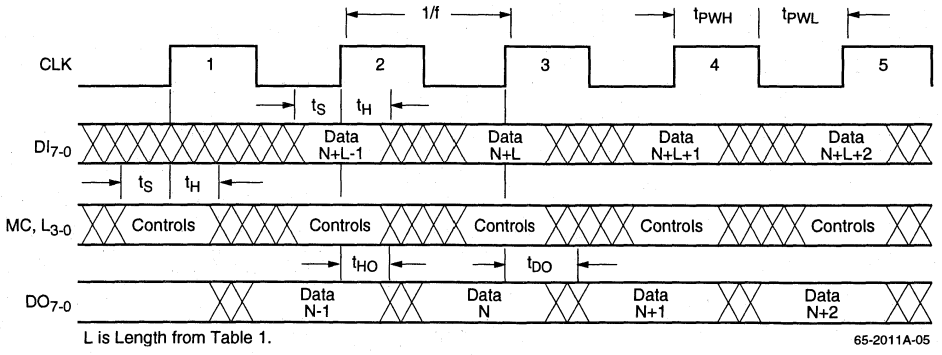


Figure 1. Preset Length Controls

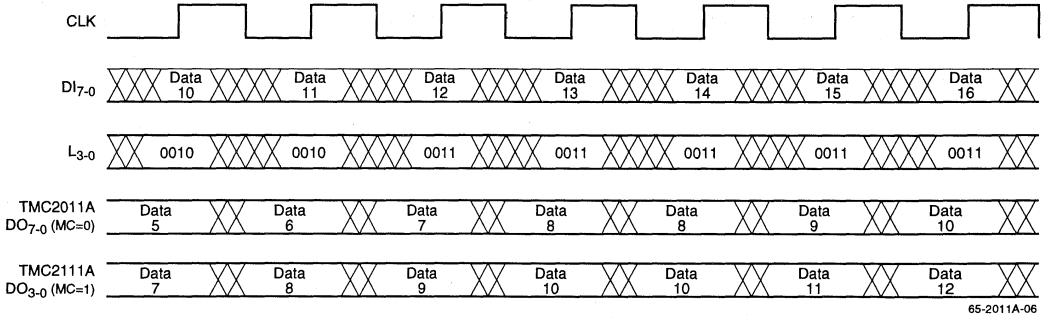


Figure 2. Length Control Operation

Equivalent Circuits

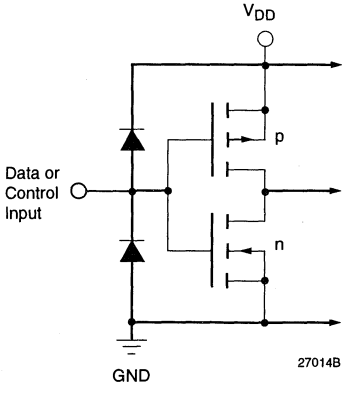


Figure 3. Equivalent Digital Input Circuit

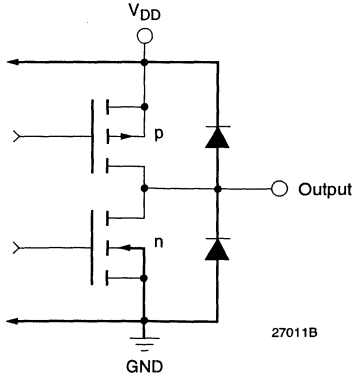


Figure 4. Equivalent Digital Output Circuit

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2011AB2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" CerDIP	2011AB2C
TMC2011AB2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" CerDIP	2011AB2C1
TMC2011AN2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" Plastic DIP	2011AN2C
TMC2011AN2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" Plastic DIP	2011AN2C1
TMC2011AR3C	0°C to 70°C	30 MHz	Commercial	28 Lead PLCC	2011AR3C
TMC2011AR3C1	0°C to 70°C	40 MHz	Commercial	28 Lead PLCC	2011AR3C1
TMC2111AB2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" CerDIP	2111AB2C
TMC2111AB2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" CerDIP	2111AB2C1
TMC2111AN2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" Plastic DIP	2111AN2C
TMC2111AN2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" Plastic DIP	2111AN2C1
TMC2111AR3C	0°C to 70°C	30 MHz	Commercial	28 Lead PLCC	2111AR3C
TMC2111AR3C1	0°C to 70°C	40 MHz	Commercial	28 Lead PLCC	2111AR3C1

TMC2081
Digital Video Mixer

Features

- Mixes 24//16-bit RGB/YC_BC_R444//YC_BC_R422 and 8-bit color-index sources
- 24//16-bit RGB/YC_BC_R444//YC_BC_R422 output
- 256-step proportional mixing via α_{7-0} inputs
- 257-step mixing with α_{8-0} for α=100h unity gain
- 256 x 8-bit look-up table on α channel
- Lap-dissolve and fade effects
- α and crosspoint controls for soft and color-border wipe generation
- Mask register and three 256 x 8 bypassable CLUTs with overlay on A-channel
- Analog preview output with sync on Green/Y
- 15 overlay colors on analog outputs
- D/A power-down modes
- Single +5 volt power supply operation
- Pin compatible with TMC22080 Digital Mixer

Applications

- Mixing computer graphics and live video
- Lap-dissolve between video sources
- Fade to black or to user-selectable fill color
- Window/wipe processing

Description

The TMC2081 is a Digital Video Mixer that performs

$$\mathbf{M} = (\alpha) \mathbf{V}_1 + (1-\alpha) \mathbf{V}_2 (\text{for } 0 \le \alpha \le 1)$$

cross-fading at speeds faster than 40 Mpps proportionally controlled by a 9-bit α-channel input. Variable rate dissolves and fades may be implementedwith unity gain at the α end-points. With the α-Look-Up Table (αLUT), mixing may be controlled by a single bit of the α-channel input. Setup is via a microprocessor interface.

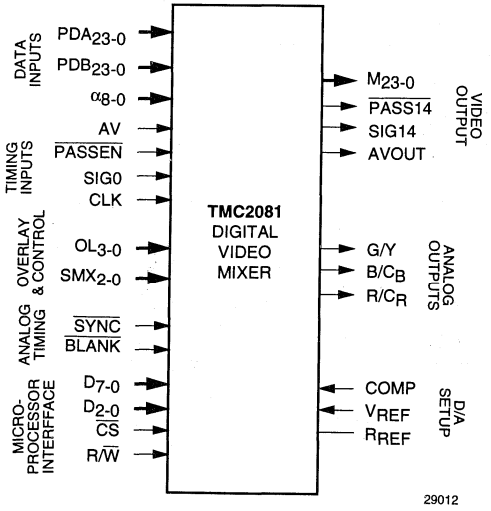
Supported video formats are 24-bit RGB, YC_BC_R444, and 16-bit YC_BC_R422 component video. Dissimilar pixel formats may be mixed using on-chip interpolation and decimation filters and RGB/YC_BC_R and YC_BC_R/RGB color-space conversion matrices.

An additional format accepted by the A-channel is 8-bit color-indexed pixel data which addresses three bypassable 256 x 8 color look-up tables (CLUTs). A 15 color overlay palette and a 24-bit fill register are also included.

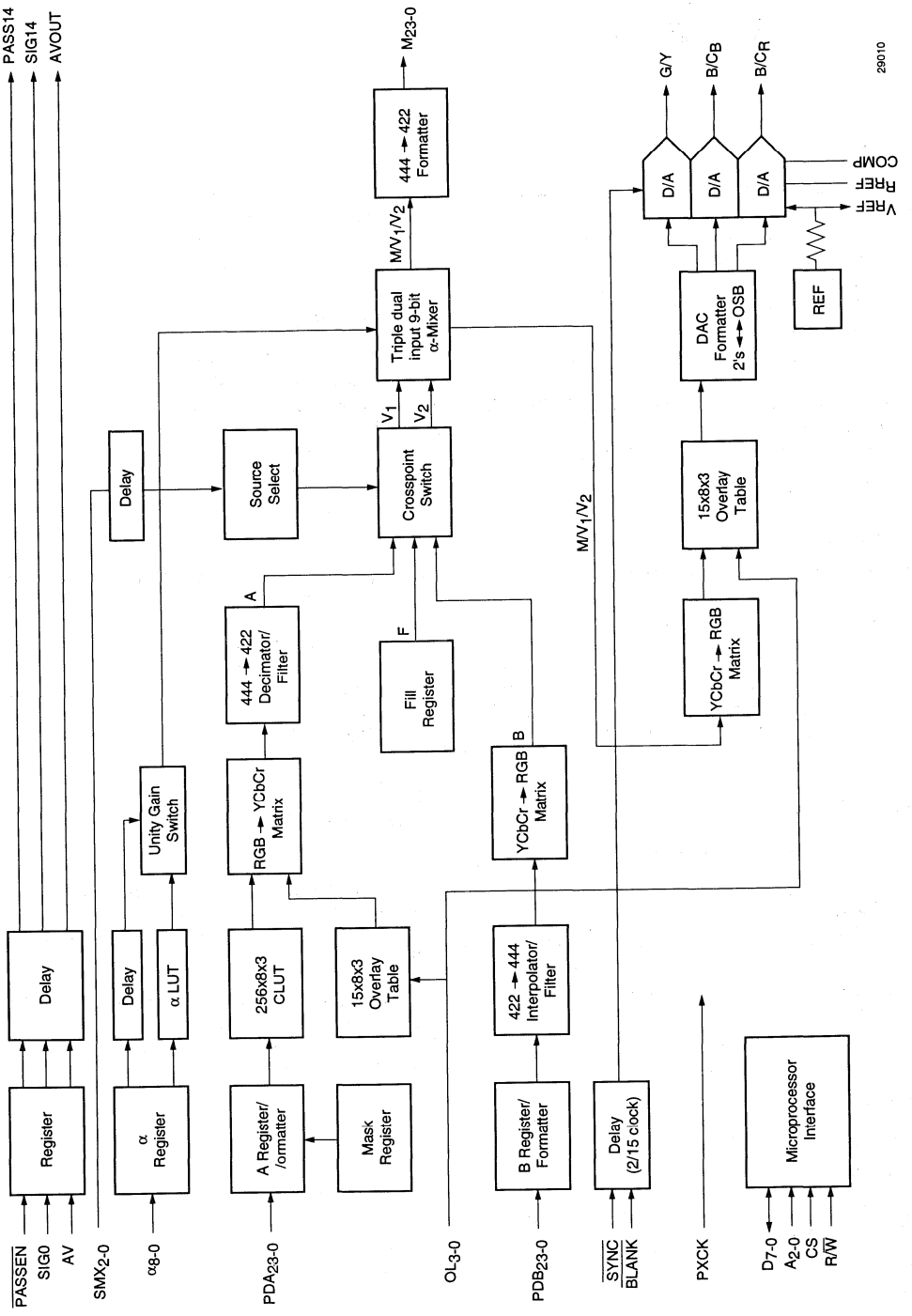
Digital and Analog outputs may be programmed to view either mixer inputs, V_1 or V_2 or mixer output, M. A 15-color overlay is included in the A-channel and the Analog Output channel.

Packaged in a 128-lead plastic quad flat-pack (PQFP), the TMC2081 is fabricated with a sub-micron CMOS process. Performance is guaranteed over the commercial, 0°C to 70°C temperature range.

Logic Symbol



Block Diagram



Functional Description

The TMC2081 is a monolithic digital video processor that proportionally mixes digital video in RGB, YC_BC_R, or color-index formats. Some of the variety of input and output data format combinations are shown in Table 1.

The A-channel data path has transformation circuits that can look up 24-bit RGB values from 8-bit color-index inputs, convert RGB-to-YC_BC_R format, and decimate YC_BC_R444 to YC_BC_R422. The B-channel path includes circuits that convert YC_BC_R to RGB and interpolate YC_BC_R422 to YC_BC_R444. Prior to mixing, incoming pixel data streams must be converted to matching formats by setting the A and B channel control registers.

Data enters the TMC2081 through the PDA_{23-0}, PDB_{23-0}, α_{8-0}, and OL_{3-0} ports. Data and video controls ($\overline{PASSEN}$ and AV) are simultaneously registered on the rising edge of PXCLK. Pipeline latency is 14 clock cycles to the mixed digital video output.

Although PDA_{23-0}, PDB_{23-0}, and M_{23-0} data formats may be different, V_1 and V_2 data formats at the α-Mixer input must be matched: unsigned magnitude for RGB and Y components; 2's complement for C_B and C_R components. Data formats are converted within the TMC2081 by programming internal registers.

Output format may be RGB, YC_BC_R444 or YC_BC_R422. Mixer output or either mixer input may be selected at the M_{23-0} port. Table 2, Table 3 and Table 4 show examples of the M_{23-0} output for 9-bit α-mixing. In Table 3, C_BC_R is accepted by the C_B input. Table 4 exemplifies format conversion.

Mixer output and inputs may be previewed by three video D/A converters. Analog outputs may be either RGB or YC_BC_R.

For initialization and control, internal registers and tables may be accessed through a microprocessor interface.

Power may be conserved by disabling the D/A converters or sections of the TMC2081 via internal Control Registers. In the latter mode, the microprocessor interface remains active and Control Register settings are retained but CLUT locations are not accessible.

Table 1. Input and Output Data Format Examples

A Input Format	B Input Format	A CLUT	A RGB-YC_BC_R	A Decimate	B Interpolate	B YC_BC_R-RGB	M Output Format
YC_BC_R444	YC_BC_R444	Bypass	Bypass	Bypass	Bypass	Bypass	YC_BC_R444
YC_BC_R444	YC_BC_R422	Bypass	Bypass	Bypass	Enable	Bypass	YC_BC_R444
YC_BC_R444	YC_BC_R422	Bypass	Bypass	Enable	Bypass	Bypass	YC_BC_R422
YC_BC_R422	YC_BC_R422	Bypass	Bypass	Bypass	Bypass	Bypass	YC_BC_R422
YC_BC_R422	YC_BC_R422	Bypass	Bypass	Bypass	Bypass	Bypass	YC_BC_R444
RGB, CI	YC_BC_R444	Enable	Bypass	Bypass	Bypass	Enable	RGB
RGB, CI	YC_BC_R444	Enable	Enable	Bypass	Bypass	Bypass	YC_BC_R444
RGB, CI	YC_BC_R422	Enable	Bypass	Bypass	Enable	Enable	RGB
RGB, CI	YC_BC_R422	Enable	Enable	Enable	Bypass	Bypass	YC_BC_R422
RGB, CI	RGB	Enable	Bypass	Bypass	Bypass	Bypass	RGB

Table 2. RGB Mixing Example (9-bit α)

α (hex)	PDA (hex)			PDB (hex)			M (hex)		
	G	B	R	G	B	R	G	B	R
0	BB	CC	AA	EE	FF	DD	EE	FF	DD
40	BB	CC	AA	EE	FF	DD	E1	F2	D0
80	BB	CC	AA	EE	FF	DD	D5	E6	C4
100	BB	CC	AA	EE	FF	DD	BB	CC	AA

Table 3. YC_BC_R422 Mixing Example (C_B and C_R in 2's Complement)

α	PDA (hex)			PDB (hex)			M (hex)		
(hex)	Y	C_B	C_R	Y	C_B	C_R	Y	C_B	C_R
40	10	F4	XX	20	4	XX	1C	00	00
80	10	F4	XX	20	4	XX	18	00	00
40	10	F4	XX	20	4	XX	1C	00	00
40	10	FE	XX	20	2	XX	1C	01	00
A0	30	60	XX	40	70	XX	36	66	00
B0	30	80	XX	40	90	XX	35	86	00
A0	30	C0	XX	40	D0	XX	36	C6	00
B0	30	E0	XX	40	F0	XX	35	E5	00

Table 4. YC_BC_R422-to-YC_BC_R444 Mixing Example

α	PDA (hex)			PDB (hex)			M (hex)		
(hex)	Y	C_B	C_R	Y	C_B	C_R	Y	C_B	C_R
40	10	F4	XX	20	4	XX	1C	00	00
40	10	F4	XX	20	4	XX	1C	00	00
40	10	F4	XX	20	4	XX	1C	00	01
40	10	FE	XX	20	2	XX	1C	00	01
A0	30	60	XX	40	70	XX	36	66	86
B0	30	80	XX	40	90	XX	35	66	86
A0	30	C0	XX	40	D0	XX	36	C6	E5
B0	30	E0	XX	40	F0	XX	35	C6	E5

Input Formats

Data is accepted by PDA and PDB channels in one pair of the following formats:

1. YC_BC_R444.
2. YC_BC_R422.
3. RGB.
4. 8-bit color-index mapped to a palette of 256x256x256 colors. (A-channel only)

Details of bits assignments are shown in Figure 1. Pixel Data Formats with the expected data ranges are shown in Table 5.

Table 5. YC_BC_R and RGB Data Types and Ranges

Signal	Min.	Max.	Format
RGB	0	255	Unsigned Binary
Y	16	235	Unsigned Binary
C_BC_R	-112	+112	2's Complement
			Offset Binary

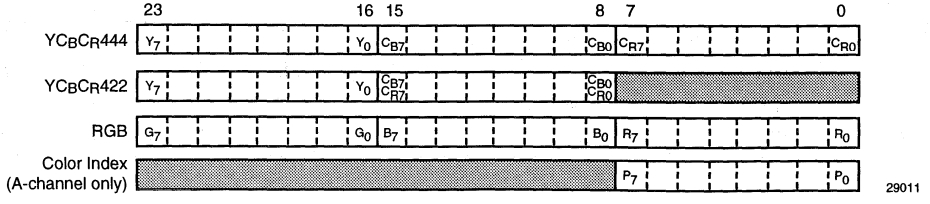


Figure 1. Pixel Data Formats

A-channel Operation

A-channel pixel data, PDA is registered on the rising edge of CLK. C_BC_R datais either passed or format converted (from offset binary to 2's complement) by MSB inversion. 16-bit YC_BC_R422 data is converted to 24-bit YC_BC_R data by pixel replication of C_BC_R data. Each of the three A channel bytes is logically-ANDed with the contents of the Mask Register

The CLUT in the A-channel pixel data path comprises three 256-word x 8-bit sections. When the CLUT is enabled, pixel data addresses the CLUT, which outputs the address contents for subsequent processing. The CLUT may also be bypassed, passing incoming pixel data directly to subsequent circuits.

For 24-bit RGB operation, each of the 256-word by 8-bit CLUTs is independently addressed by green, blue, and red bytes from PDA_{23-0}. For Color-index operation, each of the 256 x 8 CLUTs is addressed by the same pixel data from PDA_{7-0}.

CLUT locations may hold RGB or YC_BC_R color values. V_1 and V_2 mixer input formats must match CLUT formats.

The PDA overlay palette is addressed by four Overlay inputs, OL_{3-0} and is enabled via the Control Register. Each valid Overlay address produces one of 15 24-bit colors selected from stored 8-bit red, green, and blue values. If all four overlay inputs are LOW, CLUT data is output. If any overlay input is HIGH, OL_{3-0} is decoded and the color corresponding to that address is output from the CLUT. OL_{3-0} may be changed on a pixel-by-pixel basis. OL_{3-0} also address the D/A output channel overlay palette.

Table 6. A-channel RGB-to-YC_BC_R Mapping for Fully-Saturated Colors

Color	Input Values			Output Values		
	R	G	B	Y	C_B	C_R
White	255	255	255	235	0	0
Yellow	255	255	0	210	-112	18
Cyan	0	255	255	169	38	-112
Green	0	255	0	144	-74	-94
Magenta	255	0	255	106	74	94
Red	255	0	0	81	-38	112
Blue	0	0	255	41	112	-18
Black	0	0	0	16	0	0

Table 7. B-Channel YC_BC_R-RGB Mapping for Fully-Saturated Colors

Color	Input Values			Output Values		
	Y	C_B	C_R	R	G	B
White	235	0	0	255	255	255
Yellow	210	-112	18	255	255	0

Table 7. B-Channel YC_BC_R-RGB Mapping for Fully-Saturated Colors (continued)

Color	Input Values			Output Values		
	Y	C_B	C_R	R	G	B
Cyan	169	38	-112	0	255	255
Green	144	-74	-94	0	255	0
Magenta	106	74	94	255	0	255
Red	81	-38	112	255	0	0
Blue	41	112	-18	0	0	255
Black	16	0	0	0	0	0

B-channel operation

YC_BC_R444, YC_BC_R422, or RGB are accepted by the B-channel. PDB_{23-0} pixel data is registered on the rising edge of CLK. 16-bit YC_BC_R422 data is converted to 24-bit YC_BC_R422 data by pixel replication of C_BC_R data in the Register/Formatter.

24-bit data is passed to an interpolation filter followed by a color-space converter to ensure that the B-channel data format matches that of the A-channel prior to mixing. Table 1 illustrates the setup of color-space converters, decimation, and interpolation filters. Pipeline latencies of the A and B-channels are matched

Interpolation and Decimation Filters

Digital interpolation and decimation filters in the A- and B-channel paths suppress unwanted artifacts in the chrominance components. Maximum passband attenuation is 0.06 dB. Minimum stopband rejection is 41 dB.

Filters are synchronized with incoming YC_BC_R data by the AV input. When the input format is YC_BB_R422, the incoming pixel following AV transitioning HIGH is assumed to be the C_B pixel. (See Figure 11.)

α-channel Operation

Nine bits of α data are registered on a pixel-by-pixel basis from α_{8-0}. Either 9-bit or 8-bit α values can be selected by setting Control Register Bit αGAIN. Table 8 shows the differences between the gain settings for a 0FF input.

Bits α_{7-0} address a 256 x 8-bit lookup table (αLUT). The αLUT may be used to redefine the function of incoming α data for special effects or low resolution dissolves and fades.

Bit α_8 controls a unity gain switch. If $\alpha_8 = 1$, then α is set to unity gain.

By setting control register bit αLUTEN = 0, the αLUT may be completely bypassed, allowing α_{8-0} to directly control the mixing of A, B and F. αLUT locations may be accessed-via the D_{7-0} microprocessor port.

Table 8. Alpha Channel Gains

α value (hex)	8-bit Gain	9-bit Gain
000	0/256	0/256
001	1/256	1/256
..		
07F	127/256	127/256
080	128/256	128/256
..		
0FE	254/256	254/256
0FF	256/256	255/256
100	256/256	256/256
1XX	256/256	256/256

Fill Color Registers

Three registers, 03, 04, and 05 store a solid fill color, F. Either RGB values or YC_BC_R values may be stored but the format mustmatch the data format of the A- and B-channels at the input to the crosspoint switch.

Fill color registers are accessed through the D_{7-0} microprocessor port. Fill color may be used as an alternative video source for fades.

α-Mixer

There are three sources of data for the mixer: A-channel pixels, B-channel pixels, and the stored fill color, F. One pair of inputs, either AB, BF or FA are selected by the Crosspoint Switch to be passed to the V_1 and V_2. inputs of the α-Mixer. Prior to mixing, V_1 and V_2 data formats must be matched (see Table 1).

Within the α-Mixer are three dual input 9-bit mixers which mix each of the component channels of V_1 and V_2. By varying the value on the α-channel from 000_h to 100_h, the Mixer performs a 256-step transition from one digital video source to the other.

Six dissolve transitions are supported: A-to-B, A-to-F, B-to-A, B-to-F, F-to-A, and F-to-B. Type of dissolve is selected by directing the A-, B-, or F pixels to the V_1 or V_2 mixer input via the ABF Crosspoint Switch. This is done either by internal Control Registers via the microprocessor port or directly through the SMX_{2-0} inputs (see Signal Definitions). SMX_{2-0} input pins are enabled via SMX Control Register bits. When enabled, SMX_{2-0} directly control the ABF Crosspoint Multiplexer on a pixel-by-pixel basis, for externally derived wipe patterns.

Rate of dissolve is controlled directly through the α-channel. Transfer function of the mixer is:

$$M = (\alpha) V_1 + (1-\alpha) V_2$$

where V_1 and V_2 are two of the three inputs A, B or F selected by the crosspoint switch.

For an A-to-B dissolve transition, as the value of the eight LSBs of the α-channel change from 00_h to FF_h, (or 00_h to 100_h in the 9-bit mode), an increasing level of A-channel contribution and a decreasing level of B-channel contribution becomes evident at the output, M.

Bit$\alpha_8$of the α-channel can correct for the 255/256 gain factor in the A-channel that occurs when the 8-bit α value is FF_h. When α_8 =1, bits α_{7-0} are ignored, A-channel gain is set to 256/256 and B-Channel gain is set to 0/256.

Modified transfer functions may be selected for background/foreground and drop-shadow effects by programming control register bits, MIXTFN.

A Foreground Key may be created by forcing (1-α) to zero:

$$M = (\alpha) V_1$$

A Background Key may be created forcing (1-α) to unity:

$$M = (\alpha) V_1 + V_2$$

By using foreground and background mixers in series, drop shadow effects can be implemented.

α may change at pixel rates up to 40 Mpps on a pixel-by-pixel basis, allowing smooth transitions from one video source to another. Transition time interval may vary from many frames to only a few or a single pixel depending upon the rate α-channel data varies.

α_8 may be used like a key input. Either unity gain V_1 or $(1-\alpha)V_2$ may be selected. A- and B-channel pixels may be mixed by switching α_8 on a pixel-by-pixel. Pipeline latencies of the α-, A- and B-channels are matched.

Passing of non-pixel data

In the Passon Mode, the TMC2081 is transparent to data accepted during the $\overline{PASSEN}$ = LOW period (see Figure 10 and Figure 11). Either PDA or PDB data may be selected for Passon of Genlock or Decoder reference signals containing data such as time codes and subcarrier phase and frequency data from upstream video processors.

PASSON and A/BPASS Control Register bits set the modes. If Passon is not selected, when AVOUT = LOW, mixer outputs will beRGB black (M_{23-0} = 00 00 00_h) or YC_BC_R black (M_{23-0} = 10 00 00_h in 2's complement format; M_{23-0} = 10 80 80_h in offset binary format).

Digital Outputs

Data at the M_{23-0} output port, may be selected from either the mixer or, for digital preview, either the V_1 or V_2 mixer input.

A 444-to-422 formatter may be selected or bypassed to convert 24-bit YC_BC_R444 or YC_BC_R422 data to the 16-bit YC_BC_R422 format shown in Figure 1.

Except for color index, all data formats shown in Figure 1 are available:

- YC_BC_R444
- YC_BC_R422
- RGB

Pixel data types and ranges are shown in Figure 1.

M_{23-0} bits are clocked synchronously with the rising edge of CLK. M_{23-0} data outputs may be disabled to a high-impedance state by setting the MOUT Control Register bit LOW.

Analog Preview

Either Crosspoint switch output (V_1 or V_2) or the mixed pixel data output (M_{23-0}) may be monitored by D/A converters. D/A outputs may be either YC_BC_R or RGB. A YC_BC_R-to-RGB matrix prior to the D/A converters may be selected for color-space conversion.

To view V_1 or V_2 data originating in the C_BC_R format, the DACFRM Control Register bit must be set to convert 2's-complement data to the offset binary format.

A 15 x 8 x 3 overlay palette is included in the pixel data path to the D/A converters for overlaying text or graphics over the previewed source. This is useful in systems where pull-down menus are needed, but not wanted over the "program" mixed digital video.

The D/A overlay palette is addressed by the same four overlay inputs that address the PDA overlay palette,OL_{3-0}. The D/A overlay palette is enabled or disabled via the Control Register. Each valid Overlay address produces one of 15 24-bit colors selected from stored 8-bit red, green, and blue values. If all four overlay inputs (OL_{3-0}) are LOW, the overlay palette passes incoming pixel data. If any overlay input is HIGH, OL_{3-0} is decoded and the color corresponding to that address is output from the palette. OL_{3-0} may be changed on a pixel-by-pixel basis.

With the DACSLP bit, D/A converters may be powered down and with the DACOVL bit, the D/A overlay RAM may be powered down.

D/A Converter Outputs

Each D/A converter comprises an array of current sources controlled by data, $\overline{BLANK}$ and $\overline{SYNC}$ inputs. When $\overline{BLANK}$ = HIGH, the SETUP Control Register bit determines if a pedestal is activated. With nominal R_{REF} and V_{REF}, outputs approximate SMPTE 170M levels when terminated with 37.5Ω (75Ω at the source and destination).

Full scale current is set by an external resistor, R_{SET} connected between the R_{REF} pin and A_{GND} and the reference voltage, V_{REF}. V_{REF} may be derived from either a 1.235 volt internal source or an external voltage reference connected to V_{REF}.

Nominal outputs (see Figure 2 and Figure 3) are expressed in Current Units (IU) where 1 IU is equivalent to the current activated by one unit of D/A input data (Gdata/Ydata, Bdata/$C_R$data, or Rdata/$C_B$data). SETUP = HIGH activates a 21 IU pedestal when $\overline{BLANK}$= H. $\overline{SYNC}$ = LOW suppresses a 110 IU offset to form the sync pulse. SETUP is programmed through Register 7 bit 2.

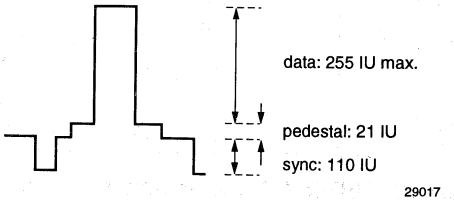


Figure 2. RGB/Y DAC output levels in Current Units

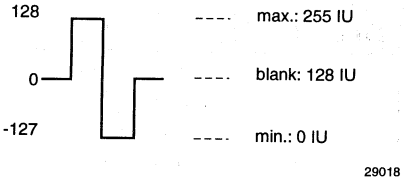


Figure 3. CBCR DAC Output levels in Current Units

To translate IUs to millivolts, V_{REF} and R_{SET} must be set to the correct values, nominally V_{REF} = 1.235 volt and R_{SET} = 681 ohms. In each table below, G and the Y outputs have been normalized to 1000 mV with Data = 255.

Since V_{REF} and R_{REF} are common to all D/A converters, B and R full scale outputs track G. C_B C_R full scale outputs track Y. R_{REF} may be trimmed to set the G or Y full scale voltage to 1000 mV.

In the equations for the RGB and YC_BC_R outputs that follow, symbols are defined as:

+ = plus

* = multiply

& = logical AND

! = logical complement

RGB Output

Expressed in IUs, the RGB transformation from data to current is as follows:

G = (Gdata + SETUP * 21) & $\overline{BLANK}$ + $\overline{SYNC}$ * 110

B = (Bdata + SETUP * 21) & $\overline{BLANK}$

R = (Rdata + SETUP*21) & $\overline{BLANK}$

Sample outputs are listed in Table 9 and Table 10.

Table 9. GBR DAC Transfer Characteristic without Pedestal (SETUP = L)

D/A Input Data	SYNC	BLANK	G IU	G mV	B or R IU	B or R mV
255	1	1	365	1000	255	699
128	1	1	238	652	128	351
0	1	1	110	301	0	0
X	1	0	110	301	0	0
X	0	0	0	0	0	0
128	0	1	128	351	128	351

Table 10. GBR DAC Transfer Characteristic with Pedestal (SETUP = H)

D/A Input Data	SYNC	BLANK	G IU	G mV	B or R IU	B or R mV
255	1	1	386	1000	276	715
128	1	1	259	671	149	386
0	1	1	131	339	21	54
X	1	0	110	285	0	0
X	0	0	0	0	0	0
128	0	1	149	386	149	386

YC_BC_R Output

Data inputs are unsigned Ydata and offset-binary format $C_B$data and $C_R$data. $\overline{BLANK}$ = L sets C_B and C_R outputs to 128, the value for zero chrominance data. YC_BC_R transfer equations are:

$Y = (Ydata + SETUP * 21) \& \overline{BLANK} + \overline{SYNC} * 110$

$C_B = (Cdata + SETUP * 21) \& \overline{BLANK} + 128 \& !\overline{BLANK}$

$C_R = (Cdata + SETUP * 21) \& \overline{BLANK} + 128 \& !\overline{BLANK}$

Sample outputs are listed in Table 11 and Table 12.

Table 11. YCrCb DAC Transfer Characteristic without Pedestal (SETUP = L)

D/A Input Data	SYNC	BLANK	Y IU	Y mV	C_B or C_R IU	C_B or C_R mV
255	1	1	365	1000	255	699
128	1	1	238	652	128.	351
64	1	1	174	477	64	175
0	1	1	110	301	0	0
X	1	0	110	301	128	351
X	0	0	0	0	128	351
64	0	1	64	175	64	175

Table 12. YCrCb DAC Transfer Characteristic with Pedestal (SETUP = H)

D/A Input Data	SYNC	BLANK	Y IU	Y mV	C_B or C_R IU	C_B or C_R mV
255	1	1	386	1000	276	715
128	1	1	259	670	149	386
64	1	1	195	505	85	220
0	1	1	131	339	21	54
X	1	0	110	285	149	386
X	0	0	0	0	149	386
64	0	1	85	220	85	220

Dissolve and Crossfade Operation

Video transitions such as dissolve and fades may be executed by direct α-channel control. Rate and start time for the transition depends entirely upon the value of the $\alpha_{8\text{-}0}$ inputs. Transitions may be executed as quickly or slowly as values are presented to the α-channel. Transitions may remain partially executed by keeping α-values constant.

It is possible to mix modes, bringing data in either 444 or 422 format and outputting data in 422 or 444 format.

In the 444/444 mode (see Figure 7), α is applied to each YC_BC_R or RGB pixel pair at the input of the mixer. The YC_BC_R444 output is mixed at the full α rate.

In the 422/422 mode (see Figure 8), α mixes theY component of incoming PDA and PDB pixels. Only odd indexed α's mix C_BC_R components. α-values applied to C_BC_R change synchronously with C_B data. Consequently, full bandwidth α data is applied to the luminance channel but the chrominance channel α values are decimated by dropping the even values that are synchronous with C_R data.

In the 422/444 mode (see Figure 9), YC_BC_R422 data is accepted at the PDA and PDB port but the output at the $M_{23\text{-}0}$ port is YC_BC_R444. α may change from pixel-to-pixel with mixing at the $M_{23\text{-}0}$ outputs tracking both Y and C_BC_R. Although odd values of C_B and C_R are repeated at half the pixel rate, α transitions are applied to C_B and C_R at the pixel rate.

Microprocessor Interface

Internal Control Registers, CLUT, αLUT, and Overlay palettes are accessed through a bi-directional microprocessor port, $D_{7\text{-}0}$. Table 13 shows how address bits, $A_{2\text{-}0}$ select the registers to be accessed.

Table 13. Microprocessor Port Address Map

A_{2-0}	Action
000	RAM Address Register for CLUT, αLUT, and overlay palettes for write operations
001	Directs RAM R/W operations selected by the two MSBs of Control Address Register
010	reserved
011	RAM Address Register for CLUT, αLUT, and overlay palettes for read operations
100	reserved
101	Directs Control Register R/W operations selected by the four LSBs of the Control Address Register
110	Mask Register
111	Control Address Register

As shown in Table 14, to access a control register, Control Address Register bits D_{3-0} must be set to specify one of the nine control registers shown in Table 17. For access to LUTs and Overlay palettes, Control Address Register bits D_{7-6} must be set to select the address of one of the four RAMs shown in Table 14.

Table 14. Control Address Register Bit Definitions

RAM Select		Reserved		Control Register Address			
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
00		A-channel CLUT					
01		A-channel Overlay palette					
10		D/A Overlay palette					
11		αLUT					

Figure 4 and Figure 5 (see page 20) show the microprocessor port read and write timing cycles. Table 15 shows the Control Register read and write sequences.

When loading or reading look-up tables or overlay palettes, with the exception of α-LUT write, the address pointer is auto-incremented after each read or write operation. For α-LUT write, the address pointer is pre-incremented, so that the address must be set one address before the required address. For α-LUT read, the address pointer is post-incremented.

When accessing the A-channel CLUT, A-channel Overlay palette, or D-Overlay palette, each address location must be written/read three consecutive times for red (R/C_R), green (G/Y), and blue (B/C_B) data. After accessing the blue data, the address pointer auto-increments.

In Table 16, note that:

1. To read the α-LUT, Control Register 06h, bit 5 must be set to enable the α-LUT.
2. To read the CLUT and Overlay Table, Control Register 00h, bit 4 (CLUT) must be set to enable both the CLUT and Overlay Table.
3. Data may be written to the CLUT or αLUT with Control Register bits set to enable or bypass.
4. When writing to the α-LUT, the address pre-increments. The address pointer is set to FFh, one address before address 00h.

Power and Ground

The TMC2081 operates from a single +5 Volt power supply. Multiple power and ground pins are assigned and must be connected.

Table 15. Control Register Read/Write Sequences

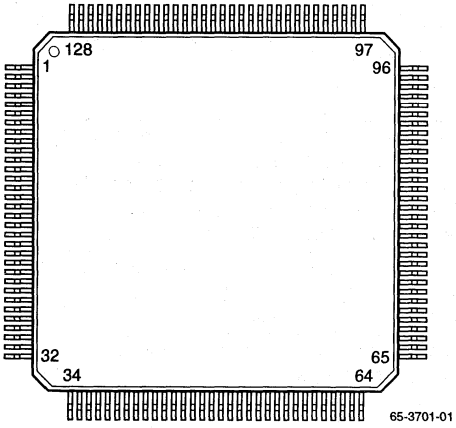
Step	R/$\overline{W}$	A_{2-0}	D_{7-0}	Function
Write to all Control Registers				
1	0	111	x0	Writes 0 to Address Control Register (selects the A-channel Control Register)
2	0	101	aa	Writes aa into A-channel Control Register
.	..	..	..	Repeat steps 1 and 2 incrementing data to Address Control Register
15	0	111	07	Writes 07 to Address Control Register (selects the D/A Control Register)
16	0	101	bb	Writes bb into D/A Control Register
Read/Modify/Write Mixer Control Register				
1	0	111	x2	Writes 02 to Address Control Register (selects the Mixer Control Register)
2	1	101	aa	Mixer Control Register contents, aa, available on D_{7-0}.
.	..	..	..	System modifies aa to get bb.
3	0	101	bb	Writes bb into Mixer Control Register

Table 16. CLUT Read/Write Sequences

Step	$\overline{R/W}$	A_{2-0}	D_{7-0}	Function
Write Entire A-channel CLUT From Address 00				
1	0	111	0x	Selects A-CLUT for R/W.
2	0	000	00	Presets RAM Address Register to FF.
3	0	001	r0	r0 written into red (R/C_R) CLUT address 00.
4	0	001	g0	g0 written into green (G/Y) CLUT address 00.
5	0	001	b0	b0 written into blue (B/C_B) CLUT address 00.
.	..	..	..	repeat steps 3,4,5 until A-CLUT is full.
768	0	001	r255	r255 written into red (R/C_R) CLUT address FF.
769	0	001	g255	g255 written into green (G/Y) CLUT address FF.
770	0	001	b255	b255 written into blue (B/C_B) CLUT address FF.
Write RGB data to A-Overlay Location address				
1	0	111	4x	Select A-channel Overlay
2	0	000	a_n	Write a_n into RAM Address Register.
3	0	001	r_n	r_n written into red (R/C_R) CLUT address.
4	0	001	g_n	g_n written into green (G/Y) CLUT address.
5	0	001	b_n	b_n written into blue (B/C_B) CLUT address.
Write all αLUT Locations starting from 00				
1	0	111	Cx	Select αLUT
2	0	011	FF	Write FF into RAM Address Register (sets address to FF for pre-increment).
3	0	001	αα	Write αα to αLUT location 00.
.	..	..	..	Repeat step 3, 254 times for locations 01h-FEh.
258	0	001	ζζ	Write ζζ, to αLUT location FF.
Read all αLUT Locations starting from 00				
1	0	111	C6	Select αLUT and Register 06 in Address Control Register
2	1	101	αα	Read Control Register 06
3				bb = (aa OR 20h) to set bit 5
4	0	101	bb	Restores aa with αLUT enabled
5	0	011	00	Write 00 into RAM Address Register (sets address to 00).
6	1	001	aa	Read contents of αLUT, αα, from location 00.
.	..	..	..	Repeat step 6 x254 for locations 01h-FEh.
261	1	001	ζζ	Read contents of αLUT, ζζ, from last location FF.

Pin Assignments

128 Pin Plastic Quad Flat Pack (PQFP), KB Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	D_5	33	PDA_{11}	65	R/C_R	97	M_{22}
2	D_4	34	PDA_{10}	66	B/C_B	98	M_{21}
3	D_3	35	PDA_9	67	A_{GND}	99	M_{20}
4	D_2	36	PDA_8	68	G/Y	100	M_{19}
5	D_1	37	PDA_7	69	COMP	101	M_{18}
6	D_0	38	PDA_6	70	V_{DDA}	102	M_{17}
7	$\overline{CS}$	39	PDA_5	71	V_{DDA}	103	M_{16}
8	$R/\overline{W}$	40	PDA_4	72	PDB_{23}	104	D_{GND}
9	A_0	41	PDA_3	73	PDB_{22}	105	V_{DD}
10	A_1	42	PDA_2	74	PDB21	106	M_{15}
11	A_2	43	PDA_1	75	PDB20	107	M_{14}
12	SIG0	44	PDA_0	76	PDB19	108	M_{13}
13	$\overline{PASSEN}$	45	α_8	77	PDB18	109	M_{12}
14	AV	46	α_7	78	PDB17	110	M_{11}
15	OL_3	47	V_{DD}	79	PDB16	111	M_{10}
16	V_{DD}	48	D_{GND}	80	PDB15	112	M_9
17	D_{GND}	49	α_6	81	PDB14	113	M_8
18	OL_2	50	α_5	82	PDB13	114	M_7
19	OL_1	51	α_4	83	PDB12	115	M_6
20	OL_0	52	α_3	84	PDB11	116	M_5
21	PDA_{23}	53	α_2	85	PDB10	117	M_4
22	PDA_{22}	54	α_1	86	PDB9	118	M_3
23	PDA_{21}	55	α_0	87	PDB8	119	M_2
24	PDA_{20}	56	SMX_2	88	PDB7	120	M_1
25	PDA_{19}	57	SMX_1	89	PDB6	121	M_0
26	PDA_{18}	58	SMX_0	90	PDB5	122	AVOUT
27	PDA_{17}	59	CLK	91	PDB4	123	$\overline{PASS14}$
28	PDA_{16}	60	$\overline{BLANK}$	92	PDB3	124	SIG14
29	PDA_{15}	61	$\overline{SYNC}$	93	PDB2	125	D_{GND}
30	PDA_{14}	62	V_{REF}	94	PDB1	126	V_{DD}
31	PDA_{13}	63	R_{REF}	95	PDB0	127	D_7
32	PDA_{12}	64	A_{GND}	96	M23	128	D_6

Pin Descriptions

Name	Pin Number	Value	Pin Function Description
Clock			
CLK	59	TTL	**Clock Input.** TTL-compatible clock. All pixel data is registered on the rising edge of CLK. CLK synchronizes the flow of pixel data through the TMC2081 and the operation of the α-input.
Pixel I/O			
PDA_{23-0}	21-44	TTL	**A-channel pixel inputs.** A-channel pixel inputs are registered on the rising edge of CLK and specify which of the CLUT locations are addressed after masking. If the CLUTs are bypassed, the A-channel pixel data is sent on to the mixer section. PDA_{7-0} are applied to all three CLUT sections when color-index pixel data is used.
PDB_{23-0}	72-95	TTL	**B-channel pixel inputs.** B-channel pixel inputs are registered on the rising edge of CLK and are applied to the mixer after color-space conversion, and interpolation, if selected.
α_{8-0}	45,46,49-55	TTL	**α-channel inputs.** The α-channel inputs are registered on the rising edge of CLK and control proportional mixing at pixel rates up to 40 Mpps. α_8 acts as a key input, switching A- and B-channel pixel data on a pixel-by-pixel basis. α_0 is the LSB.
SMX_{2-0}	56-58	TTL	**ABF Crosspoint Mux control.** When enabled by setting the SMX Control Register bits to 111, these inputs control the ABF Crosspoint Switch which directs the A- or B-channel pixels or the fill color register values to the V_1 or V_2 inputs to the mixer. SMX_{2-0} input pins are ignored when the SMX Control Register bits are not 111. SMX_{2-0} are registered on the rising edge of CLK. ABF Crosspoint Switch control is according to the following:

SMX_{2-0}	V_1	V_2
000	A	B
001	A	F
010	B	A
011	B	F
100	F	A
101	F	B
110	-	-
111	-	-

OL_{3-0}	15,18-20	TTL	**Overlay inputs.** Overlay inputs select one of 15 overlay colors from both the PDA and D/A overlay palettes. OL_{3-0} are registered on the rising edge of CLK. When PDA or D/A overlay are enabled and OL_{3-0} > 0, the contents of the addressed palette are output in place of the pixel data. Overlay is inactive when $OL_{3-0} = 0_h$ or when disabled via the Control Registers. OL_0 is the LSB.
M_{23-0}	96-103, 106-121	TTL	**Mixed pixel outputs.** Mixer output or digital preview of the V_1 and V_2 Crosspoint Switch outputs are synchronized to the rising edge of CLK. M_{23-0} date is passed on for further processing (mixing, encoding, etc.). Pipeline latency is 14 clock cycles.

Pin Descriptions (continued)

Name	Pin Number	Value	Pin Function Description
Video Controls			
$\overline{\text{PASSEN}}$	13	TTL	**Passon enable input.** Passon Enable. Data selected by A/BPASS is enabled by $\overline{\text{PASSEN}}$.
SIG0	12	TTL	**Signal 0 input.** Signal 0 input. (Has no internal function.)
$\overline{\text{PASS14}}$	123	TTL	**Pass enable output (14 clock delay).** $\overline{\text{PASSEN}}$ delayed by 14 CLK cycles to match the pipeline latency of pixels
SIG14	124	TTL	**Signal 0 output (14 clock delay).** SIG0 delayed to match the 14 CLK cycles pipeline latency of pixels
AV	14	TTL	**Active Video input.** Active Video Input. When HIGH, AV enables data from the PDA and PDB ports. When LOW, at the M_{23-0} output, RGB data is set to zero and YC_BC_R data is set to 10_h 80_h 80_h in the offset binary format and 10_h 00_h 00_h in 2's complement format. In the 422 mode, AV transitioning HIGH defines the next pixel to be the first C_B pixel.
AVOUT	122	TTL	**Delayed AV Output.** AV delayed by either 12 or 14 clock cycles. A 14 clock cycle delay matches the pipeline delay of the A and B channels. A 12 clock cycle delay is useful for interfacing with Raytheon Encoders
$\overline{\text{SYNC}}$	61	TTL	**Sync input for G/Y D/A.** D/A Converter sync input. $\overline{\text{SYNC}}$= LOW, disables a current source at the G/Y output, forcing the sync tip to zero volts. $\overline{\text{SYNC}}$ = HIGH, activates the sync current at the G/Y output. $\overline{\text{SYNC}}$ is delayedeither 2 or 15 clock cycles according to the status of the DACDLY bit. To disable sync on G/Y, ground $\overline{\text{SYNC}}$.
$\overline{\text{BLANK}}$	60	TTL	**Blanking control for D/As.** D/A Converter blanking input. $\overline{\text{BLANK}}$ = LOW disables the data and pedestal output currents. If $\overline{\text{BLANK}}$ = HIGH, data and pedestal currents are added to the SYNC current. $\overline{\text{BLANK}}$ is delayed either 2 or 15 clock cycles according to the status of the DACDLY bit. For blank levels, see Tables 9, 10, 11, and 12.
Microprocessor I/O			
R/$\overline{\text{W}}$	8	TTL	**Bus Read/Write control.** Read-Write control input. R/$\overline{\text{W}}$ controls the direction of the D_{7-0} port. If R/$\overline{\text{W}}$ = HIGH and $\overline{\text{CS}}$ is LOW, registers or CLUTs may be read. If R/$\overline{\text{W}}$ = LOW and $\overline{\text{CS}}$ = LOW, data may written to control registers or CLUTs via the D_{7-0} port. R/$\overline{\text{W}}$ is latched on the falling edge of $\overline{\text{CS}}$.
$\overline{\text{CS}}$	7	TTL	**Bus Chip Select.** Chip Select Input. If $\overline{\text{CS}}$ = HIGH, port, D_{7-0}, is set to high-impedance. If $\overline{\text{CS}}$ = LOW, port D_{7-0} is enabled. Read data (R/$\overline{\text{W}}$ = HIGH) is enabled on the falling edge of $\overline{\text{CS}}$ of the $\overline{\text{CS}}$ = LOW strobe. Write data is latched into the TMS2081 on the rising edge of the $\overline{\text{CS}}$ strobe. CLUT, αLUT, or overlay read/write operations require $\overline{\text{CS}}$ to be HIGH for at least 4 CLK cycles after the $\overline{\text{CS}}$ = LOW strobe.
A_{2-0}	11-9	TTL	**Register Select controls.** Address bits input. A_{2-0} select registers or tables to be accessed (see Table 13) via D_{7-0}. A_{2-0} are latched on the falling edge of $\overline{\text{CS}}$.
D_{7-0}	127,128, 1-6	TTL	**Data I/O port.** Bi-directional data port. D_0 is the LSB. Control Registers, CLUT, αLUT and Overlay locations are accessed via D_{7-0}.
Video Output			
G/Y	68	1 V P-P	**Green/Luminance video.** The green/luminance analog video output. Sync pulses are included on this output.
B/C_B	66	0.7 V P-P	**Blue/C_B video.** Blue/C_B analog video output.
R/C_R	65	0.7 V P-P	**Red/C_R video.** Red/C_R analog video output.

Pin Descriptions (continued)

Name	Pin Number	Value	Pin Function Description
Reference			
VREF	62	+1.23 V	**Voltage reference input/output.** An internal voltage source of +1.2 Volts (nominal) is applied to the VREF terminal. This is the reference for all three D/A converters of the TMC2081. Decoupling VREF to AGND with a 0.1µF ceramic capacitor is recommended. This pin may also be used as an input for an external voltage reference source (+1.2 V).
RREF	63	681 Ω	**Current-setting resistor.** Full-scale output current of the TMC2081 is determined by the value of the resistor connected between RREF and AGND. Varying this resistor will varythe "white" output level for all three D/A converters. The TMC2081 is not designed for operation with an external current reference.
COMP	69	0.1 µF	**Compensation capacitor.** A 0.1 µF ceramic capacitor is connected between the COMP and VDDA terminals.
Power, Ground			
VDDA	70,71	+5 V	**Analog power supply.** The TMC2081 operates from a single +5V supply. All power pins must be connected.
VDD	16,47,105,126	+5 V	**Digital power supply.** The TMC2081 operates from a single +5V supply. All power pins must be connected.
AGND	64,67	0.0 V	**Analog ground.** All ground pins must be connected.
DGND	17,48,104,125	0.0 V	**Digital ground.** All ground pins must be connected.

Control Register Map

Reg	Bit	Name	Function
A-Channel Control Register			
00	7	AOVLEN	A-channel Overlay enable/ disable
00	6	ADEC	Decimator bypass/enable
00	5	AMAT	A-channel RGB-to-YC_BC_R bypass/enable
00	4	CLUT	Bypass/enable CLUT (power down)
00	3	AMSB	Inverts C_B/C_R MSB
00	2	αGAIN	Alpha Channel 9-/8-bit unity gain
00	1-0	AFORMAT	A Pixel data path setup (4 formats)
B-Channel/Mixer Control Register			
01	7		Reserved
01	6-5	MSOURCE	M_{23-0} pixel source
01	4	BMAT	Bypass/enable the B-channel YC_BC_R-to-RGB
01	3	BINT	Bypass/enable Interpolator
01	2	BMSB	Inverts C_B/C_R MSB
01	1-0	BFORMAT	B Pixel data path setup (4 formats)
Mixer Control Register			
02	7	MIXFMT	Mixer format select
02	6-5	DSOURCE	Selects data source for the internal D/A converters.
02	4-2	SMX	Chooses video source to be directed to the mixer imputs, V_1 and V_2.
02	1-0	MIXTFN	Used to alter the mixer transfer function.
Fill Color Registers			
03	7-0	REDVAL	Value for Red/C_R
04	7-0	GRNVAL	Value for Green/Y
05	7-0	BLEVAL	Value for Blue/C_B

Reg	Bit	Name	Function
Output Control Register			
06	7	AVPIPE	Sets pipeline latency of AV
06	6		Reserved
06	5	αLUTEN	αLUTEN power down enable
06	4	PASSON	Sets pixel activity subject to mixer transfer function.
06	3	A/BPASS	Selects A or B data in PASSON mode
06	2	MOUT	Bits M_{23-0} enable
06	1	MMSB	Inverts C_B, C_R MSBs
06	0	MFORMAT	Sets output data format
D/A Control Register			
07	7-6		Reserved
07	5	DACDLY	Selects SYNC and BLANK pipe delay
07	4	DACFMT	C_B/C_R translate from 2's complement to offset binary
07	3	SLEEP	D/A converters enable/ disable
07	2	SETUP	Sets IRE blanking levels
07	1	DOVLEN	D/A converter overlay palette enable/disable
07	0	DMAT	D/A converter input data YC_BC_R/RGB conversion
Identification (read-only)			
08	7-0	REVID	Chip revision ID
09	7-0	CHIPID	Chip type ID = 2F

Control Register Definitions

A-Channel Control Register (00)

7	6	5	4	3	2	1	0
AOVLEN	ADEC	AMAT	CLUT	AMSB	αGAIN	AFORMAT	

Reg	Bit	Name	Description
00	7	AOVLEN	When HIGH, the Overlay palette in the PDA pixel path is enabled and controlled by the OL_{3-0} inputs. When LOW, the PDA Overlay palette is disabled.
00	6	ADEC	When HIGH, this bit causes A-channel pixel data to be decimated from YC_BC_R444 to YC_BC_R422 format. When LOW, no decimation filtering takes place and the data is passed through.
00	5	AMAT	When HIGH, this bit causes A-channel pixel data to be converted from RGB to YC_BC_R format. When LOW, no conversion takes place and the data is passed through.
00	4	CLUT	When HIGH, the A-channel CLUT and Overlay Palette are enabled and addressed by pixel data. When LOW the CLUT and Palette are powered down and bypassed with address data connected to the outputs.
00	3	AMSB	When LOW,the MSBs of the C_B and C_R A-channel input positions (PDA_{15} and PDA_7) are not inverted. When HIGH, the MSBs of the C_B and C_R input positions are inverted
00	2	αGAIN	a-channel gain. LOW selects 9-bit unity gain. HIGH selects 8-bit unity gain.
00	1-0	AFORMAT	The FORMAT bits set up the A pixel data path to accommodate digital video in four different formats: 0 0 YC_BC_R444 0 1 YC_BC_R422 1 0 8-bit color index 1 1 24-bit RGB

Control Register Definitions (continued)

B-Channel Control Register (01)

7	6	5	4	3	2	1	0
Reserved	MSOURCE		BMAT	BINT	BMSB	BFORMAT	

Reg	Bit	Name	Description
01	7		Reserved.
01	6-5	MSOURCE	Source of pixels to be connected to port M_{23-0}. 0 0 Mixer Pixels 0 1 A pixels 1 0 B pixels 1 1 Reserved
01	4	BMAT	When HIGH, this bit causes B-channel pixel data to be converted from YC_BC_R to RGB format. When LOW, no conversion takes place and the data is passed through
01	4	BINT	When HIGH, this bit causes B-channel pixel data to be interpolated from YC_BC_R422 to YC_BC_R444 format. When LOW, no interpolation filtering takes place and the data is passed through.
01	3	BMSB	When LOW, the MSBs of the C_B and C_R B-channel input positions (PDB_{15} and PDB_7) are inverted. When HIGH, the MSBs of the C_B and C_R input positions are not inverted.
01	1-0	BFORMAT	B-channel pixel data format select bits. 0 0 YC_BC_R444 1 0 Reserved 0 1 YC_BC11 1 1 24-bit RGB

Control Register Definitions (continued)

Mixer Control Register (02)

7	6	5	4	3	2	1	0
MIXFMT	DSOURCE		SMX			MIXFTN	

Reg	Bit	Name	Description
02	7	MIXFMT	When LOW, the mixer is set for $YCB_CR_$ format. When HIGH, the mixer expects RGB format.
02	6-5	DSOURCE	The data source for the internal D/A converters is selected by two control bits. 0 0 Crosspoint Switch A-pixels 0 1 Crosspoint Switch B-pixels 1 0 Mixed pixels 1 1 Reserved
02	4-2	SMX	These three control bits determine which video source (A-pixels, B-pixels, fill color registers) is directed to the two mixer inputs, V_1 and V_2, through the ABF Crosspoint Mux: 0 0 0 A to V_1, B to V_2 0 0 1 A to V_1, F to V_2 0 1 0 B to V_1, A to V_2 0 1 1 B to V_1, F to V_2 1 0 0 F to V_1, A to V_2 1 0 1 F to V_1, B to V_2 1 1 0 Reserved 1 1 1 Enables SMX_{2-0} input pins for external source assignments
02	1-0	MIXTFN	These two bits are used to alter the mixer transfer function: 0 0 $(V_1 - V_2)\alpha + V_2$ 0 1 $(V_1)\ \alpha + V_2$ 1 0 $(V_1)\ \alpha$ 1 1 Reserved

Fill Color Registers (03–05)

Reg	Bit	Name	Description
03	7-0	REDVAL	Value for Red/C_R
04	7-0	GRNVAL	Value for Green/Y
05	7-0	BLUVAL	Value for Blue/C_B

Control Register Definitions (continued)

Output Control Register (06)

7	6	5	4	3	2	1	0
AVPIPE	Reserved	αLUTEN	PASSON	A/BPASS	MOUT	MMSB	MFORMAT

Reg	Bit	Name	Description
06	7	AVPIPE	When LOW the pipeline latency of AV, output on AVOUT is 14 CLK cycles. When HIGH, the pipeline latency is 12 CLK cycles.
06	6		Reserved.
06	5	αLUTEN	When LOW, the αLUTEN is powered down. Data from α_{8-0} bypasses the αLUT to controls the mixer directly. When HIGH, α_{7-0} addresses the αLUT which controls the mixer.
06	4	PASSON	When LOW, pixel activity during $\overline{\text{PASSEN}}$ is subject to the mixer transfer function. When HIGH, PDA or PDB data may be selected to pass through the mixer without modification. The PASSON feature allows Genlock or Decoder reference signals to be passed downstream for subsequent processing.
06	3	A/BPASS	Selects A or B data in PASSON mode. LOW allows all pixel activity from PDA_{23-0} during $\overline{\text{PASSEN}}$ = LOW to pass to M_{23-0}. HIGH allows all pixel activity from PDB_{23-0} during $\overline{\text{PASSEN}}$ = LOW to pass to M_{23-0}.
06	2	MOUT	Digital outputs M_{23-0} are enabled when this bit is HIGH. These outputs are in a high-impedance state when MOUT is LOW.
06	1	MMSB	When LOW,the MSBs of the C_B and C_R M_{23-0} output positions (M_{15} and M_7) are not inverted. When HIGH, the MSBs of the C_B and C_R output positions are inverted
06	0	MFORMAT	When LOW, 24-bit RGB or YC_BC_R444 output data formats are enabled. When HIGH, The multiplexer in the M_{23-0} path is enabled producing 16-bit YC_BC_R422.

D/A Control Register (07)

7	6	5	4	3	2	1	0
Reserved		DACDLY	DACFMT	SLEEP	SETUP	DOVLEN	DMAT

Reg	Bit	Name	Description
07	7-6		Reserved.
07	5	DACDLY	Selects $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$pipe delay. LOW = 15 clocks, HIGH = 2 clocks
07	4	DACFMT	Translates C_B/C_Rformat from 2's complement to C_B/C_R offset binary. LOW passes C_B/C_R unchanged. HIGH inverts C_B/C_R MSB.
07	3	SLEEP	D/A converters are enabled when HIGH. The D/A converters are powered-down when SLEEP is LOW.
07	2	SETUP	When LOW, 0 IRE blanking levels are present on the D/A converter outputsWhen HIGH, blanking levels are 7 . 5 IRE units.
07	1	DOVLEN	When HIGH, the Overlay palette in the D/A converter pixel path is enabled and controlled by the OL_{3-0} inputs. When LOW, the D/A Overlay palette is disabled
07	0	DMAT	When HIGH, D/A converter input data is converted from YC_BC_R to RGB format. When LOW, no conversion takes place and the data is passed through.

Control Register Definitions (continued)

Identification Registers (08-09)

Reg	Bit	Name	Description
08	7-0	REVID	Chip revision identification.
09	7-0	PARTID	Chip type identification = 2F.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Max	Unit
Power Supply Voltage	-0.5	+7.0	V
Input Voltage	-0.5	(V_{DD} + 0.5)	V
Digital Inputs			
Applied voltage [2]	-0.5	(V_{DD}+ 0.5)	V
Externally forced current [3, 4]	-20.0	20.0	mA
Digital Outputs			
Applied voltage [2]	-0.5	(V_{DD}+ 0. 5)	V
Externally forced current [3, 4]	-20.0	20.0	mA
Short Circuit Duration (Single output in HIGH state to GND)		1 second	
Analog Output Short Circuit Duration (Single output to GND)		infinite	
Temperature			
Operating, case	-60	+130	°C
Operating, Junction, Plastic package		+150	°C
Lead,soldering (10 seconds)		300	°C
Vapor phase soldering (1 minute)		+220	°C
Storage	-65	150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Min.	Nom	Max.	Units
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH				
	TTL Inputs, all but CLK, $\overline{CE}$	2.0		V_{DD}	V
	CLK, $\overline{CE}$	2.4		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW				
	TTL Inputs	GND		0.8	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
V_{REF}	External Reference Voltage		1.235		V
I_{REF}	D/A Converter Reference Current		1.8		mA
	(I_{REF} = V_{REF} / R_{REF}, sourced from R_{REF} pin)				
R_{REF}	Reference Resistor @ V_{REF} = Nom.		681		Ω
R_{OUT}	Total Output Load Resistance		37.5		Ω
T_A	Ambient Temperature, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current[1]	f_{CLK} = 25MHz, DAC, CLUT and αLUT enabled		300		mA
I_{DDQ}	Power Supply Current[1]	f_{CLK} = 0 DAC, CLUT and αLUT enabled		260		mA
I_{DAC}	DAC Supply Current	f_{CLK} = 25MHz		80	100	mA
I_{CLUT}	CLUT Supply Current			85	100	mA
$I_{\alpha LUT}$	αLUT Supply Current			30	45	mA
I_{DDSE}	Power Supply Current	Sleep Mode (D/A, CLUT, αLUT, and D/A overlay disabled)		5		mA
V_{RO}	Voltage Reference Output		1.1	1.2	1.3	V
I_{BR}	Input Bias Current, V_{REF}	V_{REF} = Nom	-100		40	µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = 4.0V	-5		5	µA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0.4V	-5		5	µA
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, Logic LOW	I_{OL} = Max			0.4	V
I_{OZH}	Hi-Z Leakage current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}	-5		5	µA
I_{OZL}	Hi-Z Leakage current, LOW	V_{DD} = Max, V_{IN} = GND	-5		5	µA
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		15		pF
C_O	Digital Output Capacitance	T_A = 25°C, f = 1MHz		15		pF
V_{OC}	Video Output Compliance Voltage		-0.4		2.0	V
R_{OUT}	Video Output Resistance			15		kΩ
C_{OUT}	Video Output Capacitance	I_{OUT} = 0 mA, f = 1 MHz		15	25	pF

Note:

1. Typical I_{DD} measured at V_{DD}=+5.0 Volts and T_A=25°C, Maximum I_{DD} measured at V_{DD}=+5.25 Volts and T_A=0°C.

Switching Characteristics

Parameter		Min.	Nom	Max.	Units
Microprocessor Interface					
t_{PWLCS}	$\overline{CS}$ Pulse Width, LOW	95			ns
t_{PWHCS}	$\overline{CS}$ Pulse Width, HIGH		4/f_{PXL}		ns
t_{SA}	Address Setup Time	0			ns
t_{HA}	Address Hold Time	4			ns
t_{SD}	Data Setup Time (write)	6			ns
t_{HD}	Data Hold Time (write)	3			ns
t_{DOZ}	Output Delay, $\overline{CS}$ to low-Z	16			ns
t_{DOM}	Output Delay, $\overline{CS}$ to Data Valid			110	ns
t_{HOM}	Output Hold Time, $\overline{CS}$ to hi-Z	7			ns
Pixel Interface					
f_{PXL}	Pixel Rate			40	Mpps
t_{CYPX}	Pixel Cycle Period	25			ns
t_{PWH}	CLK Pulse Width, HIGH	6			ns
t_{PWL}	CLK Pulse Width, LOW	6			ns
	For PDA, PDB, α, SMX. OL, $\overline{PASSEN}$, SIG0, AV inputs				
t_{SP}	Setup Time	6			ns
t_{HP}	Hold Time	2			ns
t_{HO}	Output Hold Time, CLK to data disabled	6			ns
t_{DO}	Output Delay, CLK to data valid			17	ns
Analog Outputs					
PIPES	Pipeline Delay		15		CLKs
t_R	D/A Output Current Risetime (10% - 90%) [2]		6		ns
t_F	D/A Output Current Falltime (10% - 90%) [2]		3		ns
t_{DOV}	Analog Output Delay [2]		20		ns
SKEW	D/A to D/A Output Skew			1	ns

Notes:

1. Timing reference points are at the 50% level.
2. Analog C_{LOAD} = 15pF.

System Performance Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
V_{VID}	Video Amplitude with 37.5 ohm load		0.7		Volt
V_{SYNC}	Sync Amplitude with 37.5 ohm load		0.3		Volt
RES	D/A Converter Resolution		8		Bits
E_{LI}	D/A Integral Linearity Error			0.75	LSB
E_{LD}	D/A Differential Linearity Error			0.75	LSB
E_G	D/A Gain Error			±8	% FS

Notes:

1. TTL input levels are 0.0 and 3.0 Volts, 10%-90% rise and fall times <3 ns.
2. Analog C_{LOAD} <10 pF, D_{7-0} load <40 pF.

Timing Diagrams

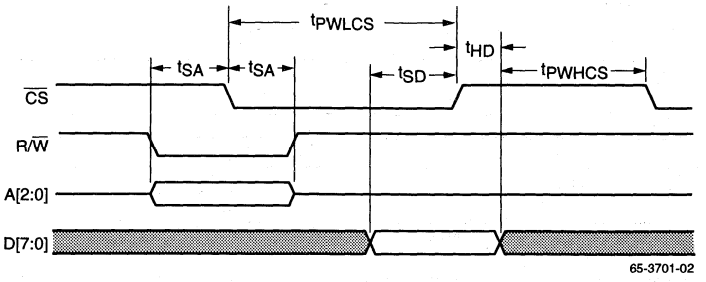


Figure 4. Microprocessor Port Write Timing

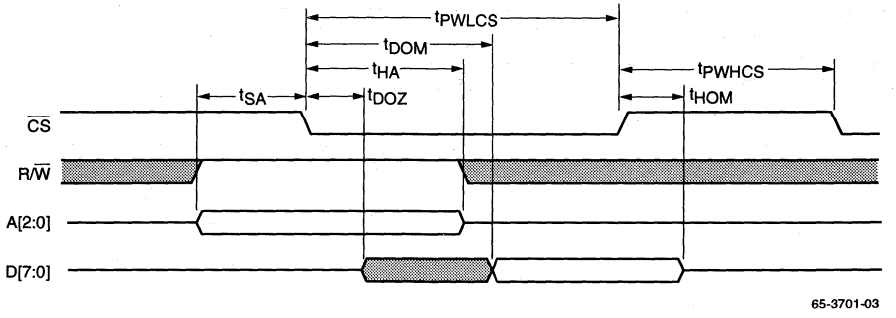


Figure 5. Microprocessor Port Read Timing

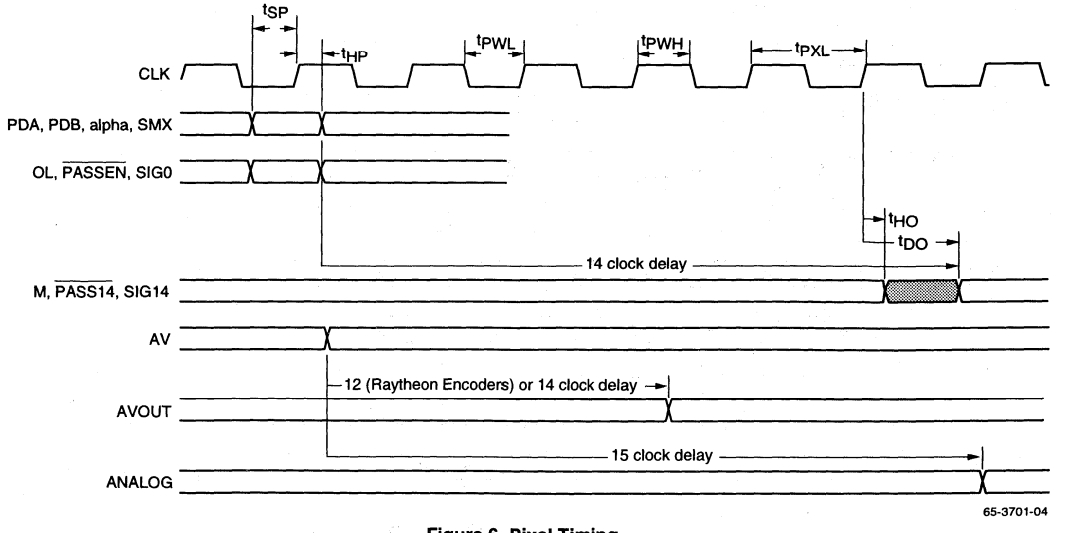


Figure 6. Pixel Timing

Timing Diagrams (continued)

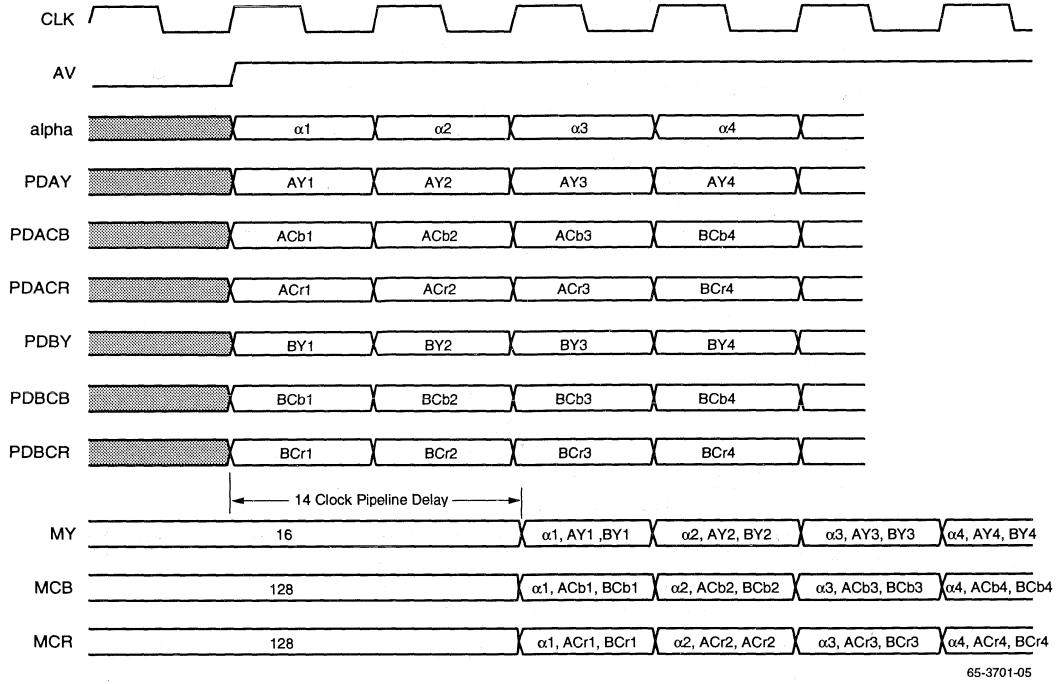


Figure 7. Pixel/Alpha Data Timing – 444/444 Mode

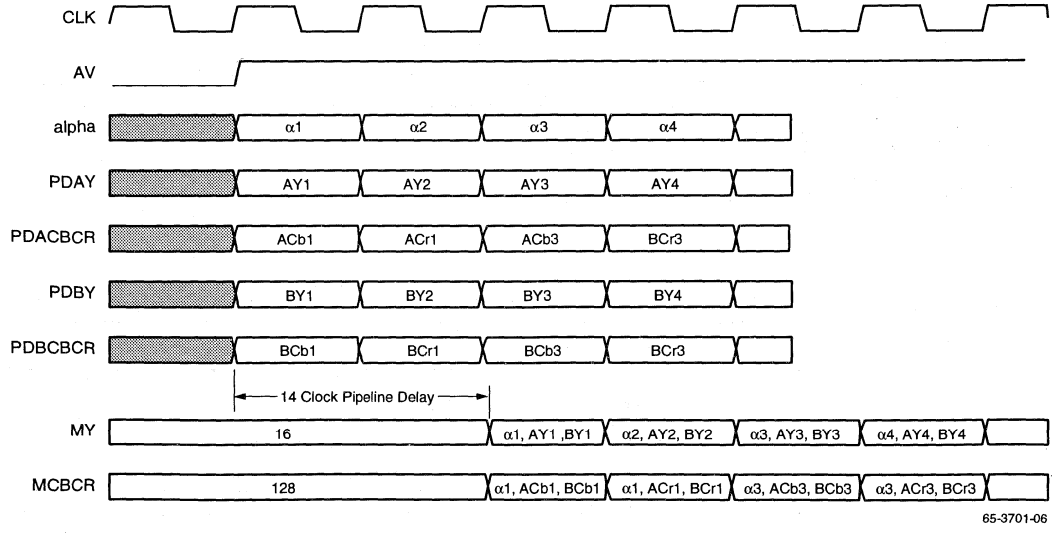


Figure 8. Pixel/Alpha Data Timing – 422/422 Mode

Timing Diagrams (continued)

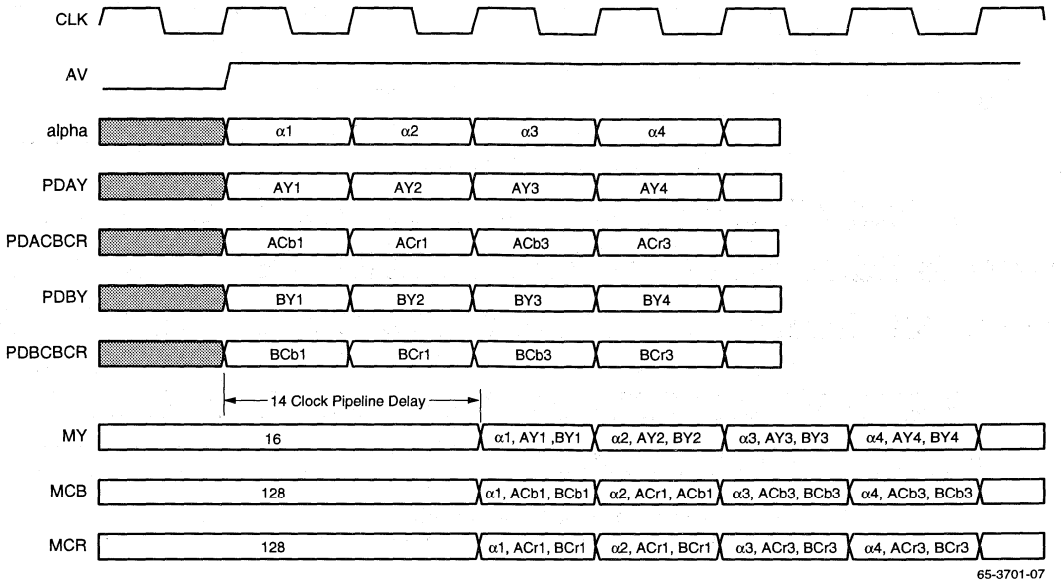


Figure 9. Pixel/Alpha Data Timing – 422/444 Mode

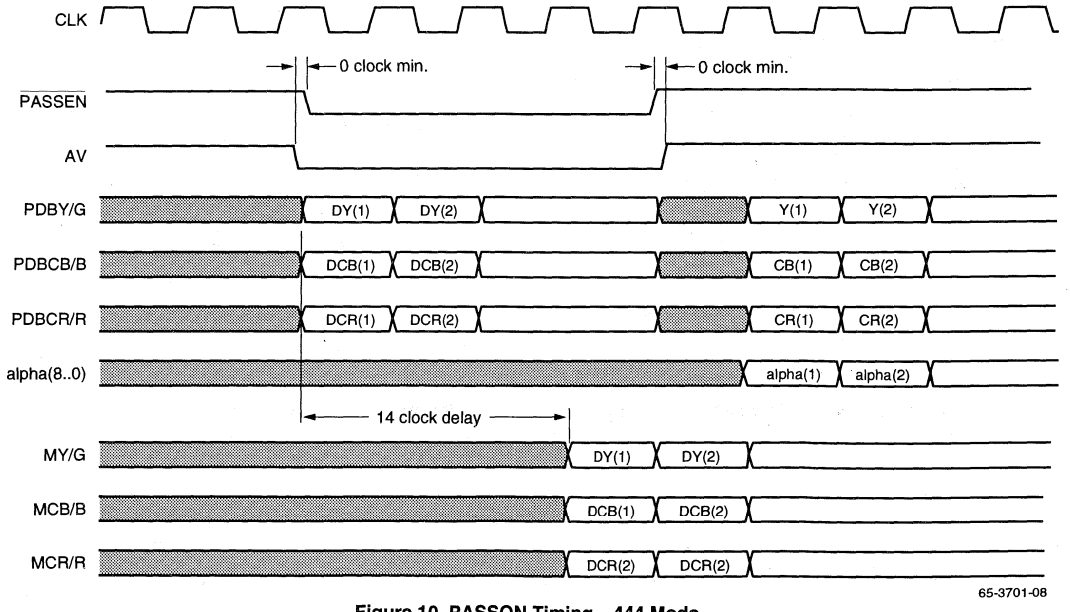


Figure 10. PASSON Timing – 444 Mode
(Control bits: PASSON = HIGH, A/BPASS = HIGH)

Timing Diagrams (continued)

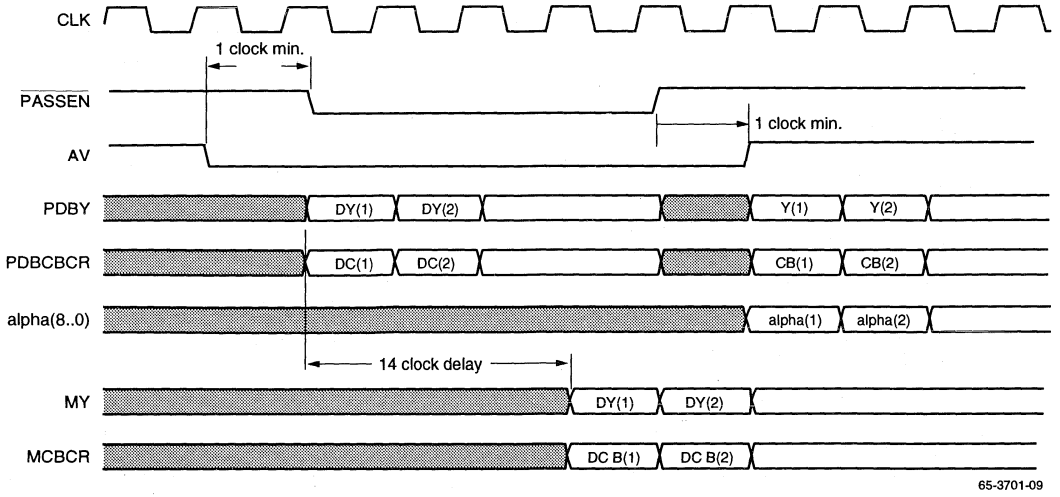


Figure 11. PASSON Timing – 422 mode
(Control bits: PASSON = HIGH, A/BPASS = HIGH)

Equivalent Circuits

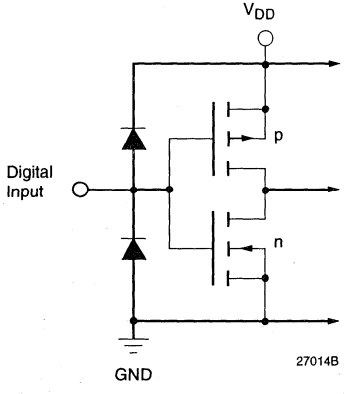


Figure 12. Equivalent Digital Input Circuit

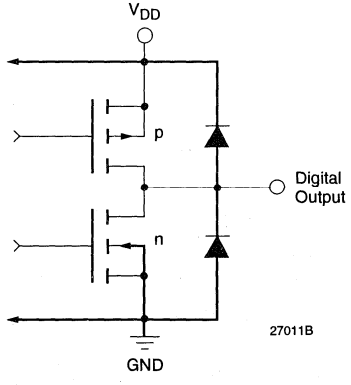


Figure 13. Equivalent Digital Output Circuit

Equivalent Circuits (continued)

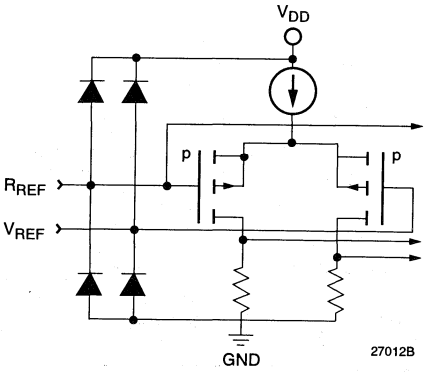


Figure 14. Equivalent Analog Input Circuit

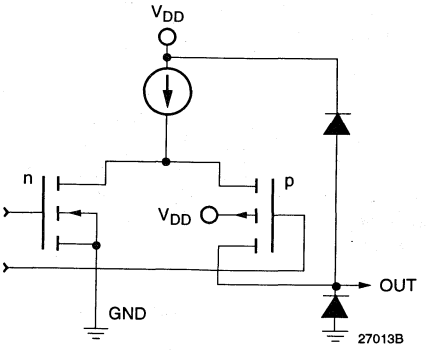


Figure 15. Equivalent Analog Output Circuit

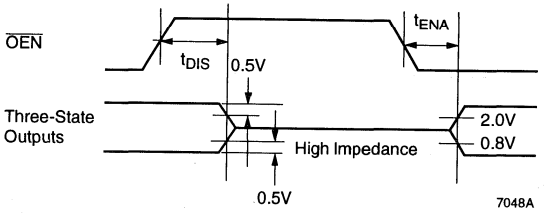


Figure 16. Threshold Levels for Three-State Measurement

Application Notes

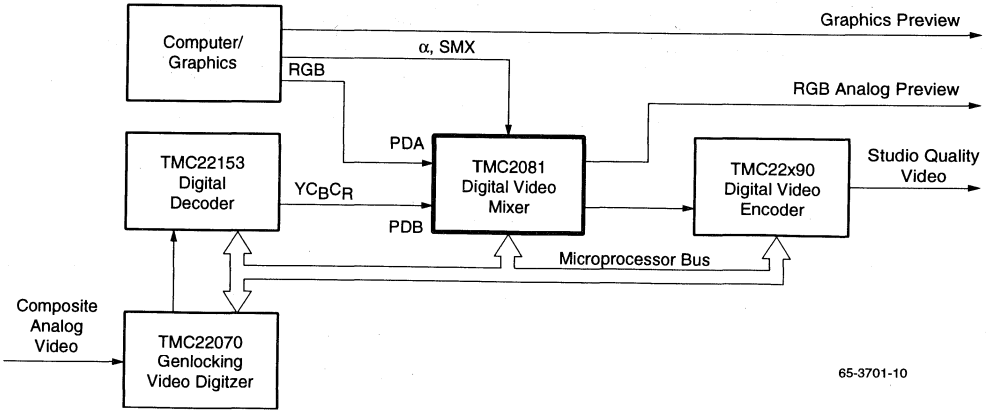


Figure 17. Mixing Video and Computer Graphics – Basic Multimedia System

Application Notes (continued)

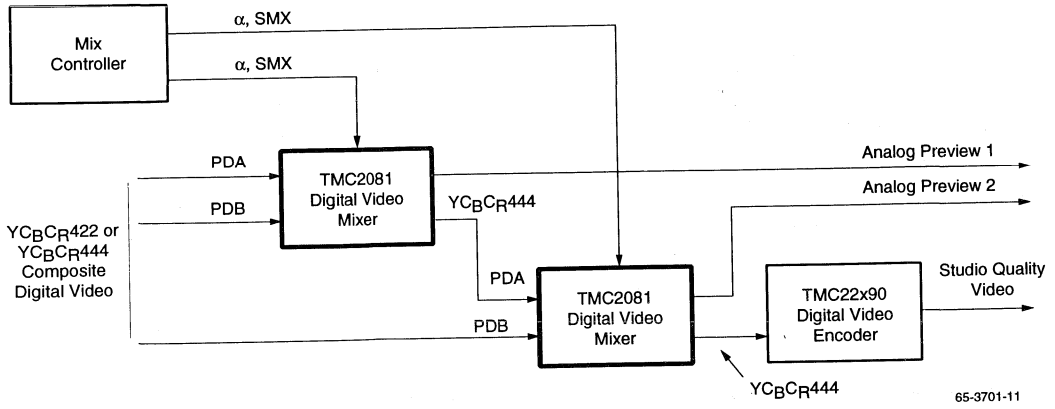


Figure 19. Multilevel Video Mixer with Special Effects

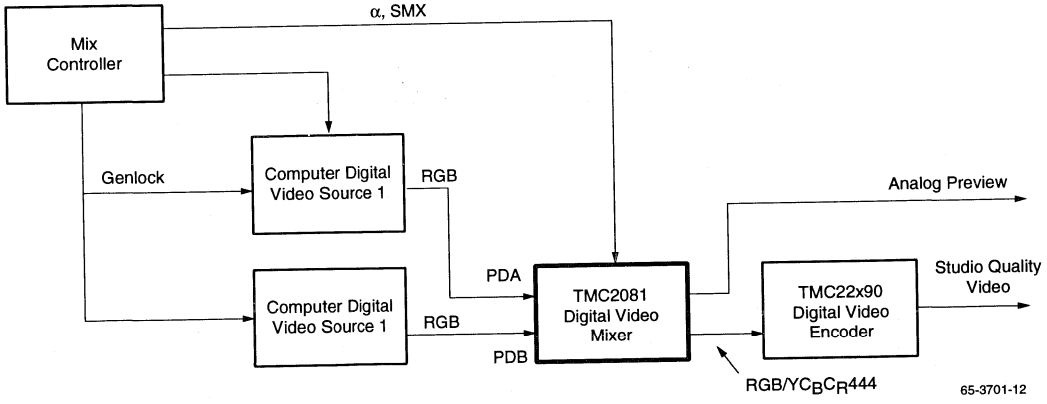


Figure 20. Mixing Two Computer Graphics Sources

Application Notes (continued)

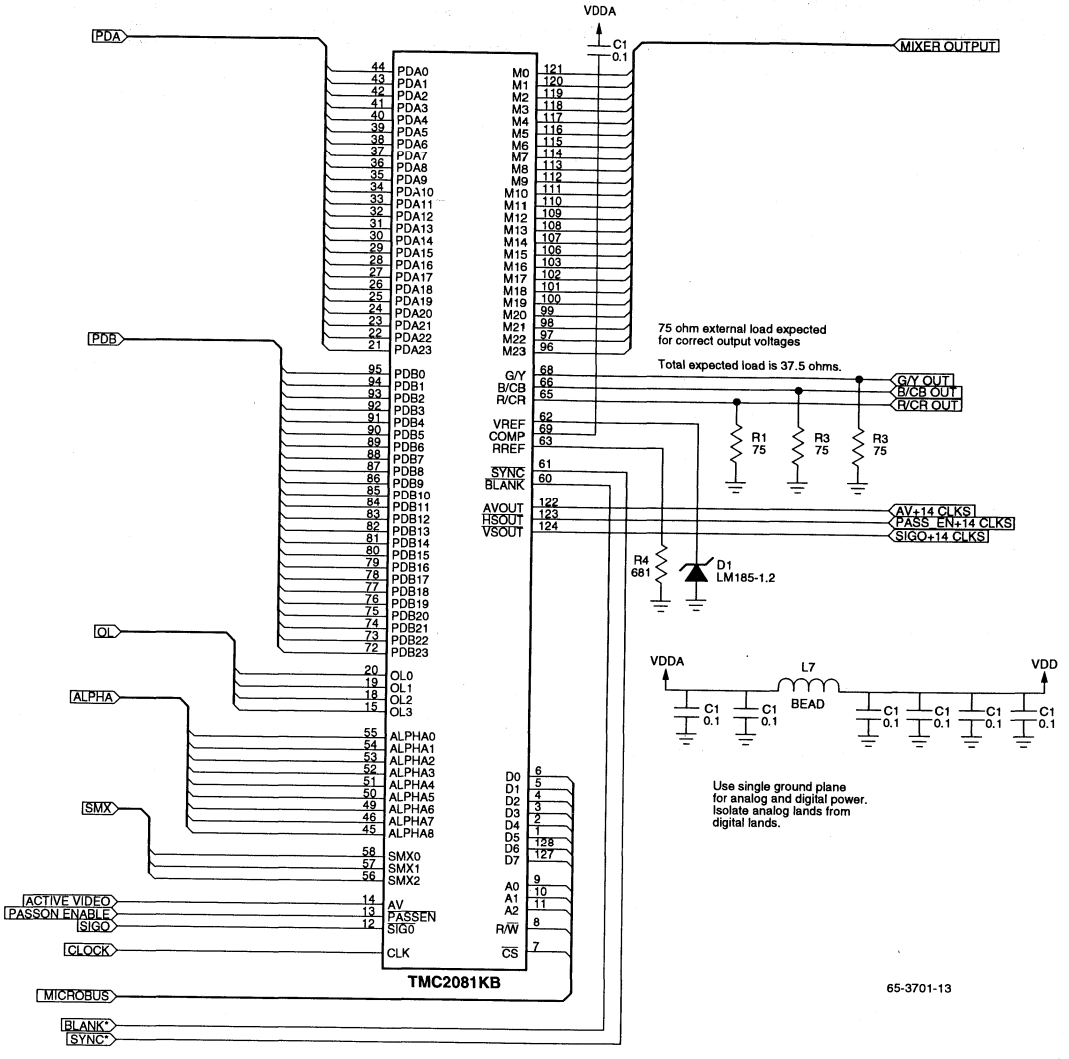


Figure 21. Recommended TMC2081 Connections

Related Products

- TMC22071 Genlocking Video Digitizer
- TMC22190/191 Digital Video Encoder
- TMC2242A/TMC2246A Digital Filter
- TMC2272A Color Space Converter

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2081KBC	T_A = 0°C to 70°C	Commercial	128-Lead MQFP	2081KBC

TMC2220/TMC2221

CMOS Programmable Digital Output Correlators

4 x 32 Bit, 20 MHz; 1 x 128 Bit 20 MHz

Features

- 20 MHz continuous correlation rate
- Fully programmable masking
- Two's complement or unsigned magnitude correlation score
- User-programmable reference load multiplexing
- Channel weighting and output formatting (TMC2220)
- Multi-bit, dual-channel or non-coherent (quadrature) correlation (TMC2220)
- Single +5V power supply
- Low power CMOS construction
- Three-state TTL compatible outputs
- TMC2220 available in 68-pin grid array and 69-pin plastic PGA packages
- TMC2221 available in a 28-pin CERDIP

Applications

- Signal detection
- Radar signature recognition
- Secure communications
- Robotics/automated assembly
- Automatic test equipment
- Electro-optical navigation
- Pattern and character recognition
- Assembly line inspection

Description

The TMC2220, 20 MHz TTL compatible CMOS correlator is composed of four separate 1 x 32 correlator modules. The correlation scores of the four modules are weighted, combined and output on two separate parallel, three-state ports.

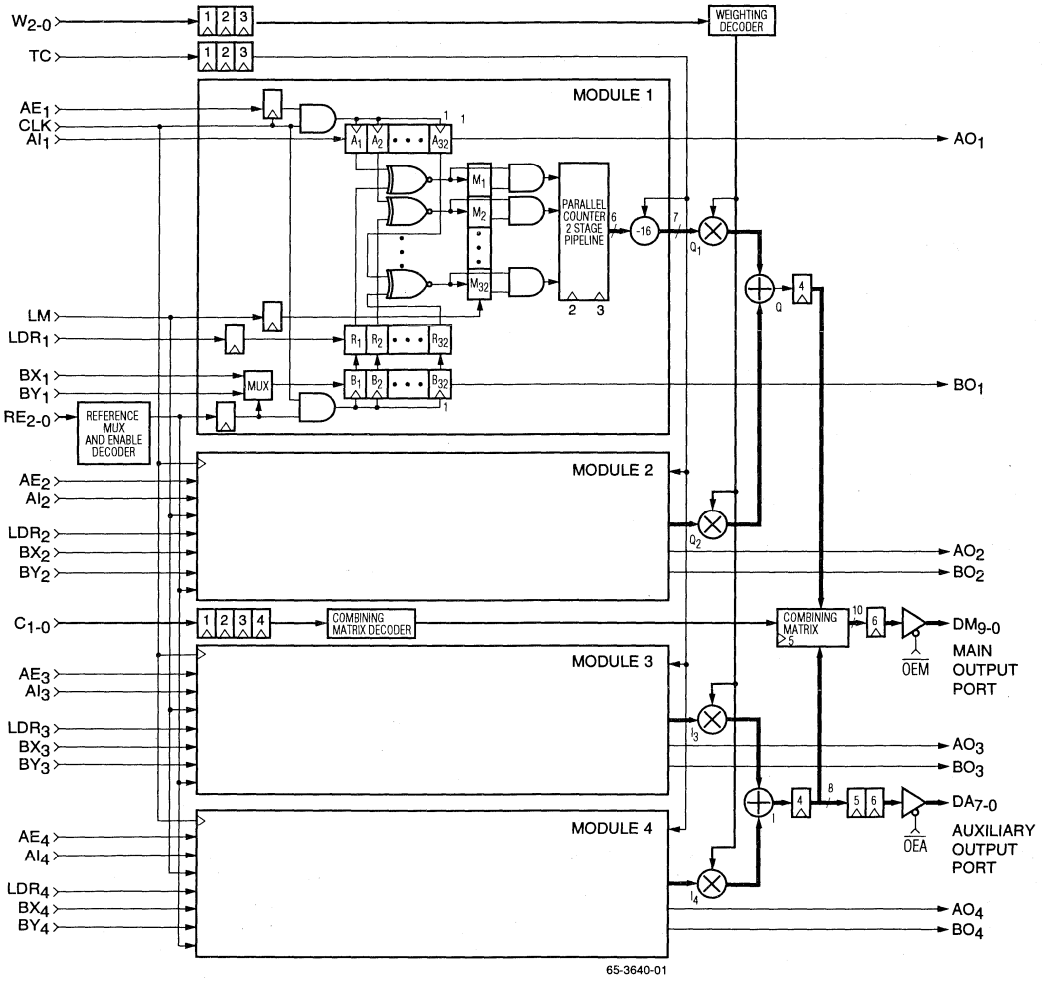
Each module contains a 32-bit serial data register, a 32-bit serial reference preload register, a 32-bit parallel reference latch and a 32-bit parallel mask latch. Correlation is performed by 32 exclusive-NOR (XNOR) gates. Each XNOR gate compares one (single bit) reference word. While correlation is being performed between the data and the present reference, the next reference pattern may be preloaded through one of two multiplexed input ports. Shorter sampling windows and bipolar correlation are also supported. Each module outputs a 6-bit binary correlation score. Either an unsigned (range 0 through 32) or bipolar (range -16 through +16) representation may be selected. The outputs of each pair of correlator modules is added, with user-selected weighting factors, producing intermediate correlation scores which can be combined or output directly to the main or auxilliary output ports.

Since the four modules can be cascaded serially or in parallel, the TMC2220 supports numerous single and dual channel applications involving 1, 2, or 4-bit wide data and window lengths up to 32, 64, 96 or 128 bits. Multiple devices can be combined to support large correlation operations.

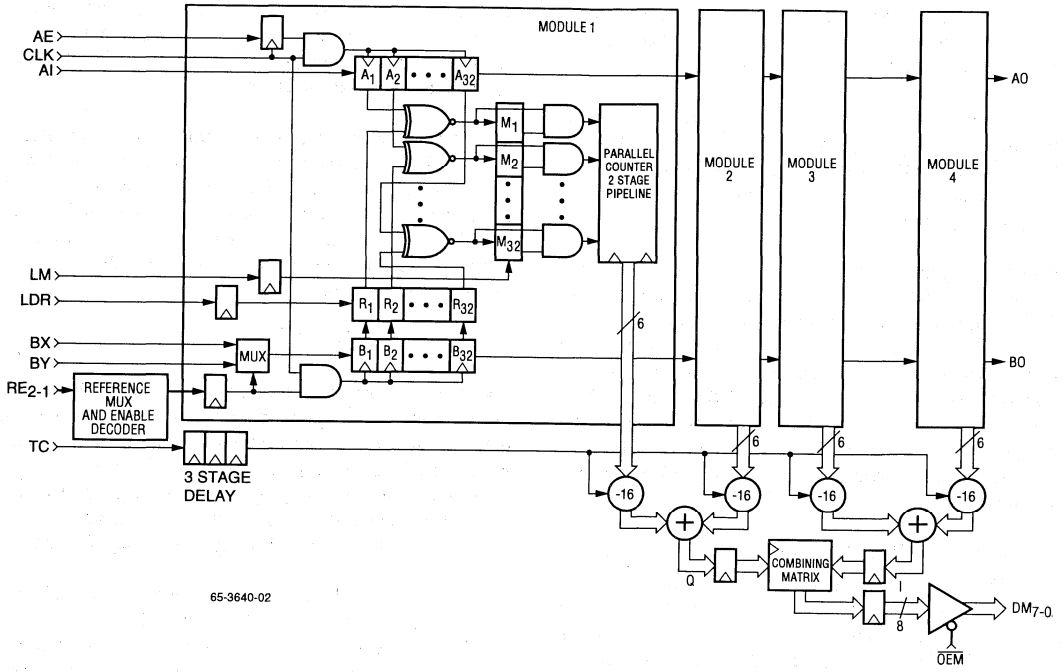
The TMC2221 combines the four 32-bit modules in series for a fixed channel configuration of 1-bit by 128. The reduced complexity and package size of the TMC2221 is ideal for applications requiring less versatility than the TMC2220. By making use of the mask function, any size single channel length of up to 128 bits is possible.

With the TMC2221, the reference word is serially loaded through the single two-input multiplexed reference port of the first correlator module. Although the configuration is fixed, the reference loading process and basic operation for each module is similar to that of the TMC2220. The outputs are summed with equal weighting, and the result is output through the single 8-bit output port. Unsigned magnitude or two's complement (bipolar) output score may be selected.

TMC2220 Block Diagram



TMC2221 Block Diagram



Functional Description

The TMC2220 consists of four independent 1 x 32 correlator channels with weighted correlation scores which are combined and output on the two output ports (main and auxiliary). By taking advantage of the instruction set and I/O structure, the TMC2220 can be adapted to a wide variety of applications.

The TMC2221 consists of the four 1 x 32 correlator modules cascaded internally for a single 1 x 128 correlator. The outputs of each module are given a unity weighting, summed and placed on the output port.

Correlator Channel Modules

Each of the four modules (i = 1 to 4) contains two 32-bit serial synchronous shift registers, A_i (data) and B_i (reference preload); two 32-bit parallel latches, R_i (reference) and M_i (mask); 32 exclusive-NOR gates; 32 AND gates; a 32-bit parallel binary counter with a 6-bit unsigned output and a defeatable half-scale (-16) subtracter with a 7-bit two's complement output.

Whenever a given A_i or B_i register is enabled, the next rising edge of the clock loads the value at the corresponding A_i or BX_i/BY_i input port into the first cell of the register, and shifts the contents of each cell to the next, overwriting the contents of the last cell. These serial-in, parallel-tapped registers form the first of six registers which account for the six internal delays. After an output buffer delay t_D, the new contents of the last cell of A_i and B_i become available at the outputs AO_i and BO_i respectively. These outputs are used for cascading multiple devices. In addition, the B_i input multiplexer selects which of two input ports, BX_i or BY_i, is to be used on that cycle.

The reference latch R_i tracks the contents of B_i when control LDR_i was HIGH on the previous cycle and holds when LDR_i was LOW. A HIGH on LDR_i transfers the contents of B_i in parallel into R_i on the next clock cycle where correlation takes place. When LDR_i is held HIGH, R_i is transparent, enabling direct correlation between A_i and B_i.

Each of the 32 outputs of R_i is correlated against the corresponding tap of A_i by an XNOR gate whose output is connected to both the masking AND gate and the masking latch M_i.

Each M_i tracks if LM was HIGH on the previous cycle and holds if LM was LOW. When LM is held HIGH, all M_i latches are transparent and the output of each XNOR gate is sent to both inputs of the corresponding AND gate to prevent

masking or disabling from occurring. A LOW on LM loads the next unmasked correlation pattern (from the XNOR gates) into each M_i. Wherever the latch holds a logic one, normal correlation is enabled; wherever it is a logic zero, correlation is masked by the AND gate.

A 32-bit parallel counter encodes the number of logic ones emerging from the AND gates as a 6-bit binary number between 0 and 32 (100000) The clock drives the two pipeline registers in the counter (the second and third registers in the six register pipeline).

The 6-bit unsigned binary output of each parallel counter then enters a half-scale subtracter where it passes unchanged if the pipelined control TC is LOW and is reduced by 16 if TC is HIGH. If TC is HIGH, the range of correlation scores becomes -16 through +16 where +16 denotes a perfect match between the contents of A_i and those of R_i with no masking. A score of -16 denotes that no unmasked data bit matches the corresponding reference bit (anti-correlation). The TC control is pipelined by 3 registers, such that it is aligned with new data entering the A_i or B_i register.

Weighing and Merging Circuitry

On the TMC2220, the 7-bit two's complement output of each correlator module (Q_1, Q_2, I_3, I_4) is multiplied by a factor of 0, 1, 2, 3, 4 or 5 according to controls W_{2-0}. The outputs of each pair of multipliers is then added and the results Q and I are loaded into the fourth pipeline register.

Following two additional pipeline delays from the fifth and sixth registers, correlation sum I is available on the TMC2220 at the 8-bit auxiliary output port, DA_{7-0}, if the buffer is enabled ($\overline{OEA}$ = LOW).

Under controls C_{1-0}, the TMC2220 combiner blends Q and I into a single final correlation score which is sent to the 10-bit main output port, DM_{9-0}, if $\overline{OEM}$ is LOW. The combiner pipeline register stage 5 and the main output register stage 6 are balanced by the auxiliary port double output register. In the simplest mode, the combiner outputs correlation sum Q permitting the TMC2220 to be used in two separate correlator channels. In this application, the combined results from modules 1 and 2 emerge through DM_{9-0} while the result-from modules 3 and 4 emerge through DA_{7-0}. In the three remaining modes, the output at the main port will reflect the correlations of all four modules.

In the second mode, the combiner outputs the unweighted sum, Q + I. In the third mode, it outputs the weighted sum, Q + 1/2, for single channel binary applications. In the fourth mode, the combiner extracts the absolute values of Q and I and adds the greater magnitude value to one half of the lesser value. This final mode is an approximation of the Pythagorean vector magnitude formula:

$$M = (X^2 + Y^2)^{1/2}$$

The TMC2220 contains a total of five pipeline registers plus the data and reference preload shift registers making the total delay six clock cycles. Instructions and data paths are pipelined so the instructions presented on a given clock cycle apply to the value entering registers A_i and B_i. Instructions RE, LM, LDR and AE, all of which enable registers or latches, must be set one cycle early (see timing diagram).

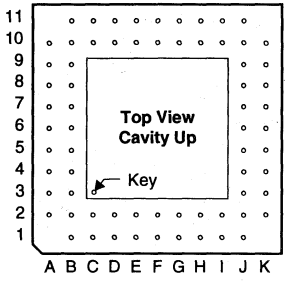
For the TMC2221, the correlation score of each module is passed unchanged (TC = LOW) or reduced by sixteen (TC = HIGH). Each module score is given a unity weighting then sent to the combining matrix where the four scores are added and output on the 8-bit data bus if $\overline{OEM}$ is LOW.

In magnitude mode (TC = LOW) and masking disabled, a perfect match between the data and reference will produce a correlation score of 128 (10000000_B) and correlation score of 0 shall indicate no matches (anti-correlation). In two's complement mode (TC = HIGH), perfect correlation will produce a score of 64 (01000000_B) and anti-correlation shall have an output of -64 (11000000_B). A total of five register delays plus the input register cause the result to be available on the sixth clock cycle after the loading of the input data.

TMC2220 Pin Assignments

68 Pin Grid Array – G8 Package

69 Pin Plastic Pin Grid Array – H8 Package[1]



Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
A2	GND	B9	LDR_3	F10	CLK	K4	W_2
A3	DA_2	B10	LDR_4	F11	GND	K5	W_0
A4	DA_4	B11	V_{DD}	G1	DM_8	K6	C_0
A5	DA_6	C1	DM_1	G2	DM_7	K7	LM
A6	BO_3	C2	DM_0	G10	BX_1	K8	AE_1
A7	BO_4	C10	BX_4	G11	GND	K9	AE_2
A8	V_{DD}	C11	AI_4	H1	BO_1	K10	RE_2
A9	AE_3	D1	DM_3	H2	DM_9	K11	AI_2
A10	AE_4	D2	DM_2	H10	AI_1	L2	V_{DD}
B1	DA_0	D10	AI_3	H11	BY_1	L3	$\overline{OEM}$
B2	DA_1	D11	BY_4	J1	BO_2	L4	W_1
B3	DA_3	E1	DM_5	J2	AO_1	L5	C_1
B4	DA_5	E2	DM_4	J10	BY_2	L6	TC
B5	DA_7	E10	BY_3	J11	BX_2	L7	LDR_1
B6	AO_3	E11	BX_3	K1	AO_1	L8	LDR_2
B7	AO_4	F1	DM_6	K2	GND	L9	RE_0
B8	$\overline{OEA}$	F2	V_{DD}	K3	GND	L10	RE_1

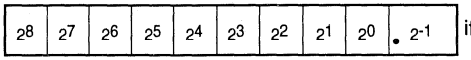
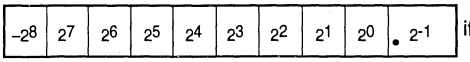
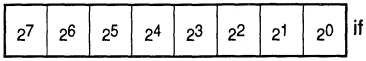
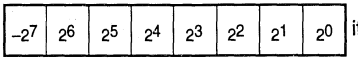
65-3640-14

Note:
1. Pin C3 is a mechanical orientation pin on the H8 package at manufacturer's option.

TMC2220 Pin Descriptions

Pin Name	Pin Number	Pin Function Description
Power		
V_{DD}	F2, L2, B11, A8	**Supply Voltage.** The TMC2220 operate from a single +5V power supply. All power and ground pins must be connected.
GND	K2, K3, G11, F11, A2	**Ground.** The TMC2220 operate from a single +5V power supply. All power and ground pins must be connected.
Inputs		
AI_{1-4}	H10, K11, D10, C11	**Data Input.** Each data input is a single-bit serial input to the A_i register of each correlator module.
BX_{1-4}	G10, J11, E11, C10	**Main Reference Preload.** The main, BX_i, reference preload inputs to the B_i register of each correlator module are selected by controls RE_{2-0}.
BY_{1-4}	H11, J10, E10, D11	**Alternate Reference Preload.** The alternate, BY_i, reference preload inputs to the B_i register of each correlator module are selected by controls RE_{2-0}.
Outputs		
AO_{1-4}	J2, K1, B6, B7	**Data Output.** Each cascade data output is a single-bit serial output from the A_i register of each correlator module.
BO_{1-4}	H1, J1, A6, A7	**Reference Preload Output.** Each cascade reference preload output is a single-bit serial output from the B_i register of each correlator module.

TMC2220 Pin Descriptions (continued)

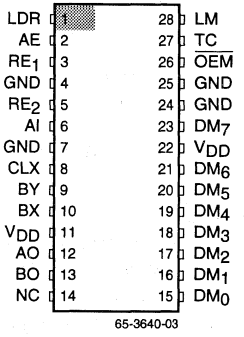
Pin Name	Pin Number	Pin Function Description
DM_{9-0}	H2, G1, G2, F1, E1, E2, D1, D2, C1, C2	**Main Port.** The 10-bit main correlation output is a combination of the four module output scores, Q_1, Q_2, I_3, I_4, which are dependent on the W_{2-0} weighted adder and C_{1-0} combining matrix controls. The main output port is enabled by $\overline{OEM}$. The TMC2220 10-bit output format is:  if TC is LOW  if TC is HIGH
DA_{7-0}	B5, A5, B4, A4, B3, A3, B2, B1	**Auxiliary Port.** The 8-bit auxiliary correlation output is the sum of two module output scores, I_3 and I_4, which are dependent on the W_{2-0} weighted adder controls. The auxiliary output port is enabled by $\overline{OEA}$. The 8-bit binary output format is:  if TC is LOW  if TC is HIGH
Clock		
CLK	F10	**Master Clock.** The clock for A_i data and B_i reference preload registers can be toggled at up to 20MHz. All registers are strobed on the rising edge of CLK and dependent on the registered enable controls, AE_i for the A_i registers, and RE_{2-0} for the B_i registers. The pipeline delay registers for the controls, W_{2-0}, C_{1-0}, and TC are also strobed on the rising edge of CLK.
Controls		
AE_{1-4}	K8, K9, A9, A10	**Register Clock Enable.** The clock enable for the four A_i data registers is a registered, active HIGH control. When AE_i is LOW on the previous cycle, no shifting of data occurs on A_i. AE_i is read on the rising edge of CLK, thus the shifting of data in A_i will occur on the next rising edge of CLK.
C_{1-0}	L5, K6	**Combining Matrix.** These pipelined instructions select the function to be executed by the combining matrix and output through the main output port, DM_{9-0}.
LDR_{1-4}	L7, L8, B9, B10	**Reference Load.** The Load Reference control copies the contents of register B_i into latch R_i for correlation. If LDR_i was LOW on the previous clock cycle, the present contents of the latch remain in R_i. If LDR_i was HIGH, R_i is transparent and the B_i are values used in the current correlation.
LM	K7	**Mask Load.** The Load Mask control allows the user to mask or select "no compare" bit positions in each channel. Inputs shifted into A_i and B_i produce a correlation pattern as the desired mask. Control LM must be HIGH on the previous cycle to track and LOW to store the pattern in the mask latches M_i If no masking is required, LM is kept HIGH, making M_i transparent.
$\overline{OEA}$	B8	**Auxilary Port Output Enable.** The asynchronous output enable for the auxiliary output port, DA_{7-0}, is an active LOW control. When $\overline{OEA}$ is HIGH, the output is in a high-impedance state.
$\overline{OEM}$	L3	**Main Port Output Enable.** The asynchronous output enable for the main output port, DM_{9-0}, is an active LOW control. When $\overline{OEM}$ is HIGH, the output is in a high-impedance state.

TMC2220 Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
RE_{2-0}	K10, L10, L9	**Reference Load Select.** The encoded clock enable and load selector controls determine the various combinations of BX_i and BY_i reference inputs that may be selected for the four reference preload registers B_i. The B_i register clocks may also be selectively enabled. Like LDR, LM and AE_i, this control is delayed by one clock cycle. See Table 1.
TC	L6	**Two's Complement.** The Two's Complement control forces the outputs of the four correlator modules to be unipolar (0 to 32) or bipolar (-16 to +16). When TC is LOW, the outputs of the correlator modules are passed unchanged to the weighting circuitry. When TC is HIGH, 16 is subtracted from each correlator output which is then interpreted as a two's complement value.
W_{2-0}	K4, L4, K5	**Module Weighing Factor.** The weighted adder controls determine the relative weightings of the four correlation module scores.

TMC2221 Pin Assignments

28 Pin CERDIP – B6 Package



TMC2221 Pin Descriptions

Pin Name	Pin Number	Pin Function Description
Power		
V_{DD}	11, 22	**Supply Voltage.** The TMC2221 operates from a single +5V power supply. All power and ground pins must be connected.
GND	4, 7, 24, 25	**Ground.** The TMC2221 operates from a single +5V power supply. All power and ground pins must be connected.
Inputs		
AI	6	**Data Input.** Each data input is a single-bit serial input to the A_i register of each correlator module.
BX	10	**Main Reference Preload.** The main, BX_i, reference preload inputs to the B_i register of each correlator module are selected by controls RE_{2-0}.
BY	9	**Alternate Reference Preload.** The alternate, BY_i, reference preload inputs to the B_i register of each correlator module are selected by controls RE_{2-0}.

TMC2221 Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
Outputs		
AO	12	**Data Output.** Each cascade data output is a single-bit serial output from the A_i register of each correlator module.
BO	13	**Reference Preload Output.** Each cascade reference preload output is a single-bit serial output from the B_i register of each correlator module.
DM_{7-0}	23, 21, 20, 19, 18, 17, 16, 15	**Main Port.** The TMC2221 has an 8-bit correlation output DM_{7-0} which always outputs the sum: $Q_1 + Q_2 + I_3 + I_4$ Where each term is either unsigned magnitude or magnitude minus 16 depending on the TC control. The TMC2221 8-bit output format is: DM_7 DM_0 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0 if TC is LOW -2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0 if TC is HIGH
Clock		
CLK	8	**Master Clock.** The clock for A_i data and B_i reference preload registers can be toggled at up to 20MHz. All registers are strobed on the rising edge of CLK and dependent on the registered enable controls, AE_i for the A_i registers, and RE_{2-1} for the B_i registers. The pipeline delay registers for the controls, W_{2-0} and TC are also strobed on the rising edge of CLK.
Controls		
AE	2	**Register Clock Enable.** The clock enable for the four A_i data registers is a registered, active HIGH control. When AE_i is LOW on the previous cycle, no shifting of data occurs on A_i. AE_i is read on the rising edge of CLK, thus the shifting of data in A_i will occur on the next rising edge of CLK.
LDR	1	**Reference Load.** The Load Reference control copies the contents of register B_i into latch R_i for correlation. If LDR_i was LOW on the previous clock cycle, the present contents of the latch remain in R_i. If LDR_i was HIGH, R_i is transparent and the B_i are values used in the current correlation.
LM	28	**Mask Load.** The Load Mask control allows the user to mask or select "no compare" bit positions in each channel. Inputs shifted into A_i and B_i produce a correlation pattern as the desired mask. Control LM must be HIGH on the previous cycle to track and LOW to store the pattern in the mask latches M_i If no masking is required, LM is kept HIGH, making M_i transparent.
$\overline{OEM}$	26	**Main Port Output Enable.** The asynchronous output enable for the main output port, DM_{7-0}, is an active LOW control. When OEM is HIGH, the output is in a high-impedance state.
RE_{2-1}	5, 3	**Reference Load Select.** The encoded clock enable and load selector controls select BX and BY reference input. Like LDR, LM and AE_i, this control is delayed by one clock cycle. See Table 1.
TC	27	**Two's Complement.** The Two's Complement control forces the outputs of the four correlator modules to be unipolar (0 to 32) or bipolar (-16 to +16). When TC is LOW, the outputs of the correlator modules are passed unchanged to the weighting circuitry. When TC is HIGH, 16 is subtracted from each correlator output which is then interpreted as a two's complement value.
No Connection		
NC	14	

Table 1. Reference Preload Register Input and Enable Operation

RE_i Controls	Selected Reference Port (TMC2220)				Selected Reference Port (TMC2221)
RE_{2-0}	1	2	3	4	
000	Dis	Dis	Dis	Dis	Dis
001	Dis	Dis	Dis	BX_4	Dis
010	Dis	Dis	BY_3	BX_4	BY
011	Dis	Dis	BY_3	BY_4	BY
100	BX_1	BX_2	BX_3	BX_4	BX
101	BY_1	BX_2	BX_3	BX_4	BX
110	BY_1	BX_2	BY_3	BX_4	BY
111	BY_1	BY_2	BY_3	BY_4	BY

Notes:
1. Dis = B_i register disabled (hold model).
2. LSB (RE_0) not used on the TMC2221.

Table 2. Module Weighting Factor Operation (TMC2220 Only)

W_i Controls	Internal Channel Configuration	
W_{2-0}	Q	I
000	$Q_1 + Q_2$	$I_3 + I_4$
001	$3Q_1 + Q_2$	$3I_3 + I_4$
010	$4Q_1 + Q_2$	$4I_3 + I_4$
011	Q_2	I_4
100	Q_1	I_3
101	$3Q_1 + 2Q_2$	$3I_3 + 2I_4$
110	$4Q_1 + 2Q_2$	$4I_3 + 2I_4$
111	$5Q_1 + 2Q_2$	$5I_3 + 2I_4$

Table 3. Combining Matrix Operation (TMC2220 Only)

C_i Controls C_{1-0}	Main Output Port Function DM_{9-0}
00	Q
01	Q + I/2
10	Q + I
11	Max (|Q|, |I|) + 1/2 Min (|Q|, |I|)[1]

Notes:
1. The larger magnitude value of Q or I plus one-half of the smaller magnitude value.
2. The TMC2221 always outputs the sum $Q_1 + Q_2 + I_3 + I_4$.

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Max	Unit
Supply	-0.5	7.0	V
Output Applied Voltage[2]	-0.5	V_{DD} + 0.5	V
Output Forced Current[3,4]	-0.5	V_{DD} + 0.5	V
Short Circuit Duration (single output in HIGH state to ground)		1	sec
Storage Temperature	-65	150	°C
Operating, case temperature	-60	130	°C
Junction Temperature		175	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			-2.0			-2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

DC Characteristics within Specified Operating Conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, $\overline{OEM}$, $\overline{OEA}$ = 5V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz, $\overline{OEM}$, $\overline{OEA}$ = 5V		70		80	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	-40			-40	µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+40		+40	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	-40		-40		µA

DC Characteristics within Specified Operating Conditions[1] (continued)

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+40		+40	µA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max		-150		-150	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:
1. Actual test conditions may vary from those shown, but guarantee operation as specified

AC Characteristics within Specified Operating Conditions

Parameter		Test Conditions	Temperature Range								Units
			Standard				Extended				
			-1				-1				
			Min	Max	Min	Max	Min	Max	Min	Max	
F_C	Clock (Correlation) Rate	V_{DD} = Min		20		17		20		17	MHz
t_{pWL}	Clock Pulse Width, LOW	V_{DD} = Min	25		30		25		30		ns
t_{pWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15		15		15		15		ns
t_S	Input Setup Time		15		15		17		17		ns
t_H	Input Hold Time		0		0		0		0		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		25		25		25		25	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF	3		3		3		3		ns
t_{ENA}	Three-State Output Enable Delay[1]	V_{DD} = Min. C_{LOAD} = 40pF		17		17		17		17	ns
t_{DIS}	Three-State Output Disable Delay[1]	V_{DD} = Min. C_{LOAD} = 40pF		22		22		22		22	ns

Note:
1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Sliding Correlation Timing

The TMC2220 and TMC2221 have a six register pipeline. There are registers for the input data and reference, parallel counter, weighting circuitry, combining matrix, and output. CLK is used to load all A_i, B_i and instruction pipeline registers. With the register controls enabled, a data or reference word is loaded into its respective A_i or B_i register on every rising edge of CLK. Data A_N enters register A_i on the rising edge of clock C_N. The reference latch is static if the previous LDR_i was LOW or tracks B_i if LDR_i was HIGH. If reference preload is not desired, holding control LDR_i HIGH makes latch R_i transparent and direct correlation between A_i and B_i occurs. Data is valid if present at the input for a setup time t_S before and a hold time t_H after the rising clock edge. Setup and hold time requirements also apply to instructions and controls, however, AE, LDR, LM and RE must be valid one cycle before taking effect.

Because of the six internal pipeline delays, the correlation score for a given set of A_i and B_i register contents appears at the output ports six clock cycles plus an output delay t_D later. When the main and auxiliary (TMC2220 only) output ports are enabled ($\overline{OEM}$ = $\overline{LOW}$ and $\overline{OEA}$ = LOW), the correlation score O_N of data window A_{N-31} through A_N is output after rising clock edge C_{N+5} (A_{N-127} through A_N on the TMC2221). Instructions TC, W, and C are registered and pipelined so that the instructions will be aligned with the data. The instructions I_N (see timing diagram) which are loaded on rising clock edge C_N apply to a correlation between data and reference words N-31 (N-127) through N. Masking is assumed to be preset (previous LM = LOW) or unused (previous LM = HIGH). The same timing applies if the reference is shifting and data is fixed.

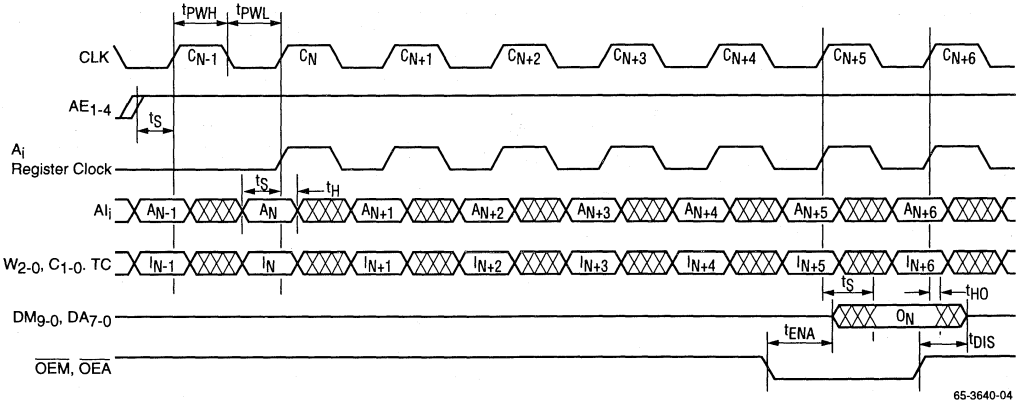


Figure 1. Sliding Correlation Timing

Reference Register Load Timing

The HIGH on LDR_i transfers the contents of B_i in parallel into R_i in the next clock period. R_i tracks B_i when control LDR_i is HIGH and holds when LDR_i is LOW. N rising edges of CLK are required to load N reference words into the reference preload register B_i. The rising edge of clock C_N loads reference word B_N so that B_i contains words B_{N-31} through B_N.

Figure 2 illustrates the LDR_i instruction timing to transfer reference window B_{N-31} through B_N into the reference latch. With this timing, correlation against the old reference pattern is preserved during the "LDR" clock cycle and that correlation against the new reference pattern B_{N-31} to B_N should commence immediately after the "LDR" clock cycle. The user must meet the normal input setup and hold time requirements and setup the instruction one clock cycle before the desired transfer.

A completely new reference can be loaded into latch R on every 32nd clock cycle. With the output ports enabled, the correlation score O_N (correlation between data A_{N-31} through A_N and reference B_{N-31} through B_N) is available an output delay t_D after the rising edge of clock C_{N+5} because of the six register pipeline.

Operation of the TMC2221 is similar to the operation described for the TMC2220 except the length of the reference word is 128 bits rather than 32. The reference register will therefore contain the pattern B_{N-127} through B_N, and correlation occurs between this reference and data A_{N-127} through A_N. A new reference word therefore requires 128 clock cycles to completely load the new value. With the output ports enabled, the correlation score O_N (correlation between data A_{N-127} through A_N and reference B_{N-127} through B_N) is available on output delay t_D after the rising edge of clock C_{N+5}.

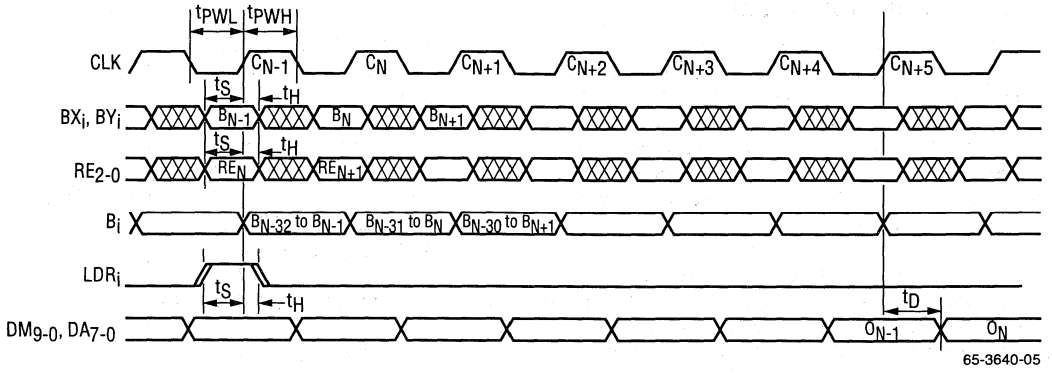


Figure 2. Reference Latch Load Timing

Mask Register Loading

Control LM latches a mask pattern into M_i which selectively disables word positions in each correlator module. Masking latch M_i tracks the XNOR output if, on the the previous clock cycle, LM was HIGH and holds if LM was LOW. Figure 3 illustrates the TMC2220 LM timing to latch a mask generated by the exclusive NOR of A_{N-31} through A_N with R_{N-31} through R_N. LM must be set HIGH t_S before the rising edge of clock C_{N-1} to load the mask for A_{N-31} thru A_N. LM must be set LOW before the next rising edge of C_N to ensure words N-31 to N remain latched as the mask pattern. A completely new mask may be loaded on every 32nd clock cycle. However, to permit time for data and reference loading, mask loading is generally limited to every 64th clock cycle. The first correlation score which reflects mask N is output t_D after the rising edge of clock cycle C_{N+6}.

Operation of the TMC2221 is similar that of the TMC2220 but requires 128 clock cycles to completely load a new mask pattern. To permit time to load new data and a new reference pattern once the mask is loaded, an additional 128 clock cycles is required. Therefore, mask loading is generally limited to every 256 clock cycles in the TMC2221. The mask pattern loaded will be the exclusive-NOR of A_{N-127} through A_N with R_{N-127} through R_N.

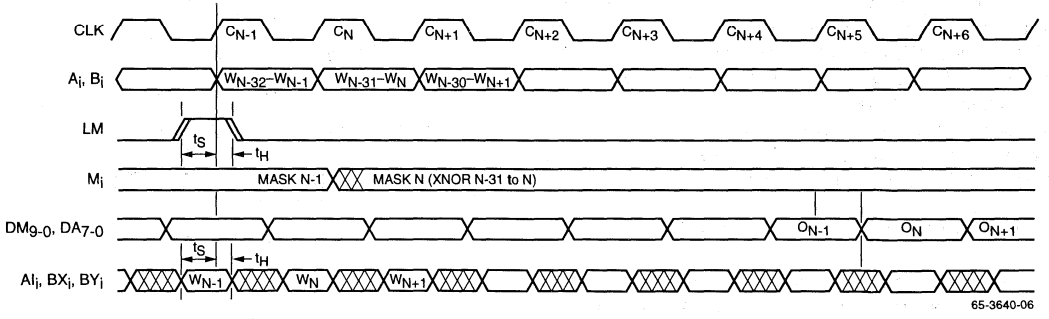


Figure 3. Masking Latch Load Timing

Applications Discussion

The TMC2220 architecture provides the flexibility for a number of configurations. The cascade outputs and the internal weighting and adder logic allow a single TMC2220 to be configured as four independent 32-bit correlators, independent 96-bit and 32-bit correlators, two independent 64-bit correlators, or as a single 128 x 1 correlator. The TMC2220 may also be cascaded serially or in parallel to increase the length or width of correlation.

To increase the correlation length in a single TMC2220 system, the cascade outputs of a module (AO_i, BO_i) can be connected to the inputs of the next module (AI_{i+1}, BI_{i+1}) When using this configuration, the input enables and load controls should be connected together. Figure 4 shows the configuration for a dual 64 x 1 correlation. In this application, the outputs of module 1 are connected to the inputs of module 2 and the outputs of module 3 are connected to the inputs of module 4. The weighting logic is set for 1:1 weighting and the combining logic is set to output $Q_1 + Q_2$ on the main output DM_{9-0}, and $I_3 + I_4$ on the auxiliary output DA_{7-0}

Figure 5 shows an example of multi-bit correlation with extended length. This example shows 4-bit correlation with a length of 64-bits. The outputs of the two TMC2220s must be externally added to obtain the 64-bit correlation score. The weighting and combining of the module correlation scores should be set as required by the application.

Figure 6 shows an example of 8-bit, two's complement correlation. Two TMC2220's are used in parallel and externally summed to obtain the properly weighted correlation score. To obtain a properly weighted correlation score, each bit of the output must be multiplied by an appropriate binary scaling factor. The 8-bit data input and reference are connected as shown. The weighting control of each TMC2220 is set for 4:1 weighting ($W_{2-0} = 010$). This multiplies the upper two bits of each TMC2220 by a factor of 4(Q_1, I_3). The next step is to multiply the 2nd and 4th bits (Q_2, I_4) by a factor of 2. This operation is accomplished by setting the combining logic to output the sum $Q + 1/2(C_{1-0} = 01)$. The final output of each TMC2220 will be equivalent to:

$$DM_{9-0} = (4 \times Q_1) + (2 \times I_3) + (1 \times Q_2) + (1/2 \times I_4)$$

Setting the weighting and combining controls as described will produce a correlation score with each bit properly weighted based on its 4-bit binary position. The final step is to multiply the correlation output of the most-significant TMC2220 (bits 7-4) by a factor of 16 then combine the outputs of the two TMC2220s. This is done using external adder circuitry. Multiplication is performed by simply shifting the output lines of the upper TMC2220 by four places at the input to the adder logic. The output of the summer, therefore, shall give the binary weighted correlation score of a quantized 8-bit input. The same circuit can be used with unsigned data if the inverter on the most-significant-bit of the reference input is omitted.

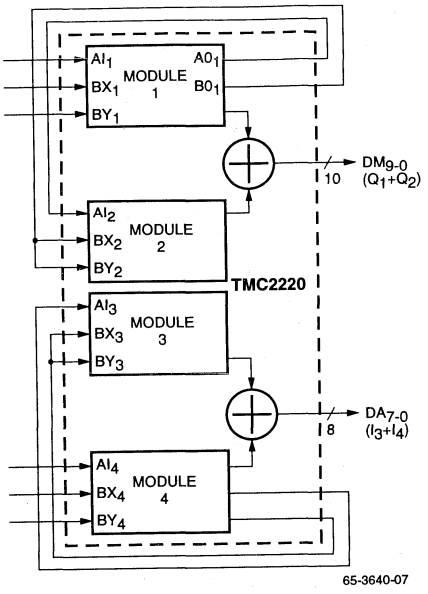


Figure 4. Dual 64 x 1 Configuration

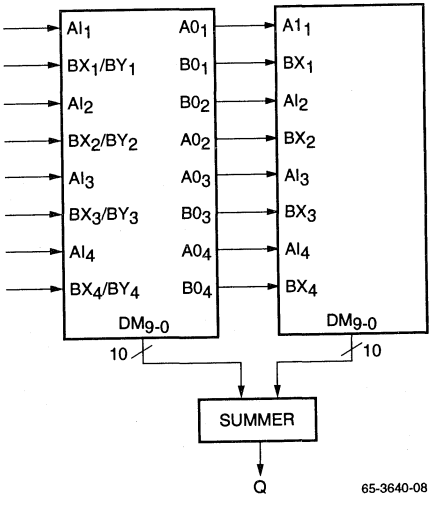


Figure 5. Cascading the TMC2220 for Extended-Length Correlation

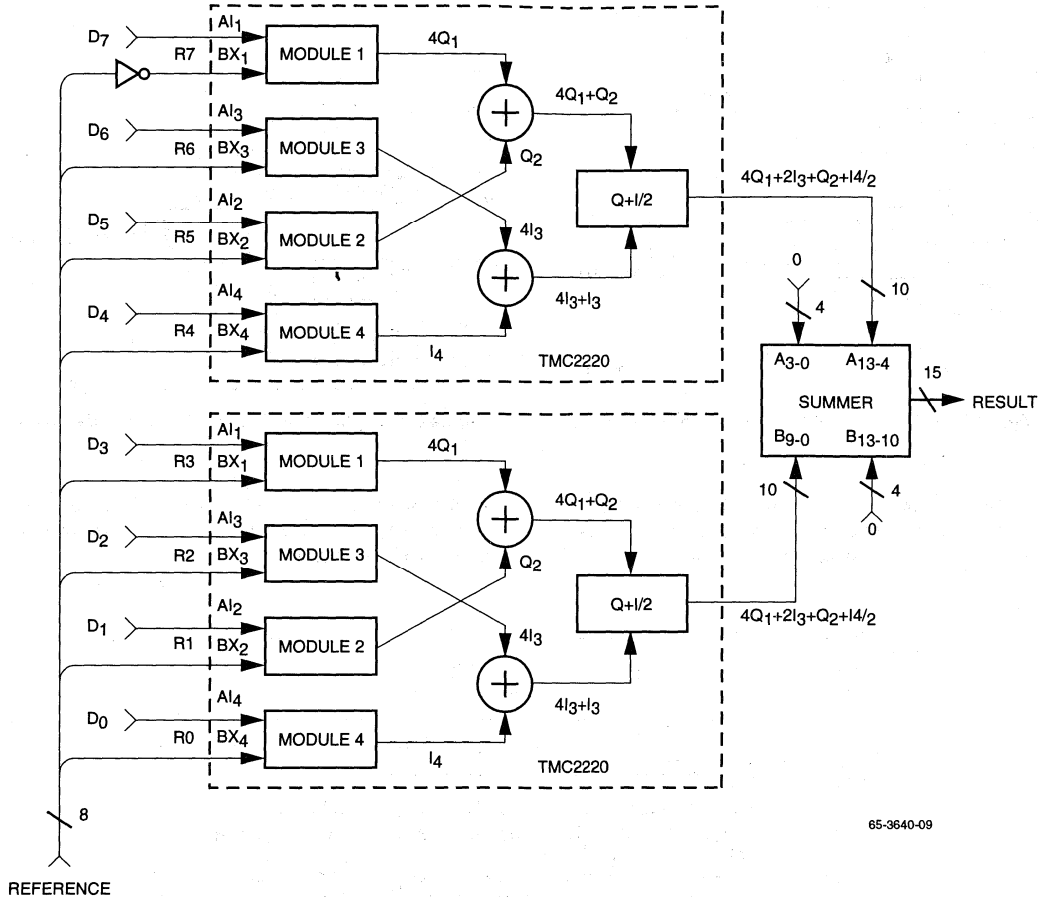


Figure 6. 8-Bit Correlation with the TMC2220

Figure 7 is an example of full complex correlation. In this example, separate real and imaginary terms are multiplied and summed internally to provide a real and imaginary result. This method preserves the phase information of the input. Inputs are connected as shown in the figure. The imaginary term in Im(D) x Im(R) is negated (inverted) for proper sign in the summation. The TMC2220 is set for 1:1 (Q_1 + Q_2, I_3 + I_4) weighting, two's complement mode, and the combining control is set to output Q on the main output and I on the auxiliary output. All 32 internal taps are used.

A simple example would be to find a sine wave in a demodulated data stream. The references would be set to:

Re(R) = Cos (ω t) and Im(R) = Sin I (ω t)

where, ω is the modulation frequency. Each term is set to 1 for positive and 0 for negative.

The data inputs are set to:

Re(D) = $data_{in}$ x Cos(ft) and Im(D) = $data_{in}$ x Sin (ft)

where, f is the mixer or carrier frequency.

Figure 8 is similar to full complex correlation, however, in this example the output is magnitude only. This application is used when the phase relationship is not required. The inputs are connected as in the previous example, however, rather than a full complex output, the outputs are combined internally to:

Max (|Q|, |I|) + 1/2 Min (|Q|, |I|)

(C_{1-0} = 11) to obtain the approximate magnitude output. Multiplying the output by 15/16 will reduce the error in the magnitude approximation.

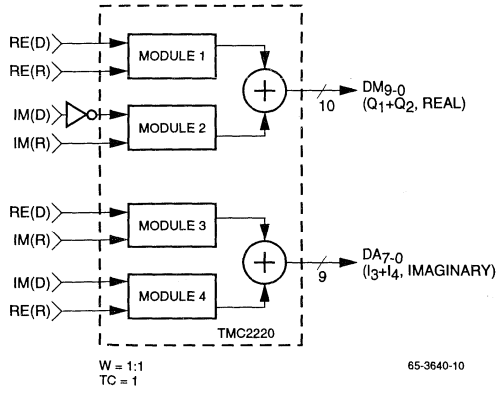


Figure 7. Full Complex Correlation with the TMC2220

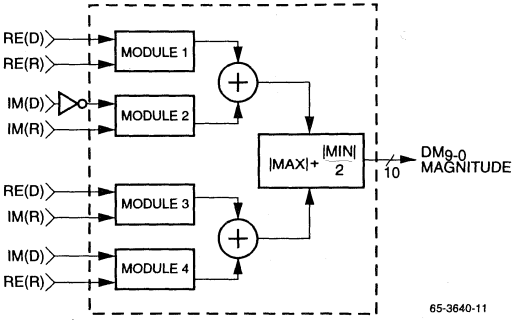


Figure 8. Complex Correlation with Magnitude Result

The TMC2221 can be cascaded to implement correlations of more than 128-bits. Typically all clocks, reference inputs and enables are connected together and the A and B outputs of preceding stages are connected to the respective inputs of subsequent stages. An external summer is required to generate the composite correlation score.

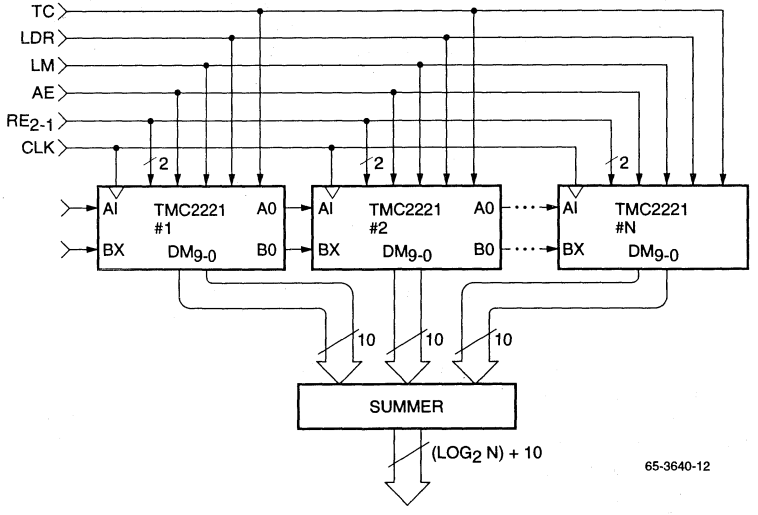


Figure 9. Cascading the TMC2221 for Extended - Length Correlation

The TMC2221 may also be used to compare multi-bit words with a single-bit reference. When this is done, the output of each TMC2221 must be appropriately weighted to the adder circuitry. The weighting reflects the relative importance of the different bit positions. Weighting can normally be accomplished by simple bit shifts at the input to the summer.

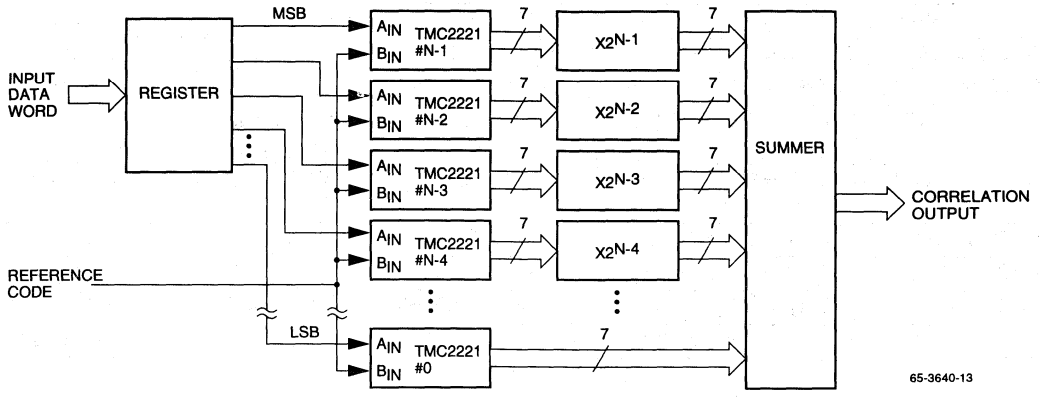


Figure 10. Multi-Bit x 1 Bit Correlation

Equivalent Circuits

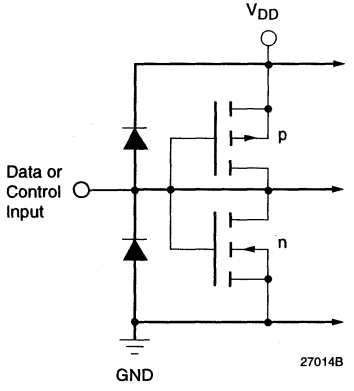


Figure 11. Equivalent Input Circuit

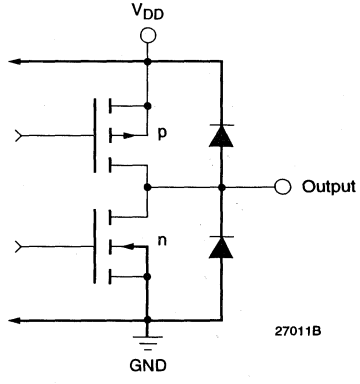


Figure 12. Equivalent Output Circuit

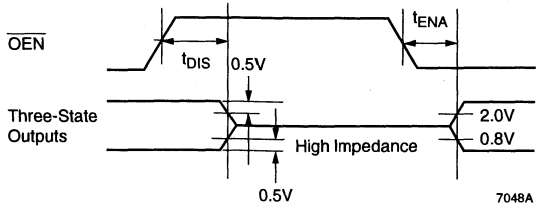


Figure 13. Threshold Levels for Three-State Measurements

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2220G8C	STD-T_A = 0°C to 70°C	Commercial, 17MHz	68 Pin Grid Array	2220G8C
TMC2220G8V	EXT-T_C = 55°C to 125°C	MIL-STD-883, 17MHz	68 Pin Grid Array	2220G8V
TMC2220G8C1	STD-T_A = 0°C to 70°C	Commercial, 20MHz	68 Pin Grid Array	2220G8C1
TMC2220G8V1	EXT-T_C = -55°C to 125°C	MIL-STD-883, 20MHz	68 Pin Grid Array	2220G8V1
TMC2220H8C	STD-T_A = 0°C to 70°C	Commercial, 17MHz	69 Pin Plastic Pin Grid Array	2220H8C
TMC2220H8C1	STD-T_A = 0°C to 70°C	Commercial, 20MHz	69 Pin Plastic Pin Grid Array	2220H8C1
TMC2221B6C	STD-T_A = 0°C to 70°C	Commercial, 17MHz	28 Pin CERDIP	2221B6C
TMC2221B6V	EXT-T_C = -55°C to 125°C	MIL-STD-883, 17MHz	28 Pin CERDIP	2221B6V
TMC2221B6C1	STD-T_A = 0°C to 70°C	Commercial, 20MHz	28 Pin CERDIP	2221B6C1
TMC2221B6V1	EXT-T_C = 55°C to 125°	MIL-STD-883, 20MHz	28 Pin CERDIP	2221B6V1

TMC2242A/TMC2242B

Digital Half-Band Interpolating/Decimating Filter

12-bit In/16-bit Out, 60 MHz

Features

- TMC2242A and TMC2242B are pin-compatible with TMC2242
- User selectable interpolate gain, -6 dB or 0 dB (2242B)
- 30, 40 and 60 MHz speed grades
- User selectable 2:1 decimation, 1:2 interpolation, and equal-rate filter modes
- Passband ripple < ±0.01 dB
- Stopband rejection 59.4 dB from 0.28 to 0.50 x f_S
- Cascading two TMC2242A or TMC2242B meets CCIR 601 low-pass filter requirement
- Dedicated 12-bit 2's complement input data port and 16-bit output data port with user-selectable rounding from 9 to 16 bits
- Two's complement or offset binary output format
- Built-in limiter prevents overflow
- Single +5 Volt power supply operation
- Small 44-Lead PLCC

Applications

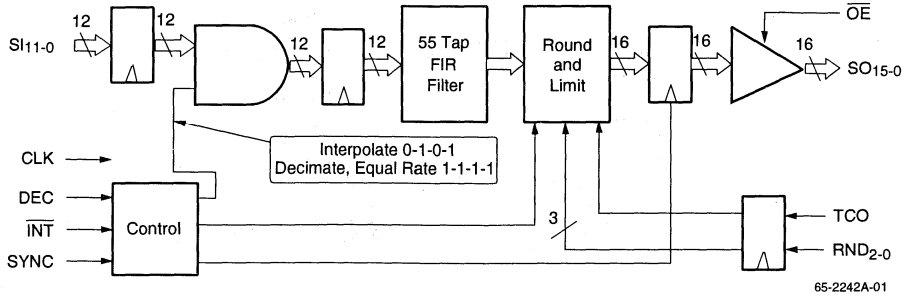
- Low-cost video filtering
- Chrominance bandwidth limiter
- Simple, inexpensive video D/A post-filters
- Reduced cost and complexity for A/D anti-aliasing filters
- High-performance digital low-pass filters
- Digital waveform reconstruction post-filtering
- Telecommunications
- Direct digital synthesis
- Radar

Description

The TMC2242A and TMC2242B are fixed-coefficient linear-phase half-band (low-pass) digital filters. They can be used to halve or double the sampling rate of a digital signal. When used as a decimating post-filter with a double-speed oversampling A/D converter, they greatly reduce the cost and complexity of anti-aliasing filters required ahead of the A/D converter. When used as an interpolating pre-filter with a double-speed oversampling D/A converter, the TMC2242A and TMC2242B significantly reduce the design complexity and production cost of reconstruction filters used on D/A outputs.

The TMC2242A and TMC2242B user selects the mode of operation (decimate, interpolate, or equal-rate) and rounding. The TMC2242A and TMC2242B accept 12-bit 2's complement data at up to 60 MHz and output saturated (overflow-protected) 2's complement or offset binary data rounded to from 9 to 16 bits. Within the speed grade I/O limit, the output sample rate may be 1/2, 1, or 2 times the input sample rate.

Block Diagram



Description (continued)

The filter response is flat to within ±0.01 dB from 0.00 to 0.22 x f_S, with stopband attenuation greater than 59.4 dB from 0.28 x f_S to the Nyquist frequency. The response is 6 dB down at 0.25 x f_S. Symmetric-coefficient filters such as the TMC2242A and TMC2242B have linear phase response. Full compliance with the CCIR-601 standard of 12 dB attenuation at 0.25 x f_S is achieved by cascading two parts.

The TMC2242A and TMC2242B are fabricated on an advanced submicron CMOS process. They are available in a 44-lead J-lead PLCC package. Performance is guaranteed from 0°C to 70°C.

Functional Description

The TMC2242A and TMC2242B implement a fixed-coefficient linear-phase Finite Impulse Response (FIR) filter of 55 effective taps, with special rate-matching input and output structures to facilitate 2:1 decimation and 1:2 interpolation. The faster of either the input or output registers will operate at the guaranteed maximum clock rate (speed grade). The total internal pipeline latency from the input of an impulse to the corresponding output peak (digital group delay) is 34 cycles; the 55-value output response begins after 7 clock cycles and ends after 61 cycles.

To perform interpolation, the chip slows the effective input register clock rate to half the output rate. It internally inserts zeroes between the incoming data samples to "pad" the input data rate to match the output rate.

To perform decimation, the chip sets the output register clock rate to half of the input rate. One output is then obtained for every two inputs.

For interpolation, the user should bring SYNC HIGH for at least one clock cycle, returning it LOW with the first desired input data value. When interpolating, the chip will then continue to accept a new data input on each alternate rising edge of the clock. When decimating, the chip will present one output value for every two clock cycles. The user may leave SYNC LOW or toggle it once per rising clock edge, with equivalent performance.

The output data format is two's complement if TCO is HIGH, inverted offset binary if LOW. The user can tailor the output data word width to his/her system requirements using the Rounding control. As shown in Table 4, the output is half-LSB rounded to the resolution selected by the value of $RND_{2\text{-}0}$. The asynchronous three-state output enable control simplifies connection to a data bus with other drivers.

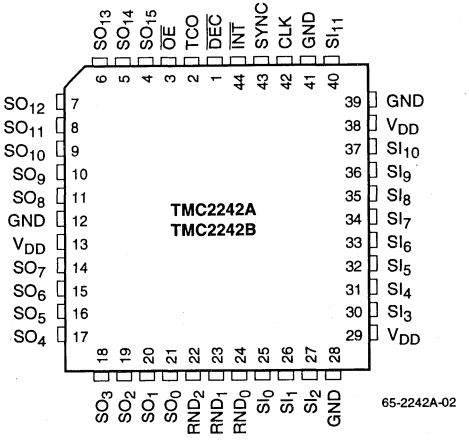
Table 1. Operating Modes

$\overline{DEC}$	$\overline{INT}$	TMC2242A	TMC2242B
0	0	Equal Rate	Interpolate (0 dB)
0	1	Decimate	Decimate
1	0	Interpolate (-6 dB)	Interpolate (-6 dB)[1]
1	1	Equal Rate	Equal Rate

Note:

1. With 15-bit overflow protection. All other modes on both parts limit to 16 bits.

Pin Assignments



65-2242A-02

Pin Descriptions

Pin Name	Pin Number	Pin Function Description
Timing Controls		
$\overline{INT}$	44	**Interpolate.** When $\overline{INT}$ is LOW and $\overline{DEC}$ is HIGH, the input data register runs at 1/2 the CLK rate and zeros are inserted in the data stream between valid input values, reducing gain by 6dB. The TMC2242A and TMC2242B interpolate and output results at the full CLK rate.
$\overline{DEC}$	1	**Decimate.** When $\overline{DEC}$ is LOW and $\overline{INT}$ is HIGH, the input data register runs at the full CLK rate. In this mode, the TMC2242A and TMC2242B decimate and output results at 1/2 the CLK rate. When $\overline{INT}$ = $\overline{DEC}$, the TMC2242A is in equal rate mode. When both $\overline{INT}$ and $\overline{DEC}$ are HIGH, the TMC2242B is likewise in equal-rate mode, but when both $\overline{INT}$ and $\overline{DEC}$ are LOW, the TMC2242B interpolates with unity gain. In equal-rate mode, the input and output sample rates equal the chip clock rate.
SYNC	43	**Synchronization.** Incoming data are synchronized by holding SYNC HIGH on CLK N–1 and LOW on CLK N when the first input data word is present on SI_{11-0}. If $\overline{DEC}$ = $\overline{INT}$=1 (equal rate mode), SYNC is inactive. SYNC may be held LOW until resynchronization is desired, or it may be toggled at 1/2 the CLK rate.
CLK	42	**Clock.** The TMC2242A and TMC2242B operate from a single master clock. All internal registers, except the output register in decimation mode, are strobed on the rising edge of CLK. All timing parameters are referenced to the rising edge of CLK.
Data Inputs		
SI_{11-0}	40, 37-30, 27-25	**Input Data Port.** A 12-bit 2's-complement input word is registered by the rising edge of CLK. In Interpolate Mode, SI_{11-0} is registered on every other CLK (synchronized by SYNC). SI_{11} is the MSB.
Data Outputs		
SO_{15-0}	4-11, 14-21	**Output Data Port.** A 16-bit 2's-complement output result is available after the rising edge of CLK. In Decimate Mode, SO_{15-0} is registered on every other CLK (synchronized by SYNC). SO_{15-0} is rounded according to the state of RND_{2-0}. SO_{15} is the MSB. The limiter circuitry ensures that for internal overflow, a valid full-scale output (7FFF or 8000) will be generated. With the TMC2242B in interpolate mode with -6dB gain, limits are 3FFF and C000 (TCO=1).
Output Controls		
$\overline{OE}$	3	**Output Enable.** When LOW, SO_{15-0} are enabled. When HIGH, SO_{15-0} are in a high-impedance state. $\overline{OE}$ is asynchronous with respect to CLK.
TCO	2	**Output Format.** When TCO is HIGH, output data are in signed 2's-complement format. When LOW, the output is inverted offset binary.
RND_{2-0}	22-24	**Rounding Select.** These inputs set the position of the effective LSB of the output result. Outputs below the rounding bit are zeroed (Table 4).
Power		
V_{DD}	13,29,38	**Supply Voltage.** +5 Volt power inputs. These should come from the same power source and be decoupled to GND.
GND	12,28,39,41	**Ground.** Ground inputs should be connected to the system digital ground plane.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Conditions	Min	Max	Units
Supply Voltage		-0.5	7.0	V
Input Voltage		-0.5	V_{DD} + 0.5	V
Output Applied Voltage[2]		-0.5	V_{DD} + 0.5	V
Externally Forced Current[3,4]		-3.0	+6.0	mA
Short Circuit Duration	Single output in HIGH state to ground		1	sec
Operating Temperature (Case)		-20	110	°C
Junction Temperature			140	°C
Lead Soldering Temperature	10 seconds		300	°C
Storage Temperature		-65	150	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Conditions	Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2242A, B			30	MHz
		TMC2242A-1,B-1			40	MHz
		TMC2242A-2,B-2			60	MHz
t_{PWH}	CLK pulse width, HIGH		6			ns
t_{PWL}	CLK pulse width, LOW		6			ns
t_S	Input Data Set-up Time		6			ns
t_H	Input Data Hold Time		1			ns
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Total Power Supply Current	V_{DD} = Max, C_{LOAD}=25pF, f_{CLK}=Max				
		TMC2242A,B			150	mA
		TMC2242A-1,B-1			195	mA
		TMC2242A-2,B-2			290	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = HIGH, f_{CLK}=Max				
		TMC2242A,B			120	mA
		TMC2242A-1,B-1			155	mA
		TMC2242A-2,B-2			230	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OZH}	Leakage Current, HIGH	$\overline{OE}$ = HIGH, V_{OUT} = V_{DD}			±10	µA
I_{OZL}	Leakage Current, LOW	$\overline{OE}$ = HIGH, V_{OUT} = 0 V			±10	µA
I_{OS}	Short-Circuit Current	V_{DD} = Max, Output = HIGH, one pin to ground, one second duration max.	-20		-80	mA
V_{OH}	Output Voltage, HIGH	SO15-0, I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	SO15-0, I_{OL} = Max			0.4	V

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			15	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	2.5			ns
t_{ENA}	Output Enable Time	C_{LOAD} = 0 pF			12	ns
t_{DIS}	Output Disable Time	C_{LOAD} = 0 pF			12	ns

Table 2. Impulse Response

Hex	Decimal Equivalent	
FFF2	-0.000875473	start & end
0000	0.0	
0017	0.001390457	
0000	0.0	
FFDB	-0.002265930	
0000	0.0	
0039	0.3501892	
0000	0.0	
FFA8	-0.006366836	
0000	0.0	
007D	0.007621765	
0000	0.0	
FF51	-0.01071167	
0000	0.0	
00F3	0.01483154	
0000	0.0	
FEB5	-0.02018738	
0000	0.0	
01CA	0.02796364	
0000	0.0	
FD79	-0.03949928	
0000	0.0	
03CD	0.05937767	
0000	0.0	
F95E	-0.1036148	
0000	0.0	
145B	0.3180542	
2010	0.5009766	center

Input = 0, 0, 0, ..., 0, 400h, 0, ..., 0, 0, 0
$\overline{INT}$ = $\overline{DEC}$ = TCO = 1

Table 3. Step Response

Input	$\overline{INT}$=1 $\overline{DEC}$=1 TCO=0	$\overline{INT}$=1 $\overline{DEC}$=1 TCO=1	$\overline{INT}$=0 $\overline{DEC}$=1 TCO=1	$\overline{INT}$=1 $\overline{DEC}$=0 TCO=1	
400	xx	xx	xx	xx	
400	xx	xx	xx	xx	
...	...	...	...	...	
400	3FE7	4018	2008	4018	DC Gain
400	3FE7	4018	2010	4018	
000	3FE7	4018	2008	4018	
...	...	...	...	...	
000	3B90	446F	245F	446F	Max Ringing
000	3B90	446F	2010	446F	
000	4FEB	3014	1004	1004	
000	6FFB	1004	0000	1004	
000	8456	FBA9	FBA9	FBA9	Min Ringing
...	...	...	...	...	
000	7FFF	0000	0000	0000	Steady State

Table 4a. Input Data Format

-2^0	2^{-1}	2^{-2}	...	2^{-10}	2^{-11}

Table 4b. Output Data Formats and Bit Weighting for TCO = 1

Interpolation Mode (TMC2242A and TMC2242B when $\overline{INT}$ = 0 and $\overline{DEC}$ = 1)

-2^{1}	2^{0}	2^{-1}	...	2^{6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}

Decimation, Equal Rate Modes (and TMC2242B in unity gain interpolate mode with $\overline{INT}$ = $\overline{DEC}$ = 0)

-2^{0}	2^{-1}	2^{-2}	...	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Rounded LSBs as a function of RND_{2-0}

												RND_{2-0}
SO_{15}	SO_{14}	SO_{13}	...	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2	SO_1	SO_{0r}	000
SO_{15}	SO_{14}	SO_{13}	...	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2	SO_{1r}	0	001
SO_{15}	SO_{14}	SO_{13}	...	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_{2r}	0	0	010
SO_{15}	SO_{14}	SO_{13}	...	SO_8	SO_7	SO_6	SO_5	SO_4	SO_{3r}	0	0	0	011
SO_{15}	SO_{14}	SO_{13}	...	SO_8	SO_7	SO_6	SO_5	SO_{4r}	0	0	0	0	100
SO_{15}	SO_{14}	SO_{13}	...	SO_8	SO_7	SO_6	SO_{5r}	0	0	0	0	0	101
SO_{15}	SO_{14}	SO_{13}	...	SO_8	SO_7	SO_{6r}	0	0	0	0	0	0	110
SO_{15}	SO_{14}	SO_{13}	...	SO_8	SO_{7r}	0	0	0	0	0	0	0	111

Notes:

1. A leading minus sign denotes the two's complement sign bit.
2. When TCO=0, the most significant bit of the output is positive instead of negative.
3. In all operating modes except $\overline{INT}$ = 0 and $\overline{DEC}$ = 1, the gain is approximately unity. When $\overline{INT}$ = 0 and $\overline{DEC}$ = 1, the output gain is -6 dB.
4. The "r" indicates that the trailing significant output bit has been rounded to the nearest 1/2 LSB. (Internally, the chip adds 1 to the next lower bit, to allow the user to obtain a properly rounded output)

Table 5. TMC2242A Steady-State Output Values and Limiter Triggers (L) versus Input Data

	$\overline{INT}$ = 1 or $\overline{DEC}$ = 0		$\overline{INT}$ = 0 and $\overline{DEC}$ = 1		
Input	TCO = 0	TCO = 1	TCO = 0	TCO = 1	Interpretation
7FF	0000 (L)	7FFF (L)	3FF7 / 3FE7	4008 / 4018	+ full-scale
400	3FE7	4018	5FF7 / 5FEF	2008 / 2010	+1/2 scale
001	7FEF	0010	7FF7	0008	+1 LSB
000	7FFF	0000	7FFF	0000	Zero
FFF	800F	FFF0	8007	FFF8	-1 LSB
C00	C017	BFE8	A007 / A00F	DFF8 / DFF0	-1/2 scale
801	FFFF (L)	8000 (L)	C007 / C017	BFF8 / BFE8	- full-scale

Table 6. TMC2242B Steady-State Output Values and Limiter Triggers (L) versus Input Data

Interpolation Modes

Input	$\overline{INT}$ = 0 and $\overline{DEC}$ = 0		$\overline{INT}$ = 0 and $\overline{DEC}$ = 1		Interpretation
	TCO = 0	TCO = 1	TCO = 0	TCO = 1	
7FF	0000 (L)	7FFF (L)	4000 (L)	3FFF (L)	+ full-scale
400	3FEF / 3FDF	4010 / 4020	5FF7 / 5FEF	2008 / 2010	+1/2 scale
001	7FEF	0010	7FF7	0008	+1 LSB
000	7FFF	0000	7FFF	0000	Zero
FFF	800F	FFF0	8007	FFF8	-1 LSB
C00	C00F / C01F	BFF0 / BFE0	A007 / A00F	DFF8 / DFF0	-1/2 scale
801	FFFF	8000 (L)	BFFF	C000 (L)	- full-scale

Decimation and Equal-Rate Modes

Input	$\overline{INT}$ = 1 and $\overline{DEC}$ = 0		$\overline{INT}$ = 1 and $\overline{DEC}$ = 1		Interpretation
	TCO = 0	TCO = 1	TCO = 0	TCO = 1	
7FF	0000 (L)	7FFF (L)	0000 (L)	7FFF (L)	+ full-scale
400	3FE7	4018	3FE7	4018	+1/2 scale
001	7FEF	0010	7FEF	0010	+1 LSB
000	7FFF	0000	7FFF	0000	Zero
FFF	800F	FFF0	800F	FFF0	-1 LSB
C00	C017	BFE8	C017	BFE8	-1/2 scale
801	FFFF (L)	8000 (L)	FFFF (L)	8000 (L)	- full-scale

Performance Curves

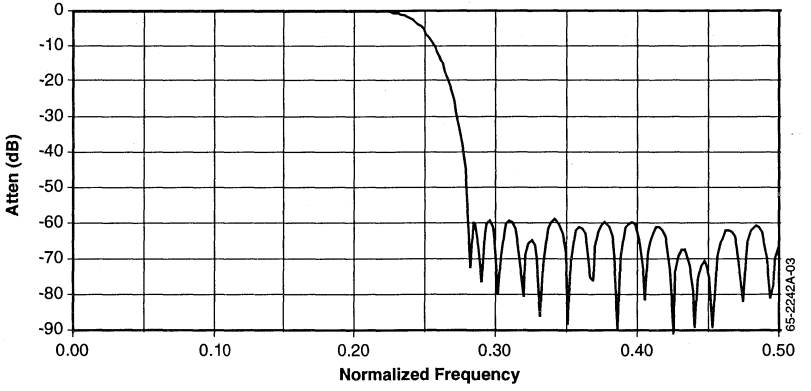


Figure 1. Frequency Response

Performance Curves (continued)

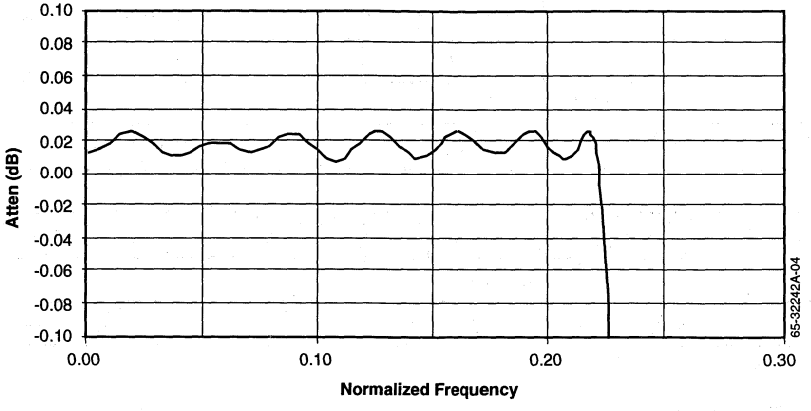


Figure 2. Passband Ripple Response

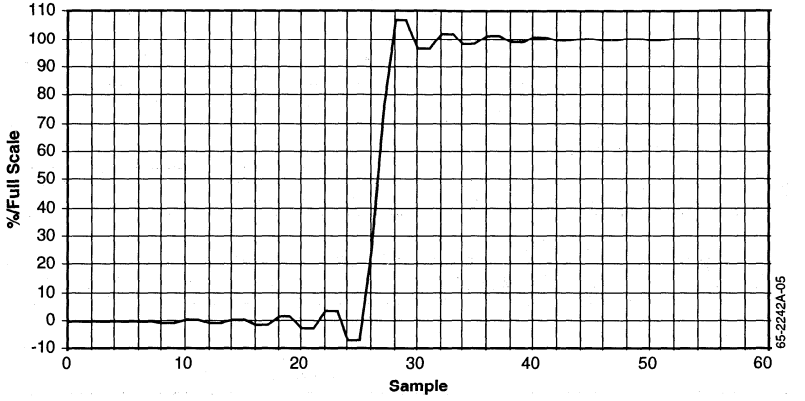


Figure 3. Step Response

Equivalent Circuits

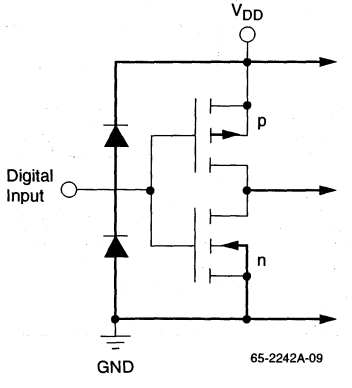


Figure 7. Equivalent Digital Input Circuit

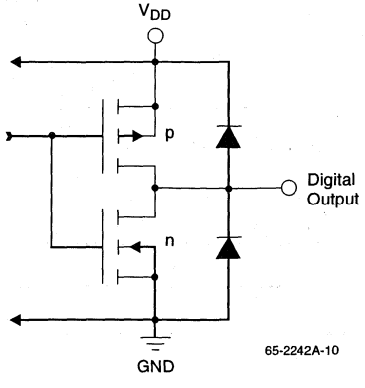
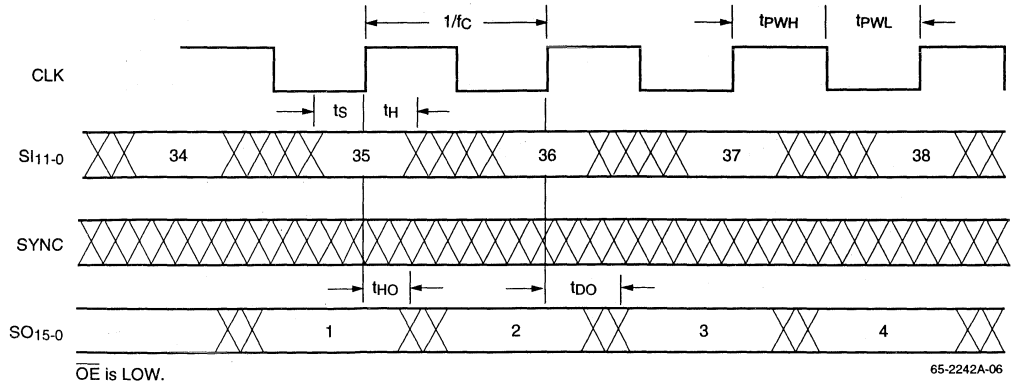


Figure 8. Equivalent Digital Output Circuit

Timing Diagrams



Note: Values at SO_{15-0} are impulse response centers (peaks) corresponding to same-numbered inputs.

Figure 4. Equal Rate Mode

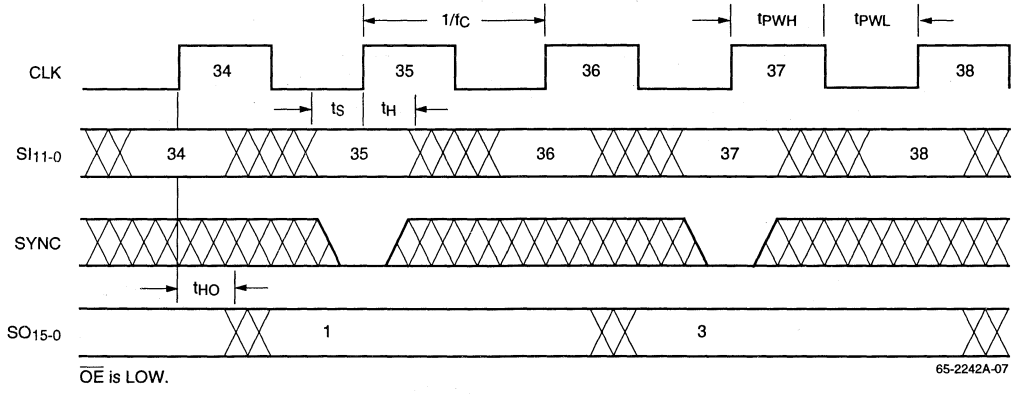


Figure 5. Decimate Mode

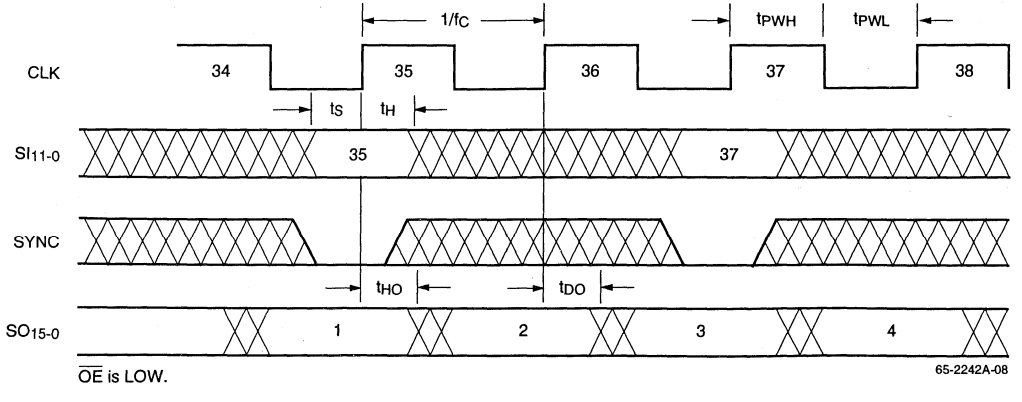


Figure 6. Interpolate Mode

Timing Diagrams (continued)

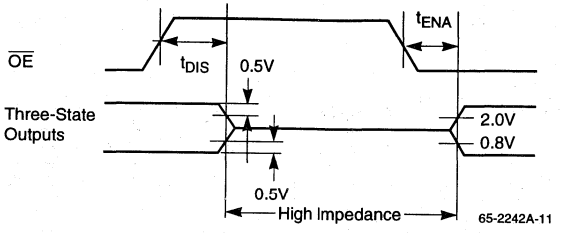


Figure 9. Threshold Levels for Three State Measurements

Applications Discussion

The TMC2242A and TMC2242B are well-suited for filtering digitized composite NTSC or PAL video. In Figure 10, the TMC1175A 8-bit video A/D converter outputs, D_{7-0}, are connected to the TMC2242B inputs, SI_{11-4}, respectively (grounding SI_{3-0}). The RND_{2-0} controls are set to 111 for a 9-bit rounded decimated output on SO_{15-7}.

In Figure 11, the TMC2242B drives a fast D/A converter to reconstruct analog composite video. The TMC3003 10-bit digital-to-analog converter inputs, D_{9-0} are connected to the TMC2242B outputs SO_{15-6}, respectively. The TMC2242B RND_{2-0} controls are set to 110 for rounded 10-bit interpolation operation.

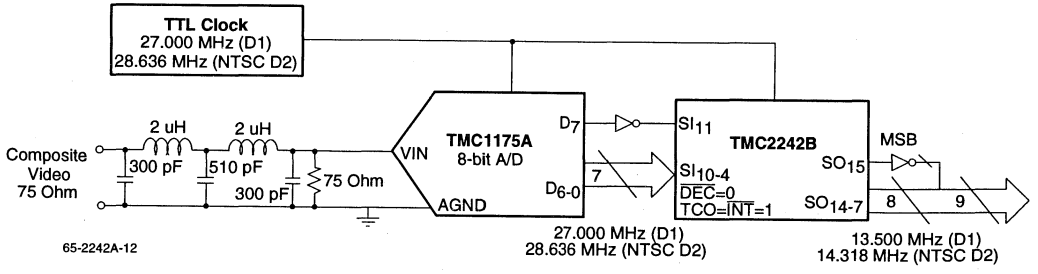
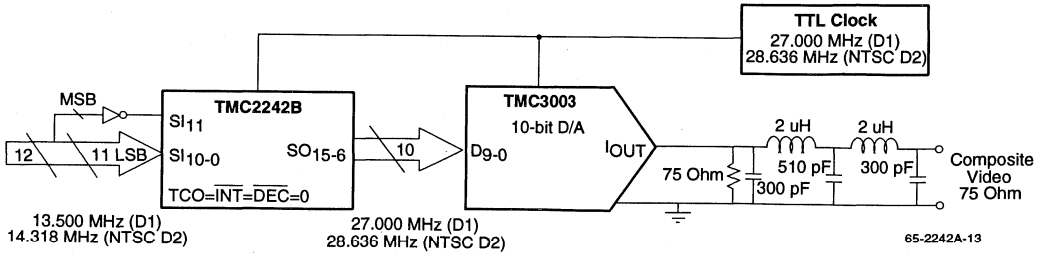


Figure 10. Decimating Oversampled Video With a Low Cost 8-bit A/D



Note: Data buses are unsigned binarys; TMC2242 input is two's complement.

Figure 11. Interpolating Digital Video Signals before Reconstruction

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2242AR2C	0°C to 70°C	30 MHz	Commercial	44-Lead PLCC	2242AR2C
TMC2242AR2C1	0°C to 70°C	40 MHz	Commercial	44-Lead PLCC	2242AR2C1
TMC2242AR2C2	0°C to 70°C	60 MHz	Commercial	44-Lead PLCC	2242AR2C2
TMC2242BR2C	0°C to 70°C	30 MHz	Commercial	44-Lead PLCC	2242BR2C
TMC2242BR2C1	0°C to 70°C	40 MHz	Commercial	44-Lead PLCC	2242BR2C1
TMC2242BR2C2	0°C to 70°C	60 MHz	Commercial	44-Lead PLCC	2242BR2C2

TMC2243

CMOS FIR Filter

10 x 10 Bit, 20 MHz

Features

- 20 MHz data input and computation rate
- 10 x 10 bit multiplication with 23-bit extended precision sum of products (overflow, plus 16 output and 6 guard bits)
- Up to 3 zero and 3 non-zero stages per device
- Two's complement arithmetic
- 16-bit Sum-In and Sum-Out ports for cascading
- Internal 1/2 LSB rounding
- All inputs and outputs are registered
- One coefficient update per clock cycle
- Low power consumption CMOS process
- Single +5V supply
- Available in 68-pin ceramic pin grid array and 69-pin plastic PGA packages

Applications

- FIR filters
- Adaptive filters
- Multi-bit correlation
- One and two dimension video filtering
- Radar signal processors
- One and two dimension convolution
- Arithmetic element for systolic array processors

Description

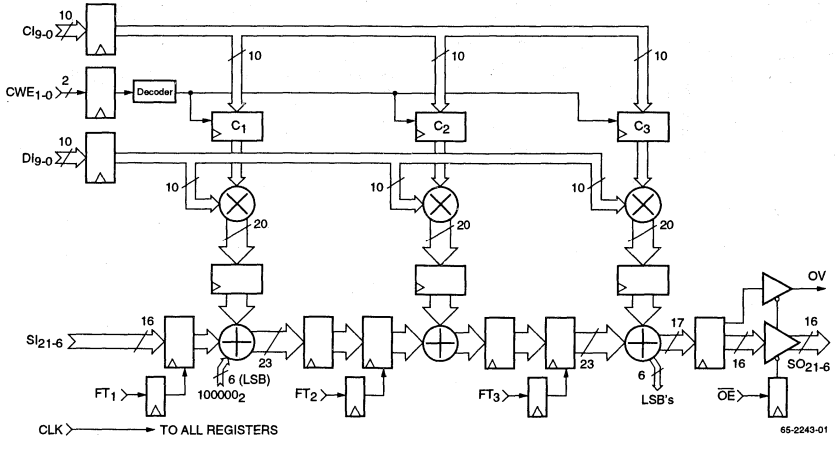
The TMC2243 is a video speed three stage 10 x 10 bit FIR (Finite Impulse Response) filter integrated circuit composed of three registered multiplier-adders concatenated into a one-dimensional systolic array. Utilizing two's complement representation, the TMC2243 accepts one 10-bit data point, updates one 10-bit coefficient, and produces one 16-bit rounded, filtered output point every 50 nanoseconds.

The TMC2243 has features which facilitate longer FIR filters: a 16-bit SUM-In port and user programmable pipeline registers. Enabling these registers allows the insertion of a zero-coefficient stage before each regular filter stage for up to six stages per TMC2243. Larger FIR filters can be built by cascading Sum-In and Sum-Out.

Coefficients are stored in 3 registers and are addressed via the 2-bit Write Enable control, allowing one coefficient to be changed per clock cycle. All Data, Sum-In, Sum-Out and instruction inputs are registered on the rising edge of clock.

The 16 bits below the MSB of the 23-bit internal summation path are available at the SUM-In and Sum-Out ports. Six bits of cumulative word growth are provided internally. Data Overflow is indicated by an output flag.

Block Diagram



Rev. 1.1.1

Functional Description

General Information

The TMC2243 consists of three identical arithmetic cells, each of which contains a 10 x 10 two's complement multiplier and a 23-bit adder. Each cell receives the current data (DI) from the Data input register, multiplies it by a locally stored Coefficient (CI_i), and adds it to the Sum $SI_{(i-1)}$ received from the previous cell. The result,

$$SI_i = DI \times CI_i + SI_{(i-1)},$$

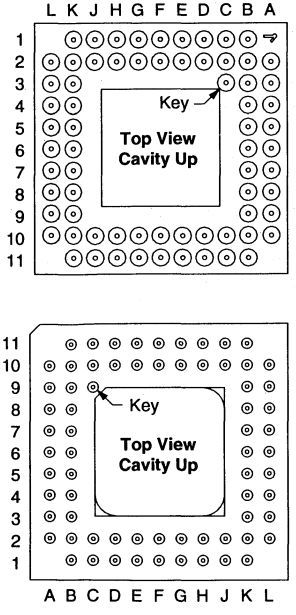
then goes to the next cell via two serial pipeline registers. When only one pipeline register is enabled, stages (i-l) and i are sequential. When both registers are enabled, there is a stage with a zero coefficient between them.

The input arithmetic cell receives $SI_{(i-1)}$ via the 16-bit Sum-In port (registered when FT_1 = LOW), filling the six lower bits with 100 000 (1/2 LSB) for internal rounding. The output cell outputs 16 of the MSBs (V_{21} through V_6) of SO_i through a register to the Sum-Out port. The Overflow flag is set when the final output exceeds 16 bits and resets with the output of the next nonoverflowing result. Sum-Out and the Overflow Flag can be forced to high-impedance with the Output Enable control. See Figure 1.

The two-bit Write Enable control specifies the loading of the three coefficient registers (one per arithmetic cell) with data appearing at the Coefficient Input port.

Pin Assignments

68 Pin Grid Array – G8 Package
69 Pin Plastic Pin Grid Array – H8 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	SO_6	B9	SO_{20}	F10	SI_{11}	K4	CI_2
A3	SO_7	B10	OV	F11	SI_{10}	K5	CI_4
A4	SO_9	B11	GND	G1	DI_6	K6	V_{DD}
A5	SO_{11}	C1	FT_0	G2	DI_7	K7	CI_7
A6	SO_{13}	C2	OE	G10	SI_{13}	K8	CI_9
A7	SO_{15}	C10	V_{DD}	G11	SI_{12}	K9	SI_{20}
A8	SO_{17}	C11	V_{DD}	H1	DI_4	K10	GND
A9	SO_{19}	D1	FT_2	H2	DI_5	K11	SI_{18}
A10	SO_{21}	D2	FT_1	H10	SI_{15}	L2	DI_0
B1	V_{DD}	D10	SI_7	H11	SI_{14}	L3	CI_1
B2	GND	D11	SI_6	J1	DI_2	L4	CI_3
B3	SO_8	E1	CWE_1	J2	DI_3	L5	CI_5
B4	SO_{10}	E2	CWE_0	J10	SI_{17}	L6	CI_6
B5	SO_{12}	E10	SI_9	J11	SI_{16}	L7	CI_8
B6	SO_{14}	E11	SI_8	K1	GND	L8	SI_{21}
B7	SO_{16}	F1	DI_8	K2	DI_1	L9	SI_{19}
B8	SO_{18}	F2	DI_9	K3	CI_0	L10	CLK

Note: Pin C3 is a mechanical orientation pin on the H8 package at manufacturer's option.

65-2243-02

Pin Descriptions

Pin Name	Pin Number	Description
Power		
V_{DD}	B1, K6, C10, C11	**Supply Voltage.** The TMC2243 operates from a single +5V supply.
GND	B2, K1, K10, B11	**Ground.**
Inputs		
DI_{9-0}	F2, F1, G2, G1, H2, H1, J2, J1, K2, L2	**Data Input.** DI_9 through DI_0 is the 10-bit registered Data Input; DI_9 is the MSB (sign bit) and DI_0 is the LSB. Data is in two's complement representation, and is clocked into the data register on each rising edge of clock. See Figure 1.
SI_{21-6}	L8, K9, L9, K11, J10, J11, H10, H11, G10, G11, F10, F11, E10, E11, D10, D11	**Sum Input.** SI_{21} through SI_6 is the 16-bit Sum-In port. SI_{21} is the MSB (sign bit). Sum-In is truncated to bit SI_6 (plus the 1/2 LSB rounding bit in SI_5) and is in two's complement representation. See Figure 1. The Sum-In port is registered, on the rising edge of clock, only when FT_1 =LOW. Unique input setup requirements must be observed when operating in the feedthrough mode (FT_1 = HIGH) See text.
CI_{9-0}	K8, L7, K7, L6, L5, K5, L4, K4, L3, K3	**Coefficient Input.** CI_9 through CI_0 is the 10-bit registered Coefficient Input; CI_9 is the MSB (sign bit) and CI_0 is the LSB. Each coefficient and its write enable address (CWE_{1-3}) are registered on the same clock. The coefficient is then latched into the indicated register (C_{1-3}) at the rising edge of the next clock. The contents of this bus are ignored if a coefficient register is not selected (CWE = 00). The format of CI_{9-0} is identical to that of DI_{9-0}.
Outputs		
SO_{21-6}	A10, B9, A9, B8, A8, B7, A7, B6, A6, B5, A5, B4, A4, B3, A3, A2	**Sum Output.** SO_{21} through SO_6 is the three-state 16-bit registered Sum-Out port; SO_{21} is the MSB (sign bit). For maximum precision, the internal products and accumulations are 23 bits but Sum-Out is internally truncated to 16 bits, and excludes the overflow bit and the 6 LSBs. The format is identical to that of SI_{21-6}. See Figure 1.
Clock		
CLK	L10	**Master Clock.** The TMC2243 has a single clock input. The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of clock.
Controls		
CWE_{1-0}	E1, E2	**Coefficient Write Enable.** The two bits of the registered Coefficient Write Enable control indicate which of the coefficient registers is to receive a new coefficient at the beginning of the next clock cycle. **CWE_{1-0} Coefficient Register Selected** 0 0 Holds all coefficients unchanged. 0 1 C_1 1 0 C_2 1 1 C_3
FT_{3-1}	D1, D2, C1	**Feedthrough.** These registered Feed Through controls select clocked (FT_i = LOW) or feedthrough (FT_i = HIGH) operation for each of the pipeline registers. Setting FT_i = LOW inserts a zero coefficient stage, or additional register, before the ith non-zero stage.
$\overline{OE}$	C2	**Output Enable.** Output Enable is a registered three-state enable control which forces the Sum-Out port and Overflow to the high-impedance state when HIGH. These outputs are enabled when $\overline{OE}$ is LOW.
Flags		
OV	B10	**Overflow.** The Overflow Flag is a registered three-state output which goes HIGH whenever the summation result exceeds 16 bits and is reset to LOW on the next nonoverflowing result.

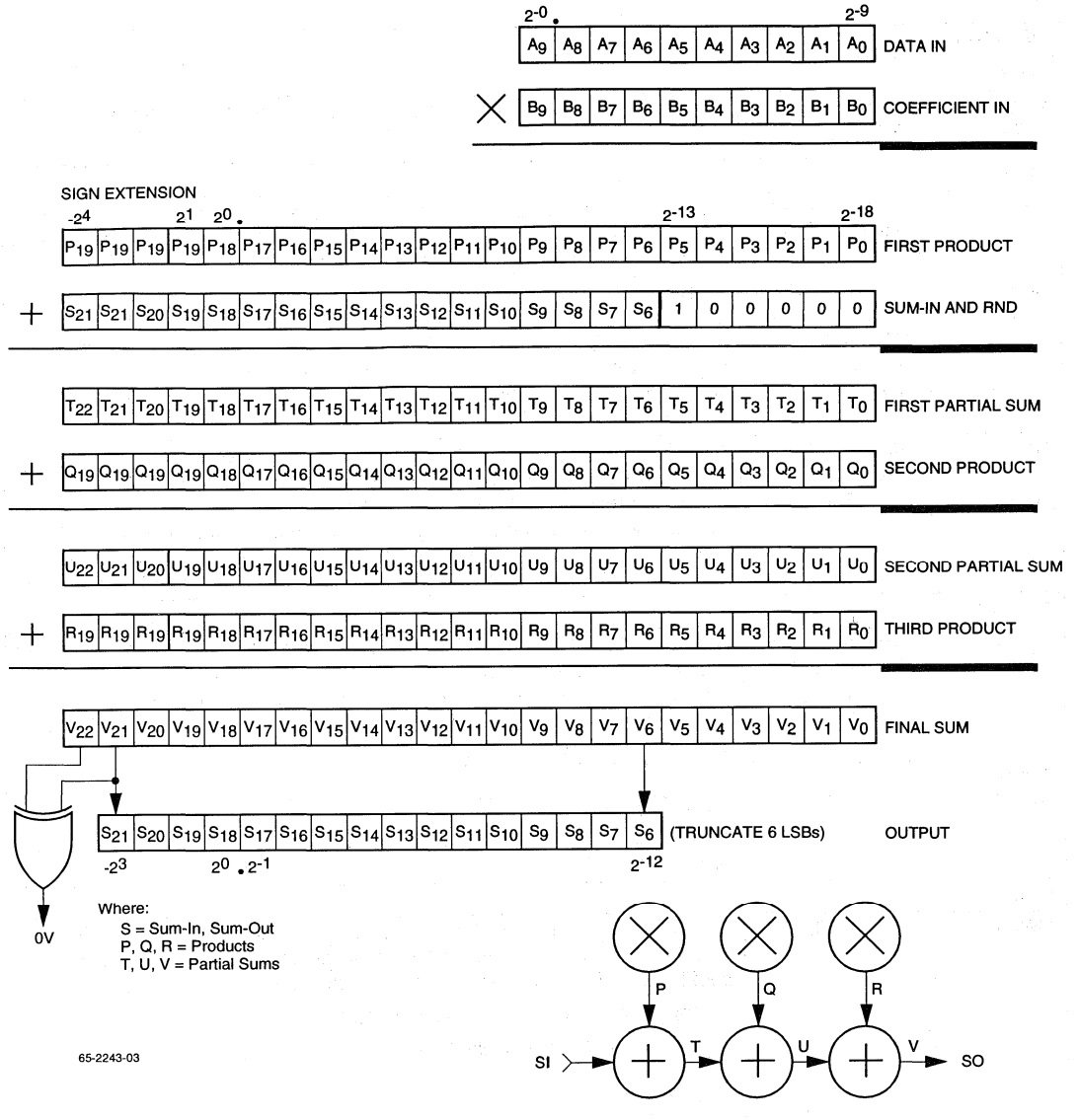
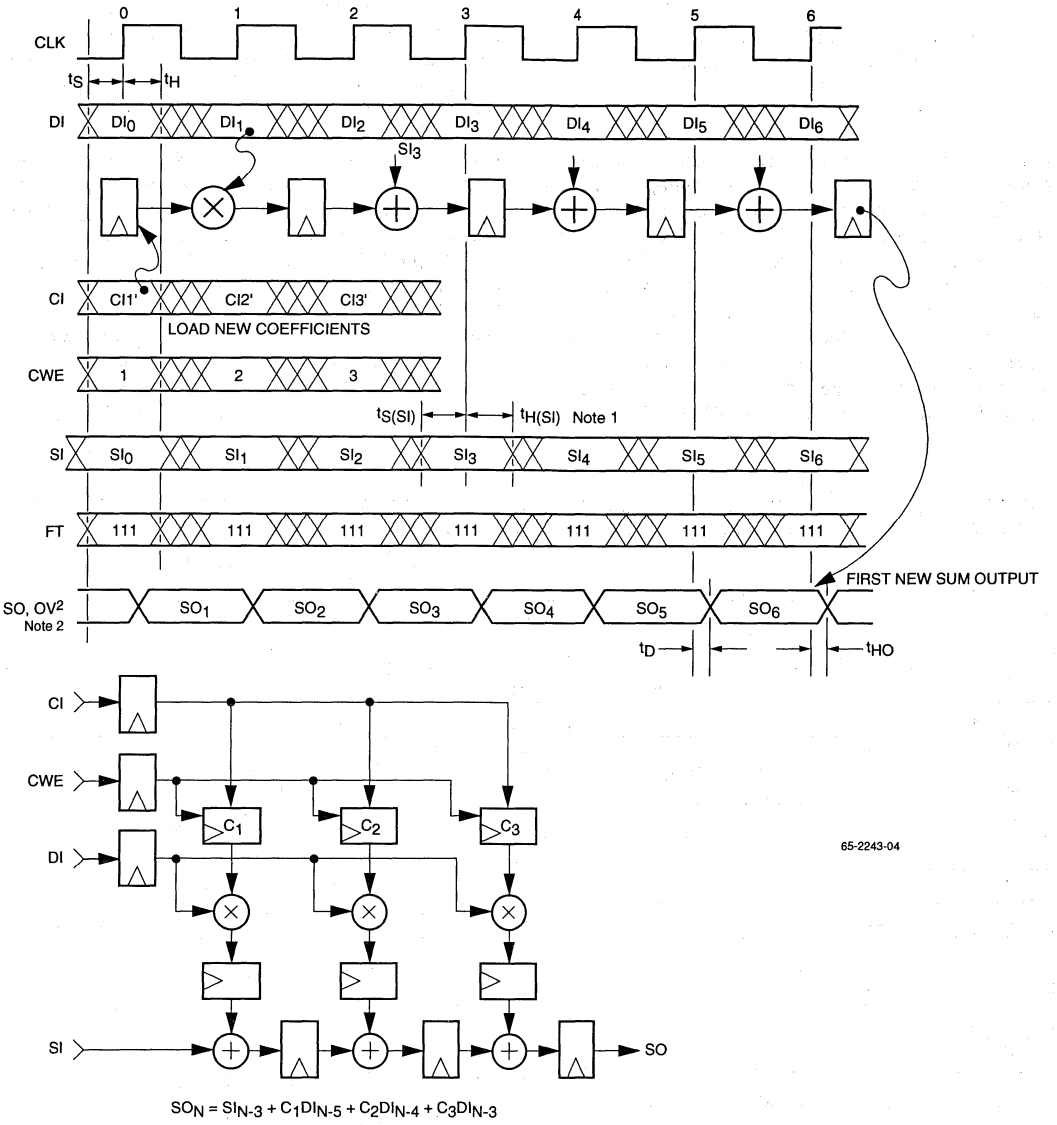


Figure 1. Data Formats and Internal Busing

Because the Sum-In and Sum-Out are truncated by 6 bits relative to the external accumulation pipeline, the TMC2243 rounds internally by adding 2^{-13} to each emerging sum of products, effecting half-LSB rounding relative to the output format. The chip internally utilizes all lower-order bits, to 2^{-18}.

Basic Operation



$$SO_N = SI_{N-3} + C_1DI_{N-5} + C_2DI_{N-4} + C_3DI_{N-3}$$

Notes:

1. Setup and Hold requirements for the Sum Input are similar to the other registered inputs when FT_1 = LOW. See text.
2. Sum Out and Overflow timing are shown with $\overline{OE}$ = LOW.

Figure 2. Timing Diagram Demonstrating Basic Operation with FT_{1-3} = HIGH (no zero stages)

The basic equation describing the function of the TMC2243 operating in a fixed state is:

$$SO(N) = SI_{(N-6+FT1+FT2+FT3)} + C_1 \times DI_{(N-7+FT2+FT3)} + C_2 \times DI_{(N-5+FT3)} + C_3 \times DI_{(N-3)}$$

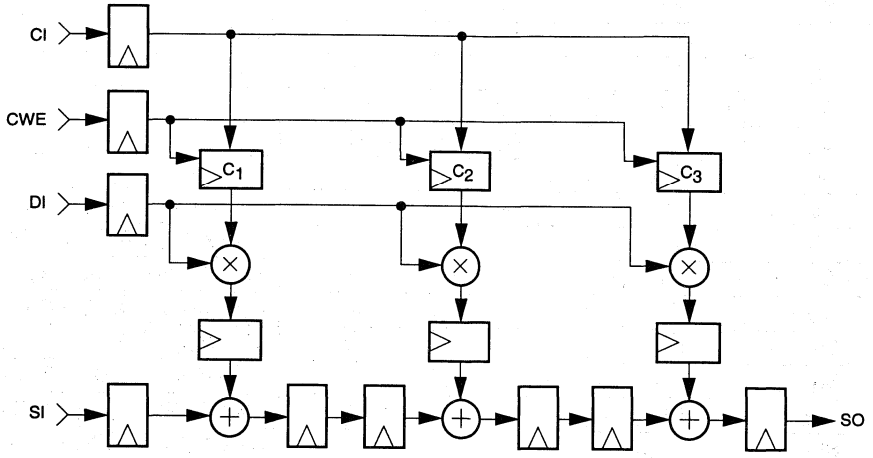
Careful observation of the clock delays shown is basic to construction of a filter algorithm. The operating sequence for the common application with $FT_{1\text{-}3}$ = HIGH (no zero stages) is shown in Figure 2. The simplified block diagram demonstrates the clock stages in this configuration. When FT_1 = HIGH, the input feedthrough register is bypassed, and care must be taken to observe the setup requirements on the input of the first adder. Due to the absence of the input register buffer, note that the adder operates on data stable just prior to the arrival of the next clock, and not that setup at the rising edge of the current clock. When FT_1 = LOW the input register latches the input data, and the Sum Input follows setup and hold requirements similar to the other registered inputs of the TMC2243. When FT_1 = HIGH, $t_{S(SI)}$ is guaranteed to allow 20MHz pipelined operation, assuming that input setup is observed, including cascaded operation. See the AC Characteristics table and Figure 9 in the Applications Discussion section.

Figure 3 shows the effects of the feedthrough registers on filter operation, with two different configurations. The inputs are those presented at the corresponding rising edge of clock, excepting the delayed setup requirements of the Sum Input when FT_1 = HIGH. The outputs are those available up to and including the corresponding edge of clock. Applications utilizing the TMC2243's ability to modify coefficients dynamically are demonstrated in Figure 4, showing the operation of a typical adaptive filter. Note that the Sum Output will be zero in the first few clock cycles of all examples only if the Coefficient Registers are initialized to zero beforehand.

Cycle	SI(A) FT_1 = LOW	SI(B) FT_1 = HIGH	DI	CI	CWE	SO
1	0	0	0	K0	01	X
2	0	0	0	K1	10	X
3	0	0	0	K2	11	X
4	SI_0	0	DI_0	0	00	X
5	SI_1	SI_0	DI_1	0	00	0
6	SI_2	SI_1	$D1_2$	0	00	0
7	SI_3	SI_2	DI_3	0	00	DI_0K_2
8	SI_4	SI_3	DI_4	K_0'	01	DI_1K_2
9	SI_5	SI_4	DI_5	0	00	$DI_0K_1 + DI_2K_2$
10	SI_6	SI_5	DI_6	K_1'	10	$SI_0 + DI_1K_1 + DI_3K_2$
11	SI7	SI_6	DI_7	0	00	$SI_1 + DI_0K_0 + DI_2K_1 + DI_4K_2$
12	SI8	SI_7	DI_8	K_2'	11	$SI_2 + DI_1K_0 + DI_3K_1 + DI_5K_2$
13	SI9	SI_8	DI_9	0	00	$SI_3 + DI_2K_0 + DI_4K_1 + DI_6K_2$
14	0	SI_9	0	0	00	$SI_4 + DI_3K_0 + DI_5K_1 + DI_7K_2$
15	0	0	0	0	00	$SI_5 + DI_4K_0 + DI_6K_1 + DI_8K_2$
16	0	0	0	0	00	$SI_6 + DI_5K_0' + DI_7K_1' + DI_9K_2'$
17	0	0	0	0	00	$SI_7 + DI_6K_0' + DI_8K_1'$
18	0	0	0	0	00	$SI_8 + DI_7K_0' + DI_9K_1'$
19	0	0	0	0	00	$SI_9 + DI_8K_0'$
20	0	0	0	0	00	DI_9K_0'
21	0	0	0	0	00	0

Figure 3. Impulse Response Filter Operation Sequence with $FT_{2,3}$ = LOW

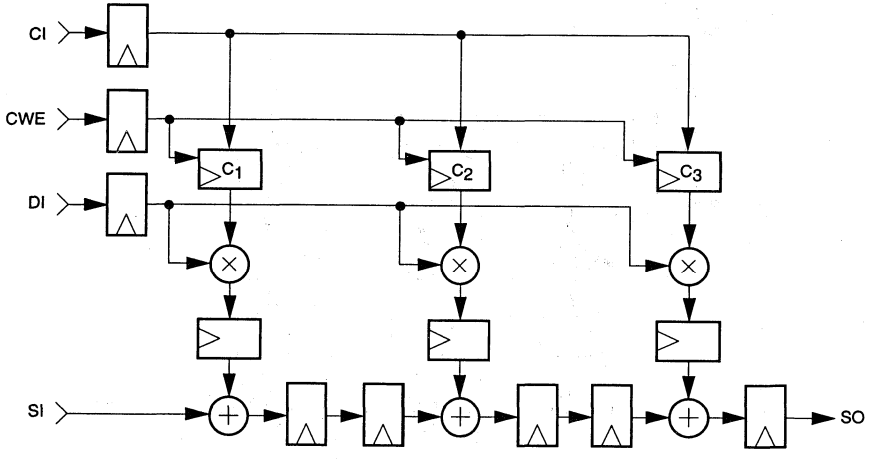
SI(A) is the sequence of Sum Input data with FT_{1-3} = LOW (three zero stages).



$SO_N = SI_{N-6} + C_1DI_{N-7} + C_2DI_{N-5} + C_3DI_{N-3}$

65-2243-05

SI(B) is the sequence of Sum Input data with FT_1 = HIGH and $FT_{2,3}$ = LOW (two zero stages).



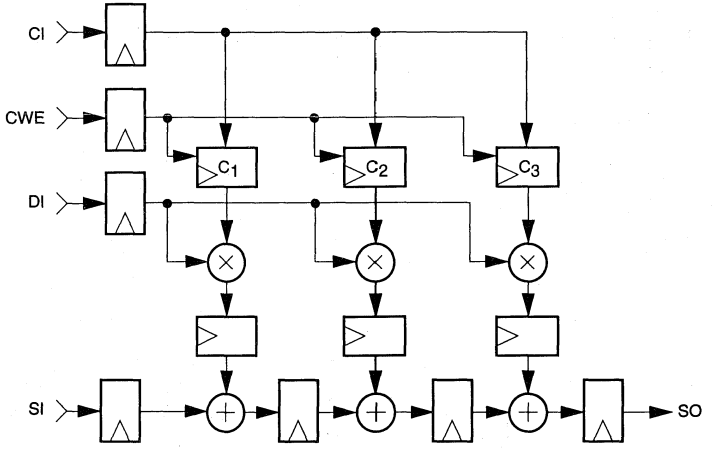
$SO_N = SI_{N-5} + C_1DI_{N-7} + C_2DI_{N-5} + C_3DI_{N-3}$

65-2243-06

Cycle	SI	DI	CI	CWE	SO
0	SI_0	DI_0	A_1	01	X
1	SI_1	DI_1	A_2	10	X
2	SI_2	DI_2	A_3	11	X
3	SI_3	DI_3	B_1	01	X
4	SI_4	DI_4	B_2	10	X
5	SI_5	DI_5	B_3	11	X
6	SI_6	DI_6	C_1	01	$SI_2 + A_1DI_1 + A_2DI_2 + A_3DI_3$
7	SI_7	DI_7	C_2	10	$SI_3 + A_1DI_2 + A_2DI_3 + A_3DI_4$
8	SI_8	DI_8	C_3	11	$SI_4 + A_1DI_3 + A_2DI_4 + A_3DI_5$
9	SI_9	DI_9		00	$SI_5 + B_1DI_4 + B_2DI_5 + B_3DI_6$
10	SI_{10}	DI_{10}		00	$SI_6 + B_1DI_5 + B_2DI_6 + B_3DI_7$
11	SI_{11}	DI_{11}		00	$SI_7 + B_1DI_6 + B_2DI_7 + B_3DI_8$
12	SI_{12}	DI_{12}		00	$SI_8 + C_1DI_7 + C_2DI_8 + C_3DI_9$
13	SI_{13}	DI_{13}		00	$SI_9 + C_1DI_8 + C_2DI_9 + C_3DI_{10}$

Figure 4. Typical Adaptive Filter Operation Sequence

with FT_1 = LOW and $FT_{2,3}$ = HIGH (one zero stage)



$SO_N = SI_{N-4} + C_1DI_{N-5} + C_2DI_{N-4} + C_3DI_{N-3}$

65-2243-07

Equivalent Circuits and Transition Levels

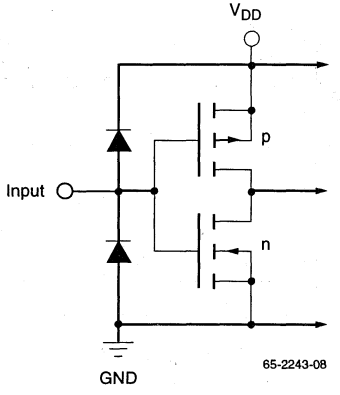


Figure 5. Equivalent Input Circuit

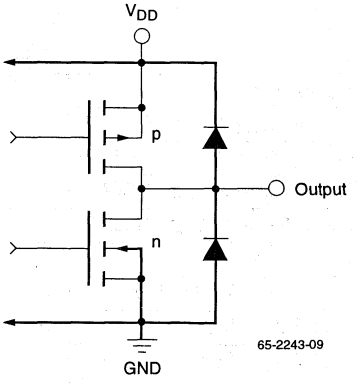


Figure 6. Equivalent Output Circuit

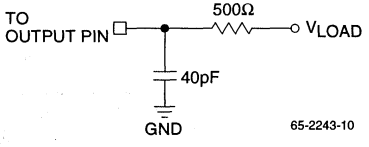
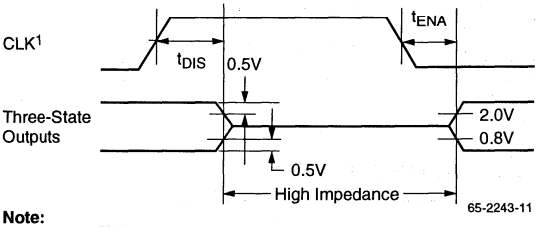


Figure 7. Test Load



Note:
1. Assumes $\overline{OE}$ has gone LOW, within the Input Setup requirements.

Figure 8. Transition Levels for Three-State Measurements

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Max	Unit
Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	VDD + 0.5	V
Output Applied Voltage[2]	0.5	VDD + 0.5	V
Output Forced Current[3,4]	-1.0	6.0	mA
Short circuit duration (single output in HIGH state to ground)		1	sec
Operating, Case Temperature	-60	130	°C
Operating, Junction Temperature		175	°C
Storage Temperature	-65	150	°C
Lead Soldering Temperature (10 seconds)		300	°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW		2.0			2.0			V
V_{IH}	Input Voltage, Logic HIGH				0.8			0.8	V
I_{OL}	Output Current, Logic LOW				4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH				-2.0			-2.0	mA
t_{CY}	Cycle Time	V_{DD} = Min	50			50			ns
t_{PWL}	Clock Pulse Width LOW	V_{DD} = Min	20			20			ns
t_{PWH}	Clock Pulse Width HIGH	V_{DD} = Min	20			20			ns
t_S	Input Setup Time		15			20			ns
$t_{S(SI)}$	Input Setup Time	SI_{21-6}, FT_1 = HIGH	25			28			ns
		FT_1 = LOW	18			20			ns
t_H	Input Hold Time		2			3			ns
$t_{H(SI)}$	Input Hold Time, SI_{21-6}		5			5			ns
T_A	Ambient Temperature, Still Air		0		70				°C
T_C	Case Temperature					-55		125	°C

DC Characteristics[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = OV, $\overline{OE}$ = HIGH		15		15	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = HIGH					
		f = 20MHz		90		90	mA
		f = 10MHz		48		48	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = OV	-75	75	-75	75	µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}	-75	75	-75	75	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min. I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = OV	-40	40	-40	40	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}	-40	40	-40	40	µA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max		-150		-150	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC Characteristics

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		30		30	ns
t_{DC}	Output Delay, Cascaded	V_{DD} = Min, C_{LOAD} = 10pF		20		20	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF	5		5		ns
t_{ENA}	Three-State Output, Enable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		20		25	ns
t_{DIS}	Three-State Output, Disable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		15		20	ns

Note:
1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Application Discussion

Loading and Updating of Coefficients

Because of the TMC2243's internal architecture, its impulse response is C_3, C_2, C_1, where C_3 is the rightmost coefficient and C_1 is the leftmost. However, for glitchless performance, coefficients must be updated from left to right: C_1 then C_2 then C_3.

For example, consider an adaptive filter whose first set of coefficients is A_i, second set is B_i and third set is C_i (Figure 4). First, the TMC2243 is initialized with A_i. If these are loaded in numerical (left to right) sequence, two of the first three data points can be loaded with them, as shown in Figure 4. Immediately after the third coefficient is loaded, the first coefficient of the next set can be loaded, if desired, along with the third data point.

Table 1. Impulse Response

FT_{3-1}	Response					
000	C_3	0	C_2	0	C_1	0
001	C_3	0	C_2	0	C_1	
010	C_3	0	C_2	C_1	0	
011	C_3	0	C_2	C_1		
100	C_3	C_2	0	C_1	0	
101	C_3	C_2	0	C_1		
110	C_3	C_2	C_1	0		
111	C_3	C_2	C_1			

Notes:
1. C_3 is she rightmost coefficient, C_1 is the leftmost
2. FT_1 is relevant only it SUMIN is used. When multiple chips are cascaded, FT_1 LOW places a zero stage between their concatenated impulse responses.

Building Longer Filters

To build a filter of more than three non-zero stages, merely concatenate a series of TMC2243s. The coefficient inputs may be connected to the data bus, a separate common coefficient bus, or separate buses, depending on system architecture, memory and bus resources, and coefficient updating requirements. The data inputs are connected to a common bus. If the first feedthrough register is used (and a zero stage is not desired there), an external register should be inserted in the data input path for proper timing (Figure 9).

The 16-bit Sum-Out port of each TMC2243 is connected to the Sum-In port of the next TMC2243 in the chain; the filter output is the Sum-Out port of the last TMC2243. Since the 6 LSBs of each TMC2243's accumulation pipeline are not output, each TMC2243 incorporates a rounding increment of 1 into the sixth bit, to minimize bias.

When TMC2243s are cascaded in this fashion, the minimum permissible clock period is the sum of the output delay and the Sum-In port's input setup time. When the Input Registers are enabled (that is, FT_1 = LOW), full 20MHz performance can be obtained.

All data and coefficient inputs and outputs are two's complement representation, whose relative scaling is presented in the Data Formats table, Figure 1. Although the data values are shown in fractional format, the user can arbitrarily rescale them, as long as consistency is maintained.

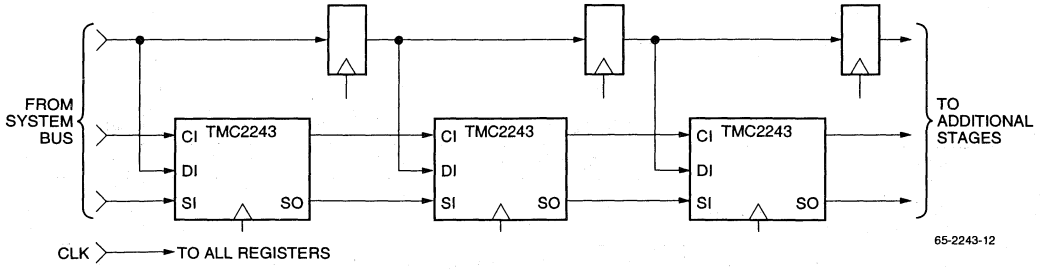


Figure 9. Basic Diagram for Stacking the TMC2243 for High–Speed Operation (no zero tap desired between each TMC2243, all FT_1 = LOW)

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2243G8C	STD-T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2243G8C
TMC2243G8V	EXT-T_C = 55°C to 125°C	MIL-STD-883	68 Pin Grid Array	2243G8V
TMC2243H8C	STD-T_A = 0°C to 70°C	Commercial	69 Pin Plastic Pin Grid Array	2243H8C

TMC2246A

Image Filter

11 x 10 bit, 60 MHz

Features

- 60 MHz computation rate
- 60 MHz data and coefficient input
- Four 11 x 10-bit multipliers
- Individual data and coefficient inputs
- 25-Bit accumulator
- Fractional and integer two's complement data formats
- Input and output data latches with user-configurable enables
- Selectable 16-bit rounded output
- Internal 1/2 LSB rounding
- Available in 120-pin PPGA or MQFP

Applications

- Fast pixel interpolation
- Fast image manipulation
- Image mixing and keying
- High-performance FIR filters
- Adaptive digital filters
- One- and two-dimensional image processing

Description

The TMC2246A is a video-speed convolutional array composed of four 11 x 10 bit registered multipliers followed by a summer and an accumulator. All eight multiplier inputs are accessible to the user and may be updated every clock cycle with integer or fractional two's complement data. A pipelined architecture, fully registered input and output ports, and asynchronous three-state output enable control simplify the design of complex systems.

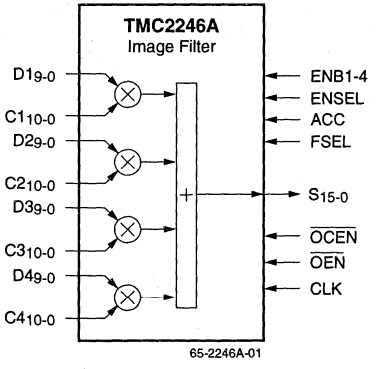
The data or coefficient inputs to the multipliers may be held over multiple clock cycles, providing storage for mixing and filtering coefficients. The 25-bit internal accumulator path allows two bits of cumulative word growth and may be internally rounded to 16 bits. Output data are updated every clock cycle, or may be held under user control. All data inputs, outputs, and controls are TTL compatible and (except for the three-state output enable) are registered on the rising edge of CLK.

The TMC2246A is uniquely suited to performing pixel interpolation in image manipulation and filtering applications. As a companion to the Raytheon Semiconductor TMC2301 and TMC2302 Image Manipulation Sequencers, the TMC2246A can execute a bilinear interpolation of an image (4-pixel kernels) at real-time video rates. Larger kernels or other, more complex, functions can be realized with no loss in performance by utilizing multiple devices.

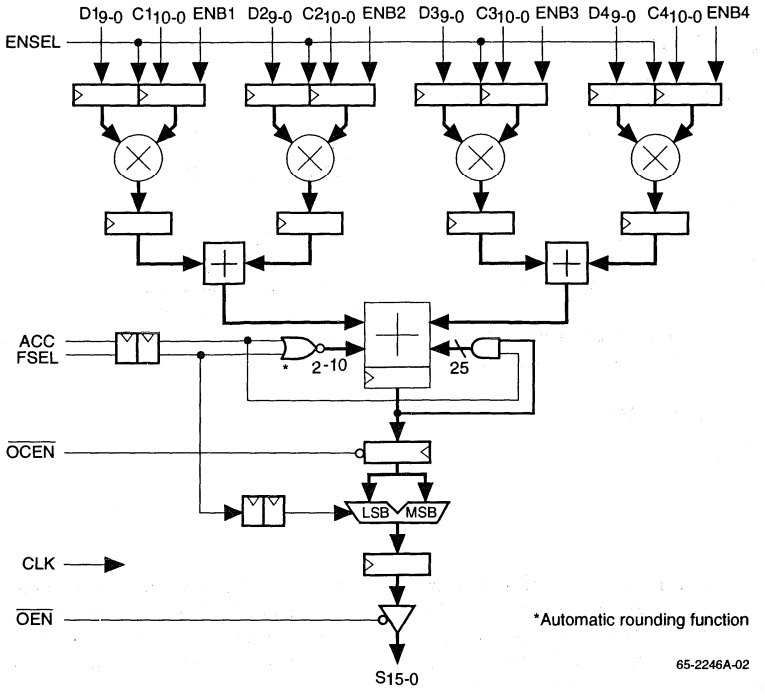
With unrestricted access to all data and coefficient input ports, the TMC2246A offers considerable flexibility in applications performing digital filtering, adaptive FIR filters, mixers, and other similar systems requiring high-speed processing.

Fabricated in a submicron CMOS process, the TMC2246A operates at a guaranteed clock rate of 60 MHz over the full temperature and supply voltage ranges. It is pin- and function-compatible with Raytheon's TMC2246, while providing higher speed operation and lower power dissipation. It is available in a 120 pin Plastic Pin Grid Array (PPGA) and a 120 lead Metric Quad FlatPack (MQFP).

Logic Symbol



Block Diagram



Functional Description

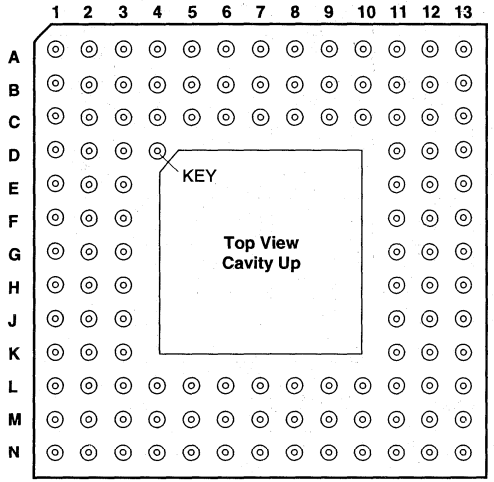
The TMC2246A Image Filter is a flexible multiplier-summer array which computes the accumulated sum of four 11x10 bit products, allowing word growth up to 25 bits.

The inputs are user-configurable, allowing latching of either the 10- or 11-bit input data. The data format is user-selectable between integer or fractional two's complement arithmetic. Total latency from input registers to output data port is 5 clocks.

The output data path is 16 bits wide, providing the lower 16 bits of the accumulator when in integer format or the upper 16 bits of the 25-bit accumulator path when fractional two's complement notation is selected. One-time rounding to 16 bits is performed automatically when accumulating fractional data, but is disabled when operating in integer format to maintain the integrity of the least-significant bits.

Pin Assignments

120 Pin Plastic Grid Array (PPGA), H5 Package



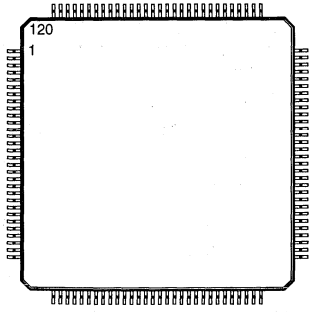
65-2246A-03

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	ENSEL	C5	$D4_8$	G11	$D3_5$	L10	$C2_8$
A2	ENB2	C6	$D4_4$	G12	$D3_6$	L11	$D2_0$
A3	ENB3	C7	GND	G13	$D3_4$	L12	$D2_4$
A4	$D4_7$	C8	V_{DD}	H1	S_6	L13	$D2_5$
A5	$D4_5$	C9	$C4_5$	H2	S_5	M1	$D1_9$
A6	$D4_2$	C10	$C4_1$	H3	V_{DD}	M2	$D1_4$
A7	$D4_1$	C11	$C3_1$	H11	GND	M3	$D1_1$
A8	$C4_{10}$	C12	$C3_3$	H12	$D3_8$	M4	$C1_{10}$
A9	$C4_8$	C13	$C3_6$	H13	$D3_7$	M5	$C1_7$
A10	$C4_6$	D1	S_{13}	J1	S_4	M6	$C1_5$
A11	$C4_3$	D2	S_{14}	J2	S_3	M7	$C1_3$
A12	$C4_0$	D3	$\overline{OCEN}$	J3	GND	M8	$C1_0$
A13	$C3_2$	D11	$C3_4$	J11	$D2_7$	M9	$C2_2$
B1	ACC	D12	$C3_7$	J12	$D2_9$	M10	$C2_5$
B2	FSEL	D13	$C3_9$	J13	$D3_9$	M11	$C2_9$
B3	ENB4	E1	S_{11}	K1	S_2	M12	$D2_1$
B4	$D4_9$	E2	S_{12}	K2	S_1	M13	$D2_2$
B5	$D4_6$	E3	GND	K3	$D1_8$	N1	$D1_6$
B6	$D4_3$	E11	$C3_8$	K11	$D2_3$	N2	$D1_3$
B7	$D4_0$	E12	$C3_{10}$	K12	$D2_6$	N3	$D1_0$
B8	$C4_9$	E13	$D3_0$	K13	$D2_8$	N4	$C1_8$
B9	$C4_7$	F1	S_9	L1	S_0	N5	$C1_6$
B10	$C4_4$	F2	S_{10}	L2	$D1_7$	N6	$C1_4$
B11	$C4_2$	F3	V_{DD}	L3	$D1_5$	N7	$C1_2$
B12	$C3_0$	F11	$D3_1$	L4	$D1_2$	N8	$C1_1$
B13	$C3_5$	F12	$D3_2$	L5	$C1_9$	N9	$C2_1$
C1	S_{15}	F13	$D3_3$	L6	GND	N10	$C2_3$
C2	$\overline{OEN}$	G1	S_7	L7	V_{DD}	N11	$C2_6$
C3	CLK	G2	S_8	L8	$C2_0$	N12	$C2_7$
C4	ENB1	G3	GND	L9	$C2_4$	N13	$C2_{10}$

BROADCAST VIDEO

Pin Assignments (continued)

120 Lead Metric Quad Flat Pack (KE) Package



65-2246A-04

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	CLK	25	S_1	49	$C1_0$	73	$D3_8$	97	$C4_4$
2	FSEL	26	S_0	50	$C2_0$	74	$D3_7$	98	$C4_5$
3	ACC	27	$D1_9$	51	$C2_1$	75	$D3_6$	99	$C4_6$
4	$\overline{OCEN}$	28	$D1_8$	52	$C2_2$	76	$D3_5$	100	$C4_7$
5	$\overline{OEN}$	29	$D1_7$	53	$C2_3$	77	$D3_4$	101	$C4_8$
6	S_{15}	30	$D1_6$	54	$C2_4$	78	$D3_3$	102	V_{DD}
7	S_{14}	31	$D1_5$	55	$C2_5$	79	$D3_2$	103	$C4_9$
8	GND	32	$D1_4$	56	$C2_6$	80	$D3_1$	104	$C4_{10}$
9	S_{13}	33	$D1_3$	57	$C2_7$	81	$D3_0$	105	$D4_0$
10	S_{12}	34	$D1_2$	58	$C2_8$	82	$C3_{10}$	106	GND
11	S_{11}	35	$D1_1$	59	$C2_9$	83	$C3_9$	107	$D4_1$
12	V_{DD}	36	$D1_0$	60	$C2_{10}$	84	$C3_8$	108	$D4_2$
13	S_{10}	37	$C1_{10}$	61	$D2_0$	85	$C3_7$	109	$D4_3$
14	S_9	38	$C1_9$	62	$D2_1$	86	$C3_6$	110	$D4_4$
15	S_8	39	$C1_8$	63	$D2_2$	87	$C3_5$	111	$D4_5$
16	GND	40	$C1_7$	64	$D2_3$	88	$C3_4$	112	$D4_6$
17	S_7	41	$C1_6$	65	$D2_4$	89	$C3_3$	113	$D4_7$
18	S_6	42	GND	66	$D2_5$	90	$C3_2$	114	$D4_8$
19	S_5	43	$C1_5$	67	$D2_6$	91	$C3_1$	115	$D4_9$
20	V_{DD}	44	$C1_4$	68	$D2_7$	92	$C3_0$	116	ENB3
21	S_4	45	$C1_3$	69	$D2_8$	93	$C4_0$	117	ENB2
22	S_3	46	V_{DD}	70	$D2_9$	94	$C4_1$	118	ENB1
23	S_2	47	$C1_2$	71	$D3_9$	95	$C4_2$	119	ENB4
24	GND	48	$C1_1$	72	GND	96	$C4_3$	120	ENSEL

Pin Descriptions

Pin Name	Pin Number PGA	Pin Number MQFP	Pin Function Description
Power			
V_{DD}	F3, H3, L7, C8	12, 20, 46, 102	**Supply Voltage.** The TMC2246A operates from a single +5V supply. All power and ground pins must be connected.
GND	E3, G3, J3, L6, H11, C7	8, 16, 24, 42, 72, 106	**Ground.** The TMC2246A operates from a single +5V supply. All power and ground pins must be connected.
Clock			
CLK	C3	1	**System Clock.** The TMC2246A operates from a single master clock input. The rising edge of clock strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.
Inputs			
D19-0	M1, K3, L2, N1, L3, M2, N2, L4, M3, N3	27, 28, 29, 30, 31, 32, 33, 34, 35, 36	**Data Input Ports.** D1 through D4 are the 10-bit data input ports. The LSB is Dx_0.
D29-0	J12, K13, J11, K12, L13, L12, K11, M13, M12, L11	70, 69, 68, 67, 66, 65, 64, 63, 62, 61	
D39-0	J13, H12, H13, G12, G11, G13, F13, F12, F11, E13	71, 73, 74, 75, 76, 77, 78, 79, 80, 81	
D49-0	B4, C5, A4, B5, A5, C6, B6, A6, A7, B7	115, 114, 113, 112, 111, 110, 109, 108, 107, 105	
C110-0	M4, L5, N4, M5, N5, M6, N6, M7, N7, N8, M8	37, 38, 39, 40, 41, 43, 44, 45, 47, 48, 49	**Coefficient Input Ports.** C1 through C4 are the 11-bit coefficient input ports. The LSB is Cx_0.
C210-0	N13, M11, L10, N12, N11, M10, L9, N10, M9, N9, L8	60, 59, 58, 57, 56, 55, 54, 53, 52, 51, 50	
C310-0	E12, D13, E11, D12, C13, B13, D11, C12, A13, C11, B12	82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92	
C410-0	A8, B8, A9, B9, A10, C9, B10, A11, B11, C10, A12	104, 103, 101, 100, 99, 98, 97, 96, 95, 94, 93	
Outputs			
S15-0	C1, D2, D1, E2, E1, F2, F1, G2, G1, H1, H2, J1, J2, K1, K2, L1	6, 7, 9, 10, 11, 13, 14, 15, 17, 18, 19, 21, 22, 23, 25, 26	**Sum Output.** The current 16-bit result is available at the Sum output. The LSB is S_0. See the Functional Block Diagram.

Pin Descriptions (continued)

Pin Name	Pin Number PGA	Pin Number MQFP	Pin Function Description
Controls			
FSEL	B2	2	**Format Select.** Coefficients input during the current clock are assumed to be in fractional two's complement format. Rounding to 16 bits is performed as determined by the accumulator control, ACC, and the upper 16 bits of the accumulator are output when the registered Format Select input (FSEL) is LOW. When FSEL is HIGH, two's complement integer format is assumed, and the lower 16 bits of the accumulator are presented at the output. No rounding is performed when operating in integer mode. See the Functional Block Diagram and the Applications Discussion.
ENSEL	A1	120	**Enable Select.** The registered Enable Select determines whether the data or the coefficient input registers may be held on the next rising edge of clock, in conjunction with the individual input enables ENB1–ENB4. See Table 1.
ENB1–ENB4	C4, A2, A3, B3	118, 117, 116, 119	**Input Enables.** When ENBi (i=1, 2, 3, or 4) is LOW, registers Ci and Di are both strobed by the next rising edge of CLK. When ENBi is HIGH and ENSEL is LOW, Di is strobed, but Ci is held. When ENBi and ENSEL are both HIGH, Di is held and Ci is strobed. See Table 1. Thus, either or both input registers to each multiplier are updated on each clock cycle.
ACC	B1	3	**Accumulate.** When the registered ACCumulator control is LOW, no internal accumulation will be performed on the data input during the current clock, effectively clearing the prior accumulated sum. If operating in fractional two's complement format (FSEL = LOW), one-half LSB rounding to 16 bits is performed on the result. This allows the user to perform summations without propagating roundoff errors. When ACC is HIGH, the internal accumulator adds the emerging products to the sum of previous products, without performing additional rounding.
$\overline{\text{OCEN}}$	D3	4	**Output Register Enable.** The output of the accumulator is latched into the output register on the next clock when the registered Clock Enable is LOW. When $\overline{\text{OCEN}}$ is HIGH the contents of the output register remain unchanged; however, accumulation will continue internally if ACC remains HIGH.
$\overline{\text{OEN}}$	C2	5	**Output Enable.** Data currently in the output registers is available at the output bus $S_{15\text{-}0}$ when the asynchronous Output Enable is LOW. When $\overline{\text{OEN}}$ is HIGH, the outputs are in the high-impedance state.
No Connect			
NC	D4 (Index Pin)		Not Connected.

Table 1. Input Register Control

ENB1-4	ENSEL	Input Register Held
1	1	Data i
1	0	Coefficient i
0	X	None

Note:
1. X denotes a "Don't Care" condition.
2. Any register not explicitly held is updated on the next rising edge of CLK.

Data Formats

Fractional Two's Complement Format (FSEL = LOW)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						-2^{0}.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	DATA (D1-4)
					-2^{1}	2^{0}.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	COEFFICIENT (C1-4)
-2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	SUM

Integer Two's Complement Format (FSEL = HIGH)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						-2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}.	DATA (D1-4)
					-2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}.	COEFFICIENT (C1-4)
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}.	SUM

Integer Two's Complement Data / Fractional Two's Complement Coefficient Format (FSEL = LOW)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						-2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}.	DATA (D1-4)
					-2^{1}	2^{0}.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	COEFFICIENT (C1-4)
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}.	SUM

Note: A minus sign indicates the sign bit.

Figure 1. Data Formats

Equivalent Circuits and Threshold Levels

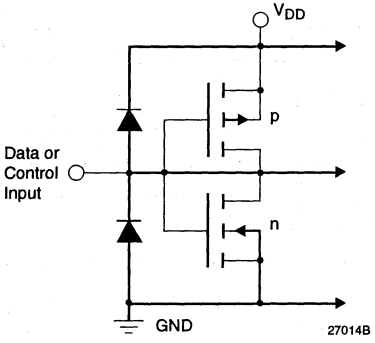


Figure 2. Equivalent Digital Input Circuit

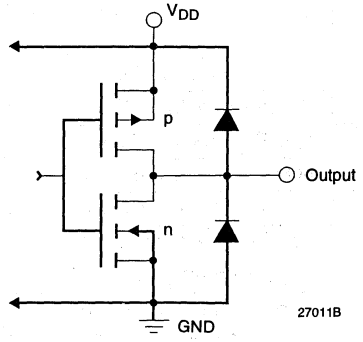


Figure 3. Equivalent Digital Output Circuit

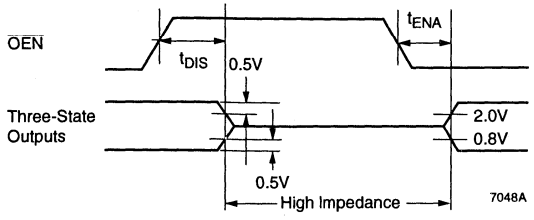


Figure 4. Threshold Levels for Three-State Measurement

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Max	Unit
Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	V_{DD} + 0.5	V
Output, Applied Voltage[2]	-0.5	V_{DD} + 0.5	V
Output, Externally Forced Current[3,4]	-3.0	6.0	mA
Output, Short Circuit Duration (single output in HIGH state to ground)		1	sec
Operating, Ambient Temperature	-20	110	°C
Junction Temperature		140	°C
Storage Temperature	-65	150	°C
Lead Soldering (10 seconds)		300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2246A			30	MHz
		TMC2246A-1			40	MHz
		TMC2246A-2			60	MHz
t_{PWH}	CLK pulse width, HIGH		8			ns
t_{PWL}	CLK pulse width, LOW		6			ns
t_S	Input Data Set-up Time		6			ns
t_H	Input Data Hold Time		1.5			ns
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Total Power Supply Current	V_{DD} = Max, C_{LOAD} = 25pF, f_{CLK} = Max				
		TMC2246A			95	mA
		TMC2246A-1			120	mA
		TMC2246A-2			170	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OEN}$ = HIGH, f_{CLK} = Max				
		TMC2246A			80	mA
		TMC2246A-1			100	mA
		TMC2246A-2			140	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	S_{15-0}, I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	S_{15-0}, I_{OL} = Max			0.4	V

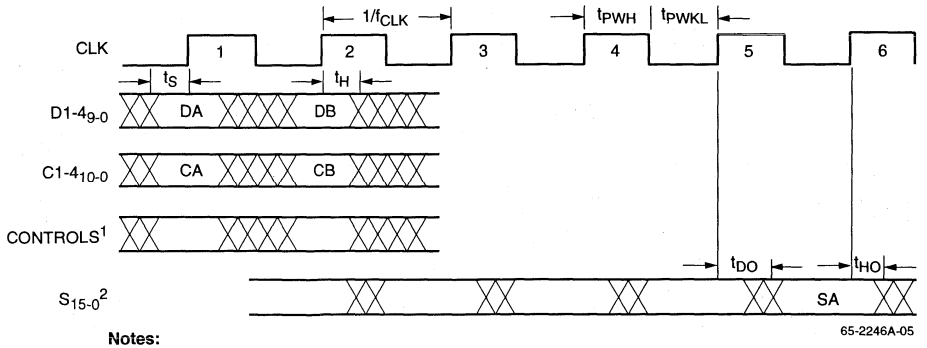
Switching Characteristics

Parameter		Conditions[1]	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			14	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	4			ns
t_{ENA}	Three-State Output Enable Delay	C_{LOAD} = 0 pF			10	ns
t_{DIS}	Three-State Output Disable Delay	C_{LOAD} = 0 pF			10	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS}.

Timing Diagram



Notes:
1. Except $\overline{OEN}$.
2. Assumes $\overline{OEN}$ = LOW.

Application Notes

Typical Operation

The versatile input clock enables and unrestricted data and coefficient inputs provided on the TMC2246A allow considerable flexibility in numerous image and signal processing architectures.

Table 2 shows a typical sequence of operations which clarifies the inherent latencies of the device and illustrates fixed coefficient storage, product accumulation, and device reconfiguration prior to beginning a new accumulation. This assumes that the device is set to fractional two's complement mode (FSEL = LOW) with $\overline{OCEN}$ = LOW, $\overline{OEN}$ = LOW, and the input registers configured to hold coefficients only (ENSEL = LOW). X= "don't care."

Using the TMC2246A for Pixel Interpolation

As a companion product to the TMC2301 Image Resampling Sequencer, the TMC2246A offers an excellent tool for performing high-speed pixel interpolation and image filtering.

Any pixel resampling operation with multiple-pixel kernels must utilize some parallel-processing technique, such as memory banding, to maintain high-speed image throughput rates. Memory banding utilizes adders to generate parallel offset addresses, allowing the user to access multiple pixel locations simultaneously. Using such techniques, one TMC2246A can perform bilinear interpolation (four-pixel kernel) with no loss in system performance.

Larger kernels can be realized in similar systems with additional TMC2246As. Figure 5 illustrates a basic pixel interpolation application.

Table 2. Typical TMC2246A Operation Sequence

CLK	D1	C1	ENB1	D2	C2	ENB2	D3	C3	ENB3	D4	C4	ENB4	ACC	Sum
0	-	-	0	-	-	0	-	-	0	-	-	0	-	-
1	D1(1)	C1(1)	1	D2(1)	C2(1)	1	D3(1)	C3(1)	1	D4(1)	C4(1)	1	0	-
2	D1(2)	X	0	D2(2)	C2(2)	0	D3(2)	X	1	D4(2)	X	1	1	-
3	D1(3)	C1(3)	0	D2(3)	C2(3)	0	D3(3)	X	0	D4(3)	X	0	1	
4	D1(4)	C1(4)	-	D2(4)	C2(4)	-	D3(4)	C3(4)	-	D4(4)	C4(4)	-	0	
5														$S(5)= D1(1)C1(1)+D2(1)C2(1) +D3(1)C3(1)+D4(1)C4(1)+ 2^{-10}$
6														$S(6)= S(5)+D1(2)C1(1)+D2(2)C2(1) +D3(2)C3(1)+D4(2)C4(1)$
7														$S(7)= S(6)+D1(3)C1(3)+D2(3)C2(3) +D3(3)C3(1)+D4(3)C4(1)$
8														$S(8)= D1(4)C1(4)+D2(4)C2(4) +D3(4)C3(4)+D4(4)C4(4)+2^{-10}$

Notice in this example, operating in fractional two's complement mode, that rounding is imposed on the first cycle only of an accumulation. This avoids the propagation of accumulated roundoff errors.

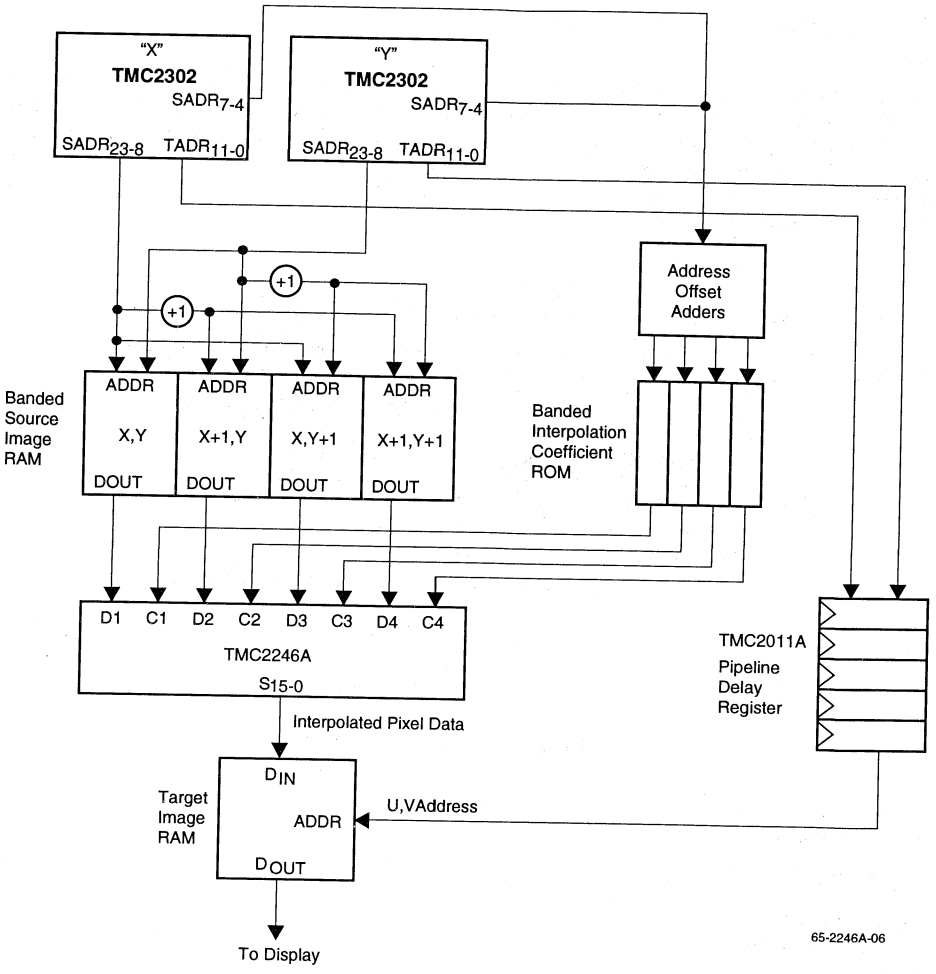


Figure 5. Bilinear Interpolation Using the TMC2246A

TMC2246A Applications in Digital Filtering

Unrestricted access to all input ports of the TMC2246A allows the user considerable flexibility in realizing numerous digital filter architectures. Figure 6 illustrates how the device may be utilized as a flexible high-speed FIR filter with the ability to modify all of the filter coefficients dynamically or to store a fixed set if desired.

Longer filters, with more taps, are realized by including an external adder (such as the common 74381 type) to cascade multiple TMC2246As. Alternatively, two additional taps and a cascading adder are available in the Raytheon TMC2249A Digital Mixer.

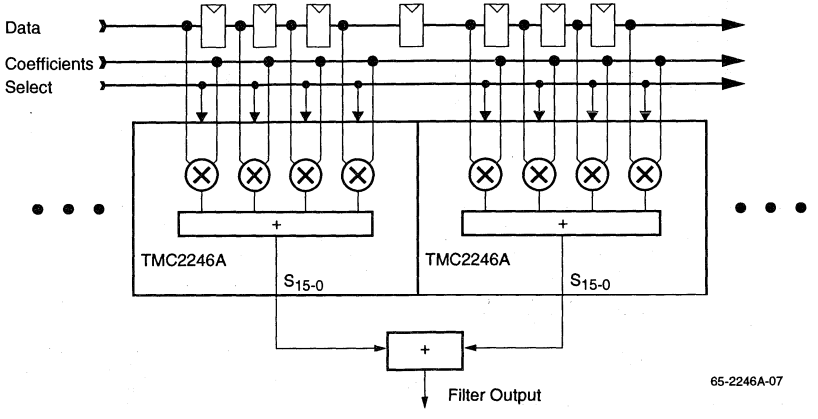


Figure 6. Using the TMC2246A For FIR Filtering

Related Products

- TMC2301 Image Resampling Sequencer
- TMC2302 Image Manipulation Sequencer
- TMC2249A Video Mixer
- TMC2242B Half-Band Filter

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2246AH5C	0°C to 70°C	30 MHz	Commercial	120 Pin Plastic Pin Grid Array	2246AH5C
TMC2246AH5C1	0°C to 70°C	40 MHz	Commercial	120 Pin Plastic Pin Grid Array	2246AH5C1
TMC2246AH5C2	0°C to 70°C	60 MHz	Commercial	120 Pin Plastic Pin Grid Array	2246AH5C2
TMC2246AKEC	0°C to 70°C	30 MHz	Commercial	120 Lead Metric Quad FlatPack	2246AKEC
TMC2246AKEC1	0°C to 70°C	40 MHz	Commercial	120 Lead Metric Quad FlatPack	2246AKEC1
TMC2246AKEC2	0°C to 70°C	60 MHz	Commercial	120 Lead Metric Quad FlatPack	2246AKEC2

TMC2249A

Digital Mixer

12 x 12 bit, 60 MHz

Features

- 60 MHz input and computation rate
- Two 12-bit multipliers
- Separate data and coefficient inputs
- Independent, user-selectable pipeline delays of 1 to 16 clocks on all input ports
- Separate 16-bit input port allows cascading or addition of a constant
- User-selectable rounded output
- Internal 1/2 LSB rounding of products
- Fully registered, pipelined architecture
- Available in 120-Pin PPGA or MQFP

Applications

- Video switching
- Image mixing
- Digital signal modulation
- Complex frequency synthesis
- Digital filtering
- Complex arithmetic functions

Description

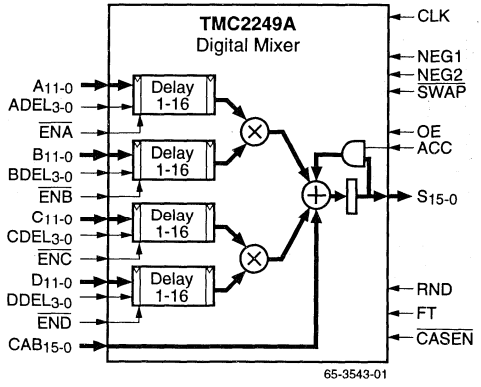
The TMC2249A is a high-speed digital arithmetic circuit consisting of two 12-bit multipliers, an adder and a cascadeable accumulator. All four multiplier inputs are simultaneously accessible to the user, and each includes a user-programmable pipeline delay of up to 16 clocks in length. The 24-bit adder/subtractor is followed by an accumulator and 16-bit input port which allows the user to cascade multiple TMC2249As. A new 16-bit accumulated output is available every clock, up to the maximum rate of 60 MHz. All inputs and outputs are registered except the three-state output enable, and all are TTL compatible.

The TMC2249A utilizes a pipelined, bus-oriented structure offering significant flexibility. Input register clock enables and programmable input data pipeline delays on each port offer an adaptable input structure for high-speed digital systems. Following the multipliers, the user may perform addition or subtraction of either product, arithmetic rounding to 16 bits, and accumulation and summation of products with a cascading input. The output port allows access to all 24 bits of the internal accumulator by switching between overlapping least and most-significant 16-bit words, and a three-state output enable simplifies connection to an external system bus.

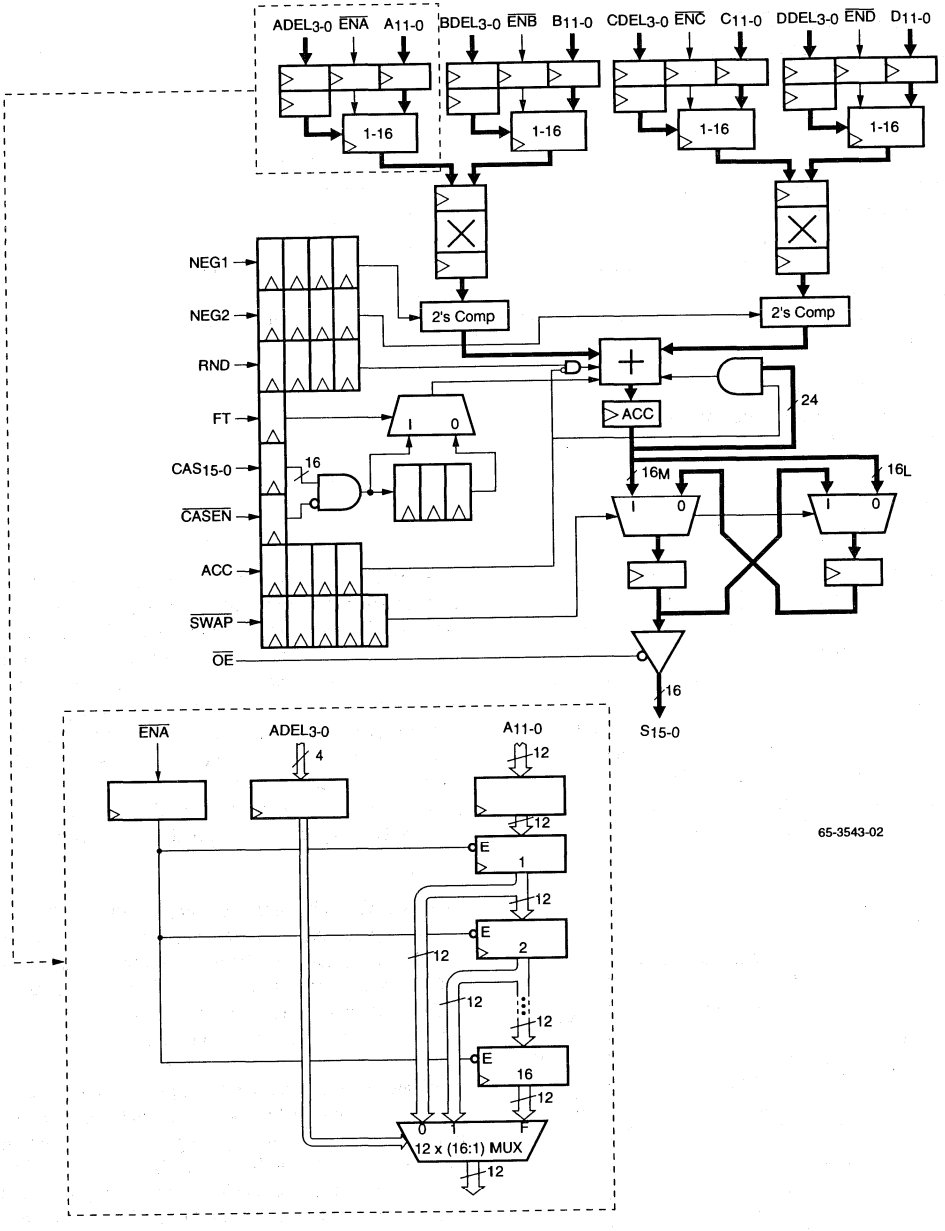
The TMC2249A has numerous applications in digital processing algorithms, from executing simple image mixing and switching, to performing complex arithmetic functions and complex waveform synthesis. FIR filters, digital quadrature mixers and modulators, and vector arithmetic functions may also be implemented with this device.

Fabricated in a submicron CMOS process, the TMC2249A operates at guaranteed clock rates of up to 60 MHz over the full temperature and supply voltage ranges. It is pin- and function-compatible with Raytheon's TMC2249, while providing higher speed operation and lower power dissipation. It is available in a 120 pin Plastic Pin Grid Array (PPGA) and a 120 lead Metric Quad FlatPack (MQFP).

Logic Symbol



Block Diagram



Functional Description

The TMC2249A performs the summation of products described by the formula:

$$S(N+5) = A(N\text{-}ADEL) \times B(N\text{-}BDEL) \times (-1^{NEG1(N)}) + C(N\text{-}CDEL) \times D(N\text{-}DDEL) \times (-1^{NEG2(N)}) + CAS(N+3 \times FT)$$

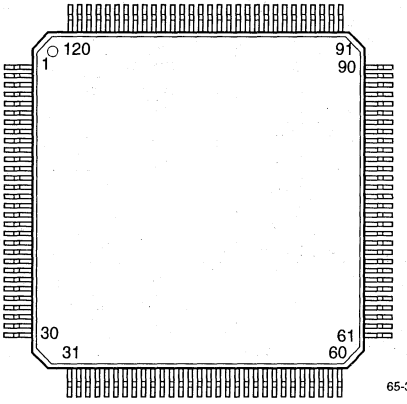
where ADEL through DDEL range from 1 to 16 pipe delays.

All inputs and controls utilize pipeline delay registers to maintain synchronicity with the data input during that clock, except when the Cascade data input is routed directly to the accumulator by use of the Feedthrough control. One-half LSB rounding to 16 bits may be performed on the sum of products while summing with the cascade input data.

The user may access either the upper or lower 16 bits of the 24-bit accumulator by swapping overlapping registers. The output bus has an asynchronous high-impedance enable, to simplify interfacing to complex systems.

Pin Assignments

120 Pin Metric Quad Flat Pack, KE Package

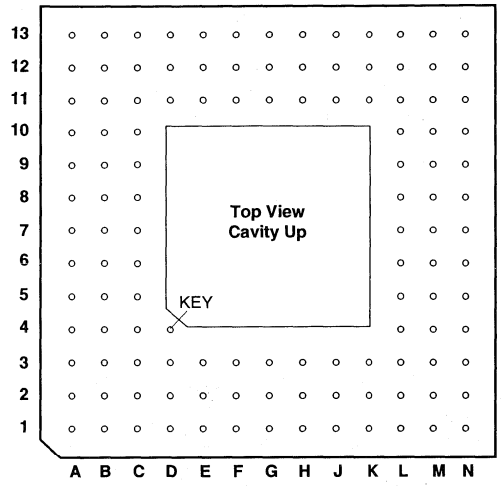


65-3543-06

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	CLK	31	$BDEL_2$	61	$ADEL_3$	91	C_1
2	ACC	32	$BDEL_3$	62	$ADEL_2$	92	C_2
3	NEG1	33	$\overline{ENB}$	63	$ADEL_1$	93	C_3
4	NEG2	34	B_0	64	$ADEL_0$	94	C_4
5	RND	35	B_1	65	NC	95	C_5
6	S_{15}	36	B_2	66	CAS_{15}	96	C_6
7	S_{14}	37	B_3	67	CAS_{14}	97	C_7
8	GND	38	B_4	68	CAS_{13}	98	C_8
9	S_{13}	39	B_5	69	CAS_{12}	99	C_9
10	S_{12}	40	B_6	70	CAS_{11}	100	C_{10}
11	S_{11}	41	B_7	71	CAS_{10}	101	C_{11}
12	V_{DD}	42	GND	72	GND	102	V_{DD}
13	S_{10}	43	B_8	73	CAS_9	103	D_{11}
14	S_9	44	B_9	74	CAS_8	104	D_{10}
15	S_8	45	B_{10}	75	CAS_7	105	D_9
16	GND	46	V_{DD}	76	CAS_6	106	GND
17	S_7	47	B_{11}	77	CAS_5	107	D_8
18	S_8	48	A_{11}	78	CAS_4	108	D_7
19	S_5	49	A_{10}	79	CAS_3	109	D_6
20	V_{DD}	50	A_9	80	CAS_2	110	D_5
21	S_4	51	A_8	81	CAS_1	111	D_4
22	S_3	52	A_7	82	CAS_0	112	D_3
23	S_2	53	A_6	83	$\overline{CASEN}$	113	D_2
24	GND	54	A_5	84	FT	114	D_1
25	S_1	55	A_4	85	$CDEL_0$	115	D_0
26	S_0	56	A_3	86	$CDEL_1$	116	$\overline{END}$
27	$\overline{OE}$	57	A_2	87	$CDEL_2$	117	$DDEL_3$
28	$\overline{SWAP}$	58	A_1	88	$CDEL_3$	118	$DDEL_2$
29	$BDEL_0$	59	A_0	89	$\overline{ENC}$	119	$DDEL_1$
30	$BDEL_1$	60	$\overline{ENA}$	90	C_0	120	$DDEL_0$

Pin Assignments (continued)

120 Pin Plastic Grid Array, H5 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	$DDEL_0$	C5	D_1	G11	CAS_6	L10	A_1
A2	$DDEL_3$	C6	D_5	G12	CAS_7	L11	$ADEL_3$
A3	$\overline{END}$	C7	GND	G13	CAS_5	L12	NC
A4	D_2	C8	V_{DD}	H1	S_6	L13	CAS_{15}
A5	D_4	C9	C_8	H2	S_5	M1	$\overline{OE}$
A6	D_7	C10	C_4	H3	V_{DD}	M2	$BDEL_3$
A7	D_8	C11	C_1	H11	GND	M3	B_1
A8	D_{10}	C12	$\overline{ENC}$	H12	CAS_9	M4	B_3
A9	C_{11}	C13	$CDEL_1$	H13	CAS_8	M5	B_6
A10	C_9	D1	S_{13}	J1	S_4	M6	B_8
A11	C_6	D2	S_{14}	J2	S_3	M7	B_{10}
A12	C_3	D3	GND	J3	GND	M8	A_{10}
A13	C_0	D11	$CDEL_3$	J11	CAS_{13}	M9	A_7
B1	NEG1	D12	$CDEL_0$	J12	CAS_{11}	M10	A_4
B2	ACC	D13	$\overline{CASEN}$	J13	CAS_{10}	M11	A_0
B3	$DDEL_1$	E1	S_{11}	K1	S_2	M12	$ADEL_2$
B4	D_0	E2	S_{12}	K2	S_1	M13	$ADEL_1$
B5	D_3	E3	GND	K3	$\overline{SWAP}$	N1	$BDEL_1$
B6	D_6	E11	FT	K11	$ADEL_0$	N2	$\overline{ENB}$
B7	D_9	E12	CAS_0	K12	CAS_{14}	N3	B_2
B8	D_{11}	E13	CAS_1	K13	CAS_{12}	N4	B_5
B9	C_{10}	F1	S_9	L1	S_0	N5	B_7
B10	C_7	F2	S_{10}	L2	$BDEL_0$	N6	B_9
B11	C_5	F3	V_{DD}	L3	$BDEL_2$	N7	B_{11}
B12	C_2	F11	CAS_2	L4	B_0	N8	A_{11}
B13	$CDEL_2$	F12	CAS_3	L5	B_4	N9	A_8
C1	S_{15}	F13	CAS_4	L6	GND	N10	A_6
C2	RND	G1	S_7	L7	V_{DD}	N11	A_3
C3	CLK	G2	S_8	L8	A_9	N12	A_2
C4	$DDEL_2$	G3	GND	L9	A_5	N13	$\overline{ENA}$

Pin Descriptions

Pin Name	Pin Number PGA	Pin Number MQFP	Pin Function Description
Power			
V_{DD}	F3, H3, L7, C8	12, 20, 46, 102	**Supply Voltage.** The TMC2249A operates from a single +5V supply. All power and ground pins must be connected.
GND	E3, G3, J3, L6, H11, C7	8, 16, 24, 42, 72, 106	**Ground.** The TMC2249A operates from a single +5V supply. All power and ground pins must be connected.
Clock			
CLK	C3	1	**System Clock.** The TMC2249A operates from a single master clock input. The rising edge of clock strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.
Inputs			
A_{11-0}	N8, M8, L8, N9, M9, N10, L9, M10, N11, N12, L10, M11	48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59	**A-D Input.** A through D are the four 12-bit registered data input ports. A_0-D_0 are the LSBs (see Table 1). Data presented to the input ports is clocked in to the top of the 16-stage delay pipeline on the next clock when enabled, "pushing" data down the register stack.
B_{11-0}	N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, L4	47, 45, 44, 43, 41, 40, 39, 38, 37, 36, 35, 34	
C_{11-0}	A9, B9, A10, C9, B10, A11, B11, C10, A12, B12, C11, A13	101, 100, 99, 98, 97, 96, 95, 94, 93, 92, 91, 90	
D_{11-0}	B8, A8, B7, A7, A6, B6, C6, A5, B5, A4, C5, B4	103, 104, 105, 107, 108, 109, 110, 111, 112 113, 114, 115	
$ADEL_{3-0}$	L11, M12, M13, K11	61, 62, 63, 64	**A-D Delay.** ADEL through DDEL are the four-bit registered input data pipe delay select word inputs. Data to be presented to the multipliers is selected from one of sixteen stages in the input data delay pipe registers, as indicated by the delay select word presented to the respective input port during that clock. The minimum delay is one clock (select word=0000), and the maximum delay is 16 clocks (select word=1111). Following powerup these values are indeterminate and must be initialized by the user.
$BDEL_{3-0}$	M2, L3, N1, L2	32, 31, 30, 29	
$CDEL_{3-0}$	D11, B13, C13, D12	88, 87, 86, 85	
$DDEL_{3-0}$	A2, C4, B3, A1	117, 118, 119, 120	
CAS_{15-0}	L13, K12, J11, K13, J12, J13, H12, H13, G12, G11, G13, F13, F12, F11, E13, E12	66, 67, 68, 69, 70, 71, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82	**Cascade Input.** CAS is the 16-bit Cascade data input port. CAS_0 is the LSB. See Table 1.
Controls			
S_{15-0}	C1, D2, D1, E2, E1, F2, F1, G2, G1, H1, H2, J1, J2, K1, K2, L1	6, 7, 9, 10, 11, 13, 14, 15, 17, 18, 19, 21, 22, 23, 25, 26	**Sum Output.** The current 16-bit result is available at the Sum output. The output may be the most or least significant 16 bits of the current accumulator output, as determined by $\overline{SWAP}$. S_0 is the LSB. See Table 1.

Pin Descriptions (continued)

Pin Name	Pin Number PGA	Pin Number MQFP	Pin Function Description
Controls			
$\overline{ENA}$-$\overline{END}$	N13, N2, C12, A3	60, 33, 89, 116	**Input Enables.** Input data presented to port i11-0 (i=A,B,C, or D) are latched into delay pipeline i, and data already in pipeline i advance by one register position, on each rising edge of CLK for which $\overline{ENi}$ is LOW. When $\overline{ENi}$ is HIGH, the data in pipeline i do not move and the value at the input port i will be lost before it reaches the multiplier.
NEG1,2	B1, D3	3, 4	**Negate.** The products of the multipliers are negated causing a subtraction to be performed during the internal summation of products, when the NEGate controls are HIGH, NEG1 negates the product A x B, while NEG2 acts on the output of the multiplier which generates the product C x D. When the length controls ADEL–DDEL are set to zero, these controls indicate the operation to be performed on data input during the same clock. As nonzero values for ADEL–DDEL do not affect the pipelining of these controls, their effect is not synchronous with the data input in these cases.
RND	C2	5	**Round.** When the rounding control is HIGH, the 24-bit sum of products resulting from data input during that clock is rounded to 16 bits. When enabled rounding is automatically performed only during the first cycle of each accumulation sequence, to avoid the accumulation of roundoff errors.
FT	E11	84	**Feedthrough.** When the Feedthrough control is HIGH, the pipeline delay through the cascade data path is minimized to simplify the cascading of multiple devices. When FT is LOW and ADEL through DDEL are all set to 0, the data inputs are aligned, such that S(n+6) = CAS(n) + A(n)B(n) + C(n)D(n). See Table 2.
$\overline{CASEN}$	D13	83	**Cascade Enable.** Data presented at the cascade data input port are latched and accumulated internally when the input enable $\overline{CASEN}$ during that clock is LOW. When $\overline{CASEN}$ is HIGH, the cascade input port is ignored.
ACC	B2	2	**Accumulate.** When the registered ACCumulator control is LOW, no internal accumulation will be performed on the data input during the current clock, effectively clearing the prior accumulated sum. When ACC is HIGH, the internal accumulator adds the emerging product to the sum of the previous products and RND is disabled.
$\overline{SWAP}$	K3	28	**Swap Output Words.** The user may access both the most and least-significant 16 bits of the 24-bit accumulator by utilizing $\overline{SWAP}$. Normal operation of the device, with $\overline{SWAP}$ = HIGH, outputs the most significant word. Setting $\overline{SWAP}$ = LOW puts a double-register structure into "toggle" mode, allowing the user to examine the LSW on alternate clocks. New output data will not be clocked into the output registers until $\overline{SWAP}$ returns HIGH.
$\overline{OE}$	M1	27	**Output Enable.** Data currently in the output registers is available at the output bus $S_{15\text{-}0}$ when the asynchronous Output Enable is LOW. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state.
No Connect			
	L12	65	Do Not Connect
	D4		Index Pin (optional)

Table 1. Data Formats and Bit Weighting

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
				-2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	DATA (A_{11-0}-D_{11-0})
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	CASCADE INPUT (CAS_{15-0})
																SUM (S_{15-0})
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	LSW
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	MSW

Notes: A minus sign indicates the two's complement sign bit.
RND adds 1 to the 2^7 position if ACC is low.

Equivalent Circuits and Threshold Levels

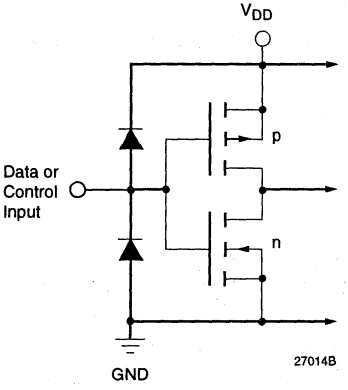


Figure 1. Equivalent Digital Input Circuit

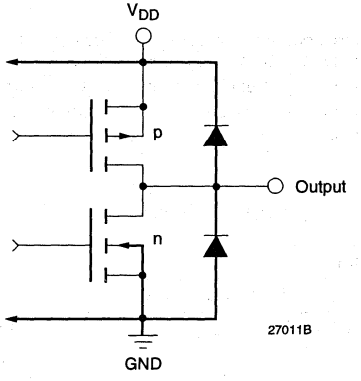


Figure 2. Equivalent Digital Output Circuit

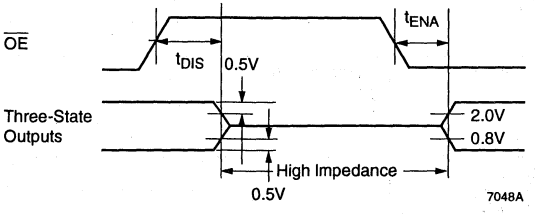


Figure 3. Threshold Levels for Three-State Measurement

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Max	Unit
Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	V_{DD} + 0.5	V
Applied Voltage (Output) [2]	-0.5	V_{DD} + 0.5	V
Externally Forced Current (Output) [3,4]	-3.0	6.0	mA
Output Short Circuit Duration (single output in HIGH state to ground)		1	sec
Operating, Ambient Temperature	-20	110	°C
Operating, Junction Temperature		140	°C
Storage Temperature	-65	150	°C
Lead, Soldering (10 seconds)		300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2249A			25	MHz
		TMC2249A-1			40	MHz
		TMC2249A-2			60	MHz
t_{PWH}	CLK pulse width, HIGH		6			ns
t_{PWL}	CLK pulse width, LOW		7			ns
t_S	Input Data Set-up Time		6			ns
t_H	Input Data Hold Time		1.5			ns
V_{IH}	Input Voltage, Logic HIGH	Data Inputs	2.0			V
		CLK Input	2.2			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

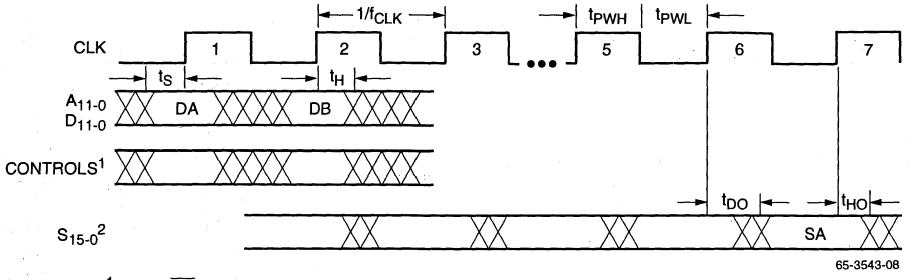
Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Total Power Supply Current	V_{DD} = Max, C_{LOAD} = 25pF, f_{CLK} = Max				
		TMC2249A			75	mA
		TMC2249A-1			105	mA
		TMC2249A-2			145	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = HIGH, f_{CLK} = Max				
		TMC2249A			68	mA
		TMC2249A-1			92	mA
		TMC2249A-2			124	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	S_{15-0}, I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	S_{15-0}, I_{OL} = Max			0.4	V

Switching Characteristics

Parameter		Conditions[1]	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			14	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	2.5			ns
t_{ENA}	Three-State Output Enable Delay	C_{LOAD} = 0 pF			12	ns
t_{DIS}	Three-State Output Disable Delay	C_{LOAD} = 0 pF			12	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS}.



[1]Except $\overline{OE}$.
[2]Assumes $\overline{OE}$ = LOW and ADEL-DDEL set to 0.

Figure 4. Timing Diagram

Application Notes

The TMC2249A is a flexible signal and image processing building block with numerous user-selectable functions which expand its usefulness. Table 2 clarifies the operation of the device, demonstrating the various feature available to the user and the timing delays incurred.

Table 2. TMC2249A Operation Sequence

CLK	ADEL	A_{11-0}	BDEL	B_{11-0}	CDEL	C_{11-0}	DDEL	D_{11-0}	NEG1	NEG2	CAS_{15-0}	FT	ACC	RND	$\overline{SWAP}$	S_{15-0}
1	0	A(1)	0	B(1)	0	C(1)	0	D(1)	L	L	0	L	L	H	H	—
2	0	A(2)	0	B(2)	0	C(2)	0	D(2)	L	H	0	L	L	H	H	—
3	0	A(3)	0	B(3)	0	C(3)	0	D(3)	H	L	0	L	L	L	H	—
4	0	A(4)	0	B(4)	0	C(4)	0	D(4)	L	L	CAS(4)	L	L	L	H	—
5	0	A(5)	0	B(5)	0	C(5)	0	D(5)	L	L	0	L	L	L	H	—
6	0	A(6)	0	B(6)	0	C(6)	0	D(6)	L	L	0	L	L	H	H	$(A(1) \times B(1)+C(1) \times D(1)+2^7)_{ms}$
7	0	A(7)	0	B(7)	0	C(7)	0	D(7)	L	L	0	L	H	X	H	$(A(2) \times B(2)-C(2) \times D(2)+2^7)_{ms}$
8	0	A(8)	0	B(8)	0	C(8)	0	D(8)	L	L	CAS(8)	H	L	L	L	$(-A(3) \times B(3)+C(3) \times D(3))_{ms}$
9	0	A(9)	0	B(9)	0	C(9)	0	D(9)	L	L	0	L	L	H	H	$(A(4) \times B(4)+C(4) \times D(4)+CAS(4))_{ms}$
10																$(A(5) \times B(5)+C(5) \times D(5)+CAS(8))_{ms}$
11																$(A(6) \times B(6)+C(6) \times D(6)+2^7)_{ms}$
12																$(A(7) \times B(7)+C(7) \times D(7)+S(11))_{ms}$
13																$(S(12))_{ls}$
14																$(A(9) \times B(8)+C(7) \times D(6)+2^7)_{ms}$

$\overline{CASEN}$ = 0, H=HIGH, L=LOW, "ms" indicates most significant output word (bits 23-8), "ls" indicates least significant word (bits 15-0). The appropriate enables for the indicated data are assumed, otherwise '-' indicates that port not enabled. Note that the output data summations including A(8)-D(8) is lost, since the output on cycle 13 is swapped to the LSW of S(12) on cycle 8. In general, RND may be left high unless the ls output is to be used, as on line 8 above.

Digital Filtering

The input structure of the TMC2249A demonstrates great versatility when all four multiplier inputs and the programmable delay registers are utilized.

Table 3 and Table 4 illlustrate how a direct-form symmetric FIR filter of up to 32 taps can be implemented. By utilizing the four input delay registers as pipelined storage banks, the user can store up to 32 coefficient-data word pairs, split into alternate "even" and "odd" halves. Two taps of the filter are calculated on each clock, and the user then increments/decrements the delay words (ADEL-DDEL). The sums of products are successively added to the global sum in the internal accumulator.

Table 3. FIR Filtering with the TMC2249A — Initial Data Loading

Register Position (Hex)	Even Data A	Odd Data C	Coefficient B	Storage D
0	x(31)	x(30)	h(0)	h(1)
1	x(29)	x(28)	h(2)	h(3)
2	x(27)	x(26)	h(4)	h(5)
3	x(25)	x(24)	h(6)	h(7)
4	x(23)	x(22)	h(8)	h(9)
5	x(21)	x(20)	h(10)	h(11)
6	x(19)	x(18)	h(12)	h(13)
7	x(17)	x(16)	h(14)	h(15)
8	x(15)	x(14)	h(15)	h(14)
9	x(13)	x(12)	h(13)	h(12)
A	x(11)	x(10)	h(11)	h(10)
B	x(9)	x(8)	h(9)	h(8)
C	x(7)	x(6)	h(7)	h(6)
D	x(5)	x(4)	h(5)	h(4)
E	x(3)	x(2)	h(3)	h(2)
F	x(1)	x(0)	h(1)	h(0)

Once all of the products of the desired taps have been summed, the result is available at the output. The user then "pushes" a new time-data sample on to the appropriate even or odd data register "stack" and reiterates the summation. Note that the coefficient bank "pointers", the BDEL and DDEL delay words, are alternately incremented and decremented on successive filter passes to maintain alignment between the incoming data samples and their respective coefficients.

The effective filter speed is calculated by dividing the clock rate by one-half the number of taps implemented.

Alternatively, non-symmetric FIR filters can be implemented using the TMC2249A in a similar fashion. Here, a shift register is used to delay the incoming data fed to the A input by an amount equal to one-half the length of the filter (the length of the A delay register).

As shown in Figure 5, the data is then sent to the C input, thus "stacking" the A and C delay registers to create a single N-tap FIR filter. The incremented delay words (ADEL-DDEL) for all four inputs are identical. Again, the filter throughput is equal to the clock speed divided by one-half the number of taps implemented.

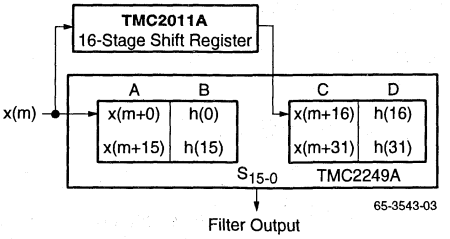


Figure 5. Non-Symmetric 32-Tap FIR Filtering Using the TMC2249A

Table 4. FIR Filtering – Operation Sequence

Cycle	Push A	B	Push C	D	ADEL	CDEL	BDEL	DDEL	ACC	ENA	ENB	ENC	END	Convolutional Sum	Resultant Output
1	–	–	–	–	0	0	0	0	L	H	H	H	H	x(31)•h(0)+x(30)•h(1)	
2	–	–	–	–	1	1	1	1	H	H	H	H	H	+x(29)•h(2)+x(28)•h(3)	
3	–	–	–	–	2	2	2	2	H	H	H	H	H	+x(27)•h(4)+x(26)•h(5)	
4	–	–	–	–	3	3	3	3	H	H	H	H	H	+x(25)•h(6)+x(24)•h(7)	
5	–	–	–	–	4	4	4	4	H	H	H	H	H	+x(23)•h(8)+x(22)•h(9)	
6	–	–	–	–	5	5	5	5	H	H	H	H	H	+x(21)•h(10)+x(20)•h(11)	
7	–	–	–	–	6	6	6	6	H	H	H	H	H	+x(19)•h(12)+x(18)•h(13)	
8	–	–	–	–	7	7	7	7	H	H	H	H	H	+x(17)•h(14)+x(16)•h(15)	
9	–	–	–	–	8	8	8	8	H	H	H	H	H	+x(15)•h(15)+x(14)•h(14)	
10	–	–	–	–	9	9	9	9	H	H	H	H	H	+x(13)•h(13)+x(12)•h(12)	
11	–	–	–	–	A	A	A	A	H	H	H	H	H	+x(11)•h(11)+x(10)•h(10)	
12	–	–	–	–	B	B	B	B	H	H	H	H	H	+x(9)•h(9)+x(8)•h(8)	See Note 2
13	–	–	–	–	C	C	C	C	H	H	H	H	H	+x(7)•h(7)+x(6)•h(6)	
14	–	–	–	–	D	D	D	D	H	H	H	H	H	+x(5)•h(5)+x(4)•h(4)	
15	–	–	–	–	E	E	E	E	H	H	H	H	H	+x(3)•h(3)+x(2)•h(2)	
16	–	–	x(32)	–	F	F	F	F	H	H	H	L	H	+x(1)•h(1)+x(0)•h(0)	
17	–	–	–	–	0	0	F	F	H	H	H	H	H	+x(31)•h(1)+x(32)•h(0)	
18	–	–	–	–	1	1	E	E	H	H	H	H	H	+x(29)•h(3)+x(30)•h(2)	
19	–	–	–	–	2	2	D	D	H	H	H	H	H	+x(27)•h(5)+x(28)•h(4)	
20	–	–	–	–	3	3	C	C	H	H	H	H	H	+x(25)•h(7)+x(26)•h(6)	
21	–	–	–	–	4	4	B	B	H	H	H	H	H	+x(23)•h(9)+x(24)•h(8)	
•															
•															

Notes:

1. If only the 16 MSBs of the result are used, the user may leave RND HIGH and $\overline{SWAP}$ low. If the 16 LSBs or all 24 bits of the result are used, then RND should be set low.
2. $s = \sum_{K=0}^{15} (x(k)\,h(k) + x(k+16)\,h(k))$

Complex Arithmetic Functions

The TMC2249A can also be used to perform complex arithmetic functions. The basic function performed by the device, ignoring the delay controls,

$$SUM = (\pm A \bullet B) + (\pm C \bullet D)$$

can realize in two steps the familiar summation:

$$(P+jR)(S+jT)=(PS-RT) + j(PT+SR)$$
$$(1) \quad (2)$$

by loading the TMC2249A as follows:

	TMC2249A Inputs						Resultant
Step	A	B	C	D	NEG1	NEG2	Output
1	P	S	R	T	L	H	(PS-RT)
2	P	T	R	S	L	L	(PT+SR)

where H and L indicate a logic HIGH and LOW.

Thus we can perform a complex multiplication in two clock cycles. Notice that the user must switch the two components of the second input vector between the B and D inputs to obtain the second complex summation.

Calculating a Butterfly

Taking advantage of the complex multiply which we implemented above using the TMC2249A, we can expand slightly to calculate a Radix-2 Butterfly, the core of the Fast Fourier Transform algorithm. To review, the Butterfly is calculated as shown in Figure 6.

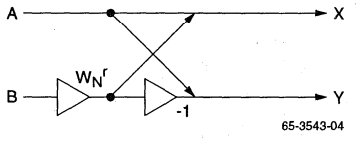


Figure 6. Signal Flow of Radix-2 Butterfly

Where

$$X=A+B(W_N^r)$$
$$Y=A-B(W_N^r),$$

and W_N^r is the complex phase coefficient, or "twiddle factor" for the N-point transform, which is:

$$W_N^r = e^{j(2\pi/N)}$$
$$= \cos(2\pi/N) + j(\sin(2\pi/N))$$
$$= Re(W) + jIm(W)$$

with Re and Im indicating the real and imaginary parts of the vector.

Expanding the complex vectors A and B to calculate X and Y, we get:

$$X = (Re(A)+jIm(A))+(Re(B)Re(W)-Im(B)Im(W)+j(Re(B)Im(W)+Im(B)Re(W)))$$
$$= (Re(A)+Re(B)Re(W)-Im(B)Im(W)) +j(Im(A)+Re(B)Im(W)+Im(B)Re(W))$$
$$= Re(X)+jIm(X)$$

and,

$$Y = (Re(A)+jIm(A))-(Re(B)Re(W)-Im(B)Im(W)+j(Re(B)Im(W)+Im(B)Re(W)))$$
$$= (Re(A)-Re(B)Re(W)+Im(B)Im(W)) +j(Im(A)-Re(B)Im(W)-Im(B)Re(W))$$
$$= Re(Y)+jIm(Y)$$

The butterfly is then neatly implemented in four clocks, as follows:

	TMC2249A Inputs							Resultant
Step	A	B	C	D	CAS Input	NEG1	NEG2	Output
1	Re(B)	Re(W)	Im(B)	Im(W)	Re(A)	L	H	Re(X)
2	Re(B)	Re(W)	Im(B)	Im(W)	Re(A)	H	L	Re(Y)
3	Re(B)	Im(W)	Im(B)	Re(W)	Im(A)	L	L	Im(X)
4	Re(B)	Im(W)	Im(B)	Re(W)	Im(A)	H	H	Im(Y)

Notice again that the components of the second vector must be switched by the user on the second half of the computation, as well as the parts of the vector presented to the cascade input.

Quadrature Modulation

The TMC2249A can also be used to advantage as a digital-domain complex frequency synthesizer, as demonstrated in Figure 7.

Here, orthogonal sinusoidal waveforms are generated digitally in the TMC2330A Coordinate Transformer. These quadrature phase coefficients are then multiplied with two input signals, such as digitized analog data.

The TMC2249A then adds these products, which can be output directly to a high-speed digital-to-analog converter such as the Raytheon TDC1012 for direct waveform synthesis. This 12-bit, 20MHz DAC is ideally suited to waveform generation, featuring extremely low glitch energy for low spurious harmonics and distortion.

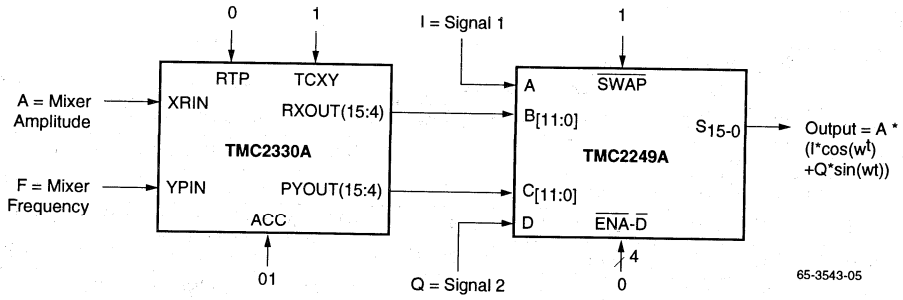


Figure 7. Direct Quadrature Waveform Synthesizer using the TMC2249A and TMC2330A

Related Products

- TMC2301 Image Resampling Sequencer
- TMC2302 Image Manipulation Sequencer
- TMC2246A Image Filter
- TMC2242B Half–Band Filter

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2249AH5C	0°C to 70°C	25 MHz	Commercial	120 Pin Plastic Pin Grid Array	2249AH5C
TMC2249AH5C1	0°C to 70°C	40 MHz	Commercial	120 Pin Plastic Pin Grid Array	2249AH5C1
TMC2249AH5C2	0°C to 70°C	60 MHz	Commercial	120 Pin Plastic Pin Grid Array	2249AH5C2
TMC2249AKEC	0°C to 70°C	25 MHz	Commercial	120 Lead Metric Quad Flat Pack	2249AKEC
TMC2249AKEC1	0°C to 70°C	40 MHz	Commercial	120 Lead Metric Quad Flat Pack	2249AKEC1
TMC2249AKEC2	0°C to 70°C	60 MHz	Commercial	120 Lead Metric Quad Flat Pack	2249AKEC2

TMC2250A

Matrix Multiplier

12 x 10 bit, 50 MHz

Features

- Four user-selectable filtering and transformation functions:
  - Triple dot product (3 x 3) matrix multiply
  - Cascadeable 9-tap systolic FIR filter
  - Cascadeable 3 x 3-pixel image convolver
  - Cascadeable 4 x 2-pixel image convolver
- 50 MHz (20ns) pipelined throughput
- 12-bit input and output data, 10-bit coefficients
- 6-bit cascade input and output ports in all filter modes
- Onboard coefficient storage, with three-cycle updating of all nine coefficients

Applications

- Image filtering and manipulation
- Video effects generation
- Video standards conversion and encoding/decoding
- Three-dimensional image manipulation
- Medical image processing
- Edge detection for object recognition
- FIR filtering for communications systems

Description

The TMC2250A is a flexible high-performance nine-multiplier array VLSI circuit which can execute a cascadeable 9-tap FIR filter, a cascadeable 4 x 2 or 3 x 3-pixel image convolution, or a 3 x 3 color space conversion. All configurations offer throughput at up to the maximum guaranteed 50 MHz clock rate with 12-bit data and 10-bit coefficients. All inputs and outputs are registered on the rising edges of the clock.

The 3 x 3 matrix multiply or color conversion configuration can perform video standard conversion (YIQ or YUV to RGB, etc.) or three-dimensional perspective translation at real-time video rates.

The 9-tap FIR filter configuration, useful in Video, Telecommunications, and Signal Processing, features a 16-bit cascade input to allow construction of longer filters.

The cascadeable 3 x 3 and 4 x 2-pixel image convolver functions allow the user to perform numerous image processing functions, including static filters and edge detectors. The 16-bit cascade input port facilitates two-chip 50 MHz cubic convolution (4 x 4-pixel kernel).

The TMC2250A is fabricated in a sub-micron CMOS process and operates at clock speeds of up to 50 MHz over the full commercial (0°C to 70°C) temperature and supply voltage ranges. It is available in 121-pin plastic pin grid array (PGA) packages as well as a 120-lead plastic quad flatpack (PQFP). All input and output signals are TTL compatible.

Functional Description

The TMC2250A is a nine-multiplier array with the internal bus structure and summing adders needed to implement a 3 x 3 matrix multiplier (triple dot product) a cascadeable 9-tap FIR filter, a 3 x 3-pixel convolver, or a 4 x 2-pixel convolver all in one monolithic circuit. With a 50MHz guaranteed maximum clock rate, this device offers video and imaging system designers a single-chip solution to numerous common image and signal-processing problems.

The three data input ports (A, B, C) accept 12-bit two's complement integer data, which is also the format for the output ports (X, Y, Z) in the matrix multiply mode (Mode 00). In the filter configurations (Modes 01, 10, and 11) the cascade ports assume 12-bit integer, 4-bit fractional two's complement data on both input and output. The coefficient input ports (KA, KB, KC) are always 10-bit two's complement fractional. Table 1 details the bit weighting of the input and output data in all configurations.

Operating Modes

The TMC2250A can implement four different digital filter architectures. Upon selection of the desired function by the user ($MODE_{1-0}$), the device reconfigures its internal data paths and input and output buses appropriately. The output ports (XC, YC and ZC) are configured in all filter modes a 16-bit Cascade In and Cascade Out ports so that multiple devices can be connected to build larger filters. These modes are described individually below. The I/O function configurations for all four modes are shown in Table 1.

Definitions

The calculations performed by the TMC2250A in each mode are also shown below, utilizing the following notation:

A(1), B(5), C(2), CASIN(3)
Indicates the data word presented to that input port during the specified clock rising edge(x). Applies to all input ports A_{11-0}, B_{11-0}, C_{11-0}, and $CASIN_{15-0}$.

KA1(1), KB3(4)
Indicates coefficient data stored in the specified one of the nine onboard coefficient registers KA1 through KC3, as shown in the block diagram for that mode, input during or before the specified clock rising edge (x).

X(1), Y(4), Z(6), CASOUT (6)
Indicated data available at that output port t_{DO} after that specified clock rising edge (x). Applies to all output ports X_{11-0}, Y_{11-0}, Z_{11-0}, and $CASOUT_{15-0}$.

Numeric Format

Table 2 shows the binary weightings of the input and output ports of the TMC2250A. Although the internal sums of products could grow to 23 bits, in the matrix multiply mode (Mode 00) the outputs X, Y and Z are rounded to yield 12-bit integer words. Thus the output format is identical to the input data format. In the filter configurations (Modes 01, 10, and 11) the cascade output is always half-LSB rounded to 16 bits, specifically 12 integer bits and 4 fractional guard bits, with no overflow "headroom". The user is of course free to half-LSB round the output word to any size less than 16 bits by forcing a 1 into the bit position of the cascade input immediately below the desired LSB. In all modes, bit weighting is easily adjusted if desired by applying the same scaling correction factor to both input and output data words. If the coefficients are rescaled, the relative weightings of the CASIN and CASOUT ports will differ accordingly.

Data Overflow

As shown in Table 2, the TMC2250A's matched input and output data formats accommodate 0dB (unity) gain. Therefore, the user must be aware of input conditions that could lead to numeric overflow. Maximum input data and coefficient word sizes must be taken into account with the specific algorithm performed to ensure that no overflow occurs.

Table 1. Data Port Formatting by Mode

	Inputs						Inputs/Output		Outputs		
Mode	**A_{11-0}**	**B_{11-0}**	**C_{11-0}**	**KA_{9-0}**	**KB_{9-0}**	**KC_{9-0}**	**XC_{11-0}**	**YC_{11-8}**	**Y_{7-4}**	**YC_{3-0}**	**ZC_{11-0}**
00	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	X_{11-0}	Y_{11-8}	Y_{7-4}	Y_{3-0}	Z_{11-0}
01	A_{11-0}	B_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
10	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
11	A_{11-0}	B_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$

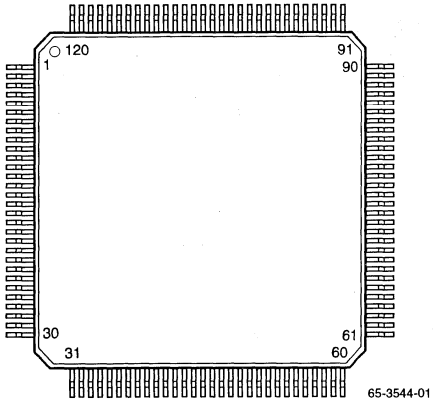
Table 2. Bit Weightings for Input and Output Data Words

Bit Weights	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}
Inputs																						
All Modes Data A, B, C	$-I_{11}$	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	.									
Coefficients KA, KB, KC												$-K_9$	.	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0
Modes 01, 10, 11 CASIN	$-CI_{15}$	CI_{14}	CI_{13}	CI_{12}	CI_{11}	CI_{10}	CI_9	CI_8	CI_7	CI_6	CI_5	CI_4	.	CI_3	CI_2	CI_1	CI_0					
Internal Sum	X_{20}	X_{19}	X_{18}	X_{17}	X_{16}	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	.	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
Outputs																						
Mode 00 X, Y, Z	$-O_{11}$	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	.									
Modes 01, 10, 11 CASOUT	$-CO_{15}$	CO_{14}	CO_{13}	CO_{12}	CO_{11}	CO_{10}	CO_9	CO_8	CO_7	CO_6	CO_5	CO_4	.	CO_3	CO_2	CO_1	CO_0					

Note: A minus sign indicates a two's complement sign bit.

Pin Assignments

120 Pin Plastic Quad Flat Pack (MQFP), KE Package

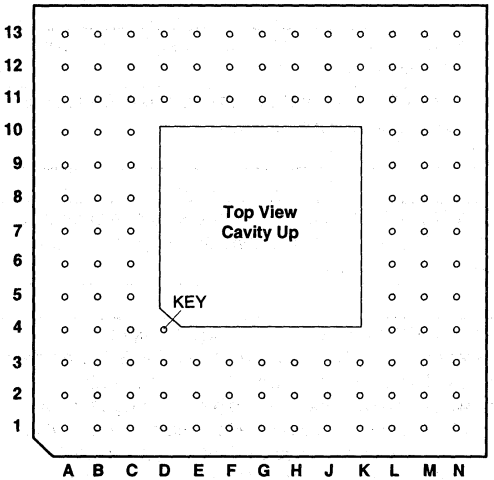


65-3544-01

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	XC_6	31	ZC_6	61	KA_1	91	B_5
2	XC_5	32	ZC_7	62	KA_2	92	B_6
3	XC_4	33	ZC_8	63	KA_3	93	B_7
4	XC_3	34	GND	64	KA_4	94	B_8
5	XC_2	35	ZC_9	65	KA_5	95	B_9
6	XC_1	36	ZC_{10}	66	KA_6	96	B_{10}
7	XC_0	37	ZC_{11}	67	KA_7	97	B_{11}
8	GND	38	KC_0	68	KA_8	98	C_0
9	YC_{11}	39	KC_1	69	KA_9	99	C_1
10	YC_{10}	40	KC_2	70	CWE_1	100	C_2
11	YC_9	41	KC_3	71	CWE_0	101	C_3
12	V_{DD}	42	GND	72	GND	102	V_{DD}
13	YC_8	43	KC_4	73	A_0	103	C_4
14	Y_7	44	KC_5	74	A_1	104	C_5
15	Y_6	45	KC_6	75	A_2	105	C_6
16	GND	46	V_{DD}	76	A_3	106	GND
17	Y_5	47	KC_7	77	A_4	107	C_7
18	Y_4	48	KC_8	78	A_5	108	C_8
19	YC_0	49	KC_9	79	A_6	109	C_9
20	V_{DD}	50	KB_0	80	A_7	110	C_{10}
21	YC_1	51	KB_1	81	A_8	111	C_{11}
22	YC_2	52	KB_2	82	A_9	112	$MODE_1$
23	YC_3	53	KB_3	83	A_{10}	113	$MODE_0$
24	GND	54	KB_4	84	A_{11}	114	GND
25	ZC_0	55	KB_5	85	B_0	115	XC_{11}
26	ZC_1	56	KB_6	86	B_1	116	XC_{10}
27	ZC_2	57	KB_7	87	B_2	117	XC_9
28	ZC_3	58	KB_8	88	CLK	118	V_{DD}
29	ZC_4	59	KB_9	89	B_3	119	XC_8
30	ZC_5	60	KA_0	90	B_4	120	XC_7

Pin Assignments (continued)

120 Pin Plastic Grid Array, H5 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	XC_7	C5	GND	G11	A_3	L10	KB_8
A2	XC_9	C6	C_{10}	G12	A_2	L11	KA_1
A3	XC_{10}	C7	GND	G13	A_3	L12	KA_5
A4	$MODE_0$	C8	V_{DD}	H1	Y_4	L13	KA_6
A5	C_{11}	C9	C_0	H2	YC_0	M1	ZC_2
A6	C_8	C10	B_8	H3	V_{DD}	M2	ZC_7
A7	C_7	C11	B_5	H11	GND	M3	ZC_9
A8	C_5	C12	B_3	H12	A_0	M4	ZC_{11}
A9	C_3	C13	B_1	H13	A_1	M5	KC_2
A10	C_1	D1	YC_{11}	J1	YC_1	M6	KC_4
A11	B_{10}	D2	XC_0	J2	YC_2	M7	KC_6
A12	B_7	D3	XC_0	J3	GND	M8	KC_9
A13	B_4	D11	CLK	J11	KA_8	M9	KB_2
B1	XC_4	D12	B_0	J12	CWE_1	M10	KB_5
B2	XC_5	D13	A_{10}	J13	CWE_0	M11	KB_9
B3	XC_8	E1	YC_9	K1	YC_3	M12	KA_2
B4	XC_{11}	E2	YC_{10}	K2	ZC_0	M13	KA_3
B5	$MODE_1$	E3	GND	K3	ZC_3	N1	ZC_5
B6	C_9	E11	A_{11}	K11	KA_4	N2	ZC_8
B7	C_6	E12	A_9	K12	KA_7	N3	ZC_{10}
B8	C_4	E13	A_8	K13	KA_9	N4	KC_1
B9	C_2	F1	Y_7	L1	ZC_1	N5	KC_3
B10	B_{11}	F2	YC_8	L2	ZC_4	N6	KC_5
B11	B_9	F3	V_{DD}	L3	ZC_6	N7	KC_7
B12	B_6	F11	A_7	L4	GND	N8	KC_8
B13	B_2	F12	A_6	L5	KC_0	N9	KB_1
C1	XC_1	F13	A_5	L6	GND	N10	KB_3
C2	XC_2	G1	Y_5	L7	V_{DD}	N11	KB_6
C3	XC_6	G2	Y_6	L8	KB_0	N12	KB_7
C4	V_{DD}	G3	GND	L9	KB_4	N13	KA_0

Pin Descriptions

Pin Name	Pin Number PGA	Pin Number MQFP	Function	Pin Description
Power				
V_{DD}	F3, H3, L7, C8, C4	12, 20, 46, 102, 118	Supply Voltage	The TMC2250A operates from a single +5V supply. All pins must be connected.
GND	E3, G3, J3, L4, L6, H11, C7, C5	8, 16, 24, 34, 42, 72, 106, 114	Ground	The TMC2250A operates from a single +5V supply. All pins must be connected.
Clock				
CLK	D11	88	System Clock	The TMC2250A operates from a single system clock input. All timing specifications are referenced to the rising edge of clock.
Controls				
$MODE_{1,0}$	B4, A4	112, 113	Mode Control	The TMC2250A will switch to the configuration selected by the user (as shown in Table 3) on the next clock. This registered control is usually static; however, should the user wish to switch between modes, the internal pipeline latencies of the device must be taken into account. Valid data will not be available at the outputs in the new configuration until enough clocks in the new mode have passed to flush the internal registers.
$CWE_{1,0}$	J12, J13	70, 71	Coefficient Write Enable	Data presented to the coefficient input ports (KA, KB, and KC) will update three of the internal coefficient storage registers, as indicated by the simultaneous Coefficient Write Enable select, on the next clock. See Table 4 and the Functional Block Diagram.
Input/Output				
A_{11-0}	E11, D13, E12, E13, F11, F12, F13, G13, G11, G12, H13, H12	84, 83, 82, 81, 80, 79, 78, 77, 76, 75, 74, 73	Data Input A	Data presented to the 12-bit registered data input ports A, B, and C are latched into the multiplier input registers for the currently selected configuration (Table 3). In all modes except Mode 00, new data are internally right-shifted to the next filter tap on each rising edge of CLK.
B_{11-0}	B10, A11, B11, C10, A12, B12, C11, A13, C12, B13, C13, D12	97, 96, 95, 94, 93, 92, 91, 90, 89, 87, 86, 85	Data Input B	
C_{11-0}	A5, C6, B6, A6, A7, B7, A8, B8, A9, B9, A10, C9	111, 110, 109, 108, 107, 105, 104, 103, 101, 100, 99, 98	Data Input C	

Pin Descriptions (continued)

Pin Name	Pin Number PGA	Pin Number MQFP	Function	Pin Description
KA9-0	K13, J11, K12, L13, L12, K11, M13, M12, L11, N13	69, 68, 67, 66, 65, 64, 63, 62, 61, 60	Coefficient Input A1, A2, A3	Data presented to the 10-bit registered coefficient input ports KA, KB and KC are latched three at a time into the internal coefficient storage register set indicated by the Coefficient Write Enable $CWE_{1,0}$ on the next clock, as shown in Table 4.
KB9-0	M11, L10, N12, N11, M10, L9, N10, M9, N9, L8	59, 58, 57, 56, 55, 54, 53, 52, 51, 50	Coefficient Input B1, B2, B3	
KC9-0	M8, N8, N7, M7, N6, M6, N5, M5, N4, L5	49, 48, 47, 45, 44, 43, 41, 40, 39, 38	Coefficient Input B1, B2, B3	
XC11-0	B4, A3, A2, B3, A1, C3, B2, B1, D3, C2, C1, D2	115, 116, 117, 119, 120, 1, 2, 3, 4, 5, 6, 7	CASIN15-4/ Output X	In all modes except Mode 00, the x port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Input port $CASIN_{15-0}$. Data presented to this input will be added to the weighted sums of the data words which were presented to the input ports (A, B and C).
YC11-8	D1, E2, E1, F2	9, 10, 11, 13	CASIN3-0/ Output Y11-0	
Y7-4	F1, G2, G1, H1	14, 15, 17, 18	Output7-4 only	In the matrix multiply mode, data are available at the 12-bit registered output ports X, Y AND Z t_{DO} after every clock. These ports are reconfigured in the filtering modes as 16-bit Cascade Input and Output ports.$CASOUT_{15-0}$
YC3-0	K1, J2, J1, H2	23, 22, 21, 19	CASOUT3-0/ Output Y3-0	
ZC11-0	M4, N3, M3, N2, M2, L3, N1, L2, K3, M1, L1, K2	37, 36, 35, 33, 32, 31, 30, 29, 28, 27, 26, 25	CASOUT15-4/ Output Z11-0	In all modes except Mode 00, the Z port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Output port $CASOUT_{15-0}$.

Note:

1. The output ports X, Y, Z and CASOUT, and input port CASIN are internally reconfigured by the device as required for each mode of the device. The multiple-function pins have names which are combinations of these titles, as appropriate.

Table 3. Configuration Mode Word

$MODE_{1,0}$	Configuration Mode
00	3 x 3 Matrix Multiply
01	9-Tap One Dimensional FIR
10	3 x 3 -Pixel Convolver
11	4 x 2 -Pixel Convolver

Table 4. Coefficient Write Enable Word

$CWE_{1,0}$	Coefficient Set Selected
00	Hold all registers
01	Update KA1, KB1, KC1
10	Update KA2, KB2, KC2
11	Update KA3, KB3, KC3

Table 5. Coefficient Input Ports

Input Port	Registers Available
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

3 x 3 Matrix Multiplier (Mode 00)

This mode utilizes all six input and output ports in the basic configuration to realize a "triple dot product", in which each output is the sum of all three input words in that column multiplied by the appropriate stored coefficients. The three corresponding sums of products are available at the outputs five clock cycles after the input data are latched, and three new data words half-LSB rounded to 12 bits are then available every clock cycle.

$$X(5)=A(1)KA1(1)+B(1)KB1(1)+C(1)KC1(1)$$
$$Y(5)=A(1)KA2(1)+B(1)KB2(1)+C(1)KC2(1)$$
$$Z(5)=A(1)KA3(1)+B(1)KB3(1)+C(1)KC3(1)$$

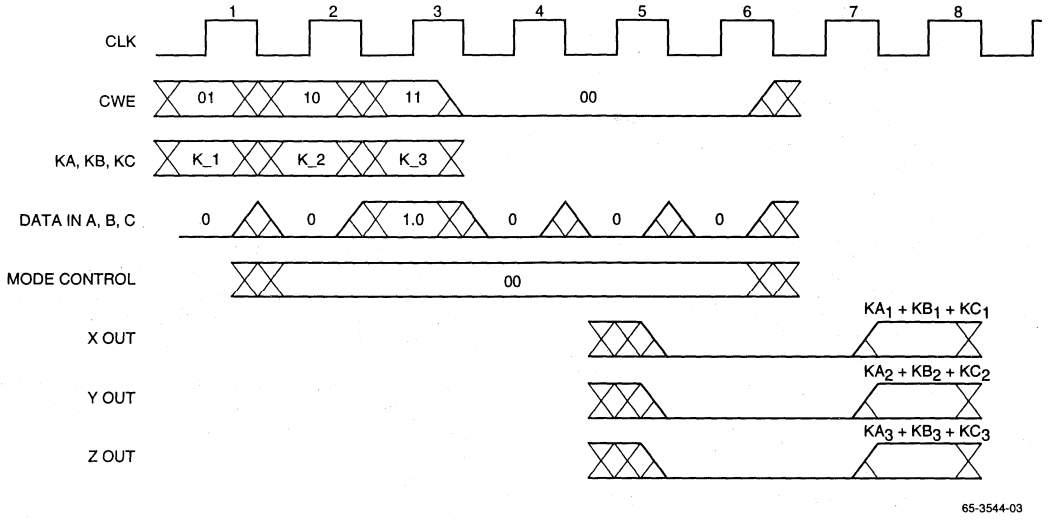


Figure 1. 3 x 3 Matrix Multiplier Impulse Response (Mode 00)

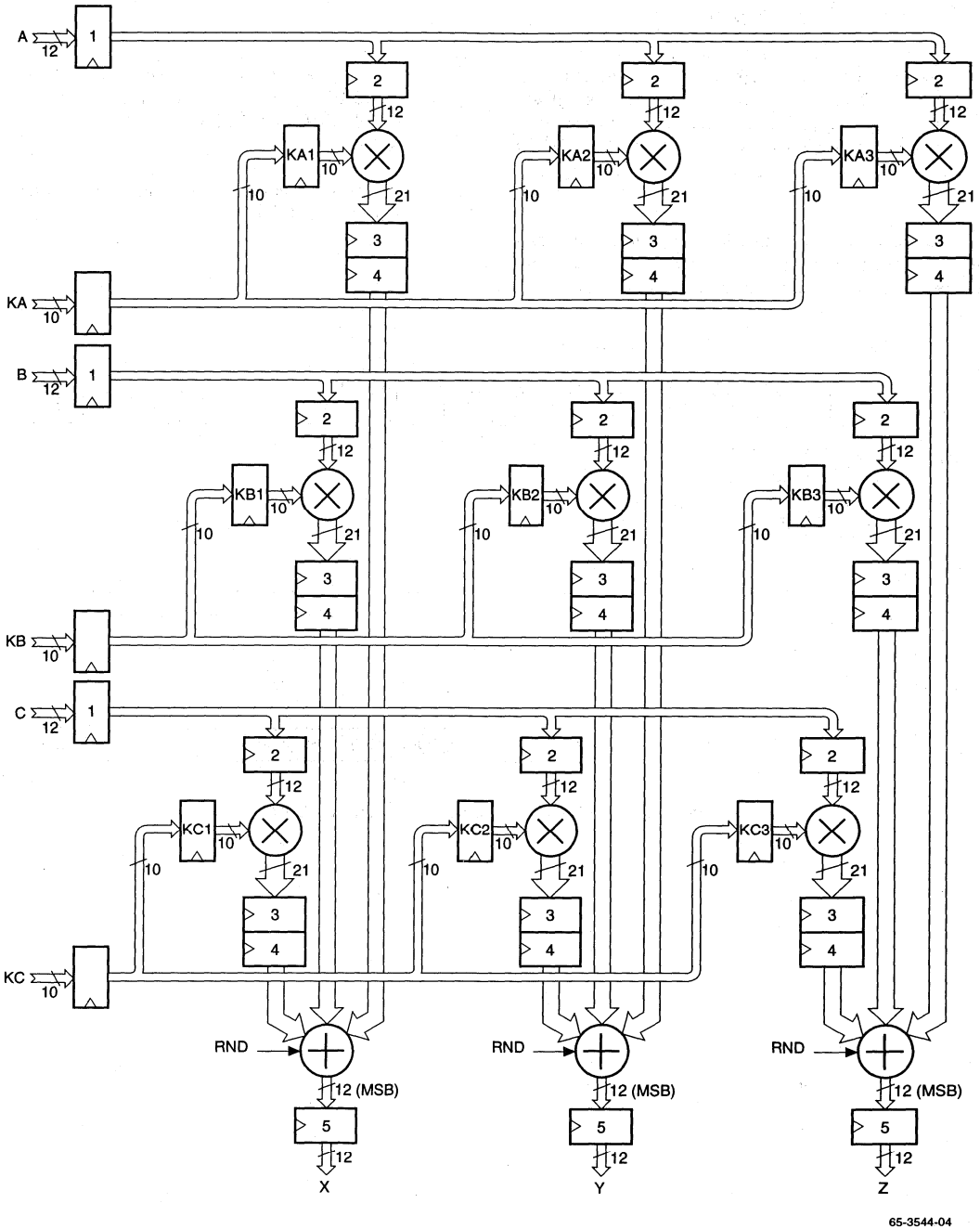


Figure 2. 3 x 3 Matrix Multiplier Configuration (Mode 00)

9-Tap FIR Filter Mode (01)

The architecture for this configuration is shown in Figure 4. The user loads the desired coefficient set, presents input data to ports A and B simultaneously (most applications will wire the A and B inputs together), and receives the resulting 9-sample response, half-LSB rounded to 16 bits, 5 to 13 clock cycles later. A new output data word is available every clock cycle.

The figure shows that the input data are automatically right-shifted by one position through the row of multiplier input registers on every clock in anticipation of a new input data word.

CASOUT(13) =
A(9)KA3(9)+A(8)KA2(8)+A(7)KA1(7)
+B(6)KB3(9)+B(5)KB2(8)+B(4)KB1(7)
+B(3)KC3(9)+B(2)KC2(8)+B(1)KC1(7)
+CASIN(10)

Latency: Impulse in to center of 9-tap response =9 registers. Cascade In to Cascade Out=4 registers.

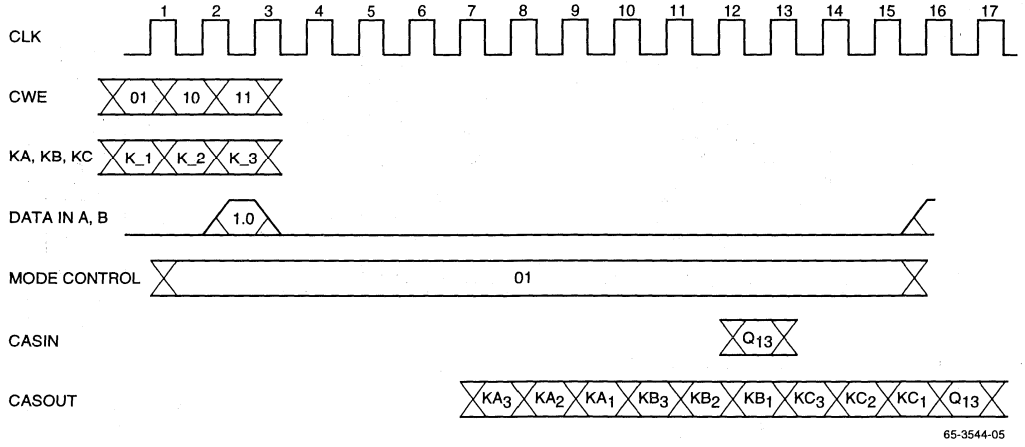


Figure 3. 9-Tap FIR Filter Impulse Response (Mode 01)

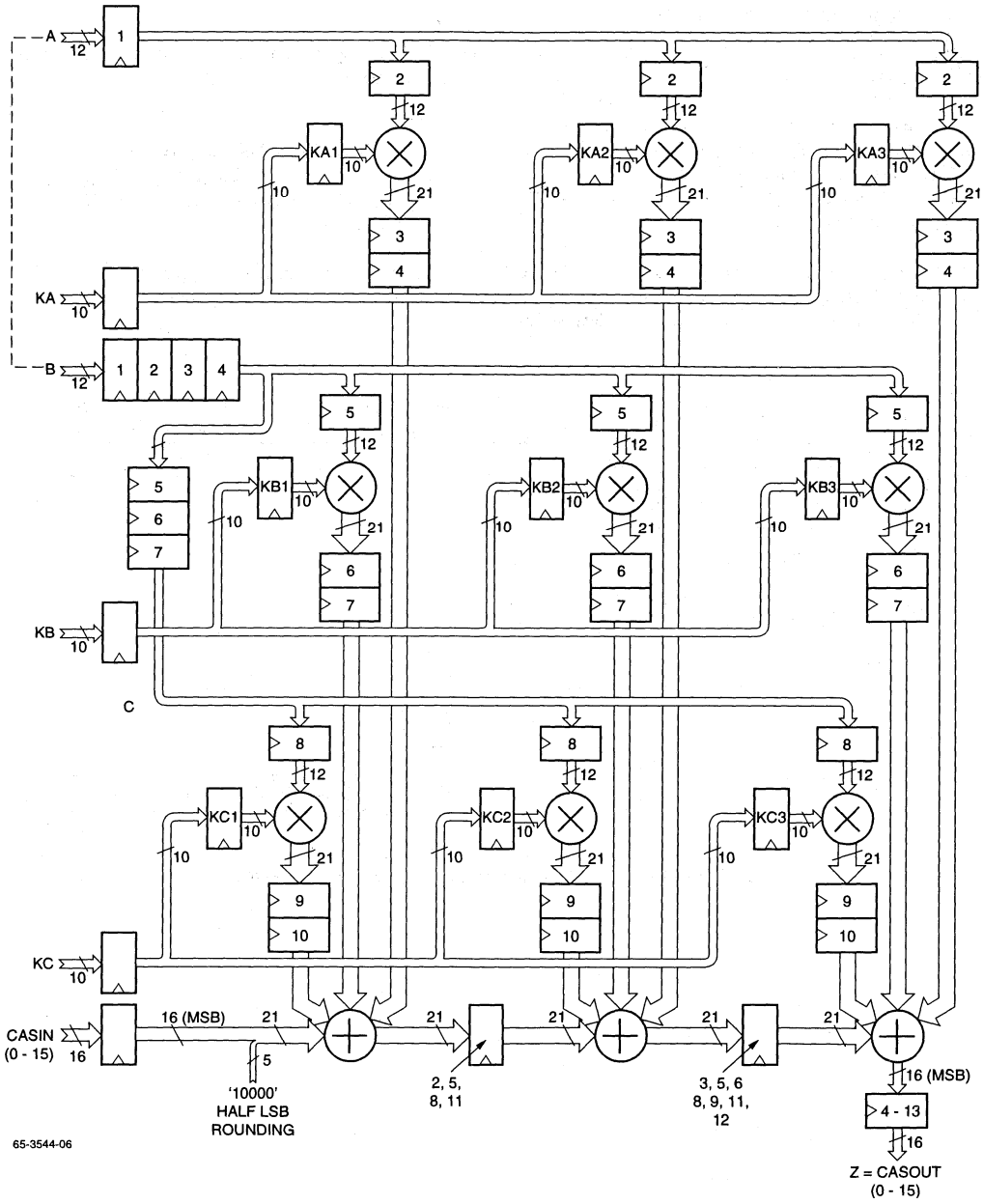


Figure 4. 9-Tap FIR Filter Configuration (Mode 01)

3 x 3 Pixel Convolver (Mode 10)

This filter configuration accepts a 3 pixel-square neighborhood, side-loaded three pixels at a time through input ports A, B and C, and multiplies the 9 most recent pixel values by the coefficient set currently stored in the registers. These products are summed with the data presented to the cascade input, and a new 3-cycle impulse response, rounded to 16 bits, is available at the output port 5 to 7 clocks later, with a new output available on every clock cycle.

The input pixel data are automatically shifted one location to the right through the three rows of multiplier input registers on every clock in anticipation of three new input data words, effectively sliding the convolutional window over one column in an image plane.

CASOUT(7)=
A(3)KA3(3)+A(2)KA2(2)+A(1)KA1(1)
+B(3)KB3(3)+B(2)KB2(2)+B(1)KB1(1)
+C(3)KC3(3)+C(2)KC2(2)+C(1)KC1(1)
+CASIN(4)

Latency: Impulse in to center of 3-tap response = 6 registers. Cascade In to Cascade Out=4 registers.

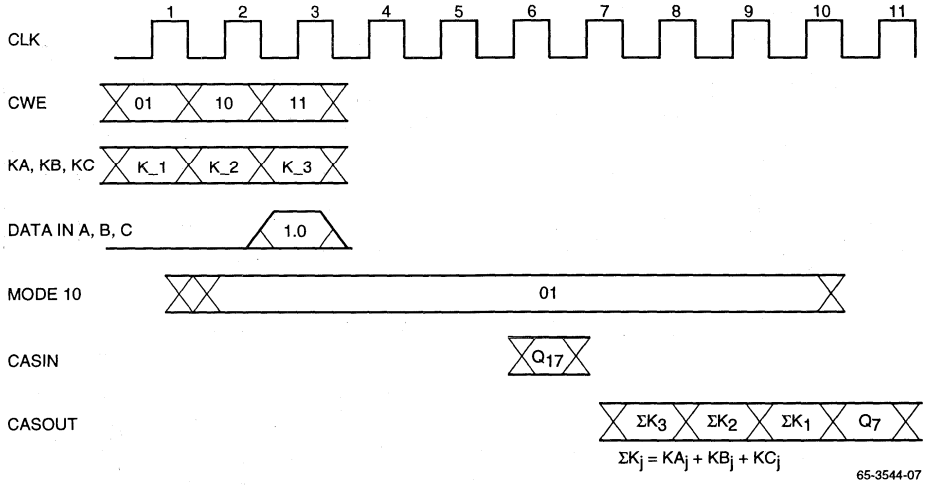


Figure 5. 3 x 3-Pixel Convolver Impulse Response (Mode 10)

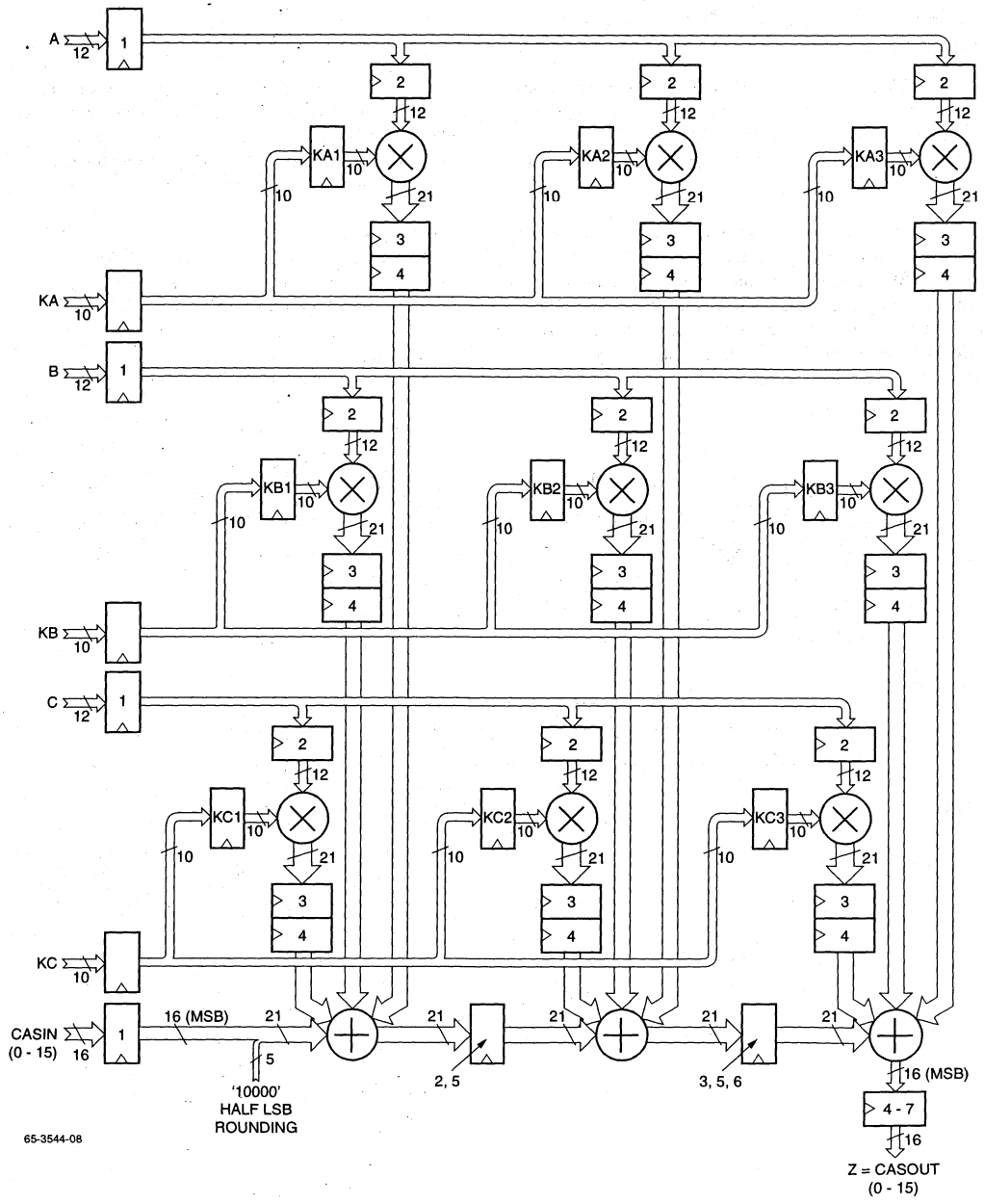


Figure 6. 3 x 3-Pixel Convolver Configuration (Mode 10)

4 x 2-Pixel Cascadeable Convolver (Mode 11)

Similar to Mode 10, the 4 x 2 -Pixel convolver allows the use to perform full-speed cubic convolution with only two TMC2250A devices and the TMC2111A Pipeline Delay Register to synchronize the cascade ports (see the Applications Discussion section).

Pixel data are side-loaded into ports A and B, multiplied by the onboard coefficients, summed with the cascade input, and half-LSB rounded to 16 bits. The four-cycle impulse response emerges at the cascade output port 5 to 8 clock cycles later. A new output word is available on every clock cycle. Note that Multiplier KC2 is not used in this mode and that its stored coefficient is ignored.

As shown below, the column of input pixel data is automatically shifted one location to the right through the two rows of multiplier input registers on every clock in anticipation of two new input data words, effectively sliding the convolutional window over one column in an image plane.

CASOUT(8)=
A(4)KA3(4)+A(3)KA2(3)+A(2)KA1(2)
+A(1)KB3(4)+B(4)KB3(4)+B(3)KB2(3)
+B(2)KB1(2)+B(1)KC1(2)+CASIN(5)

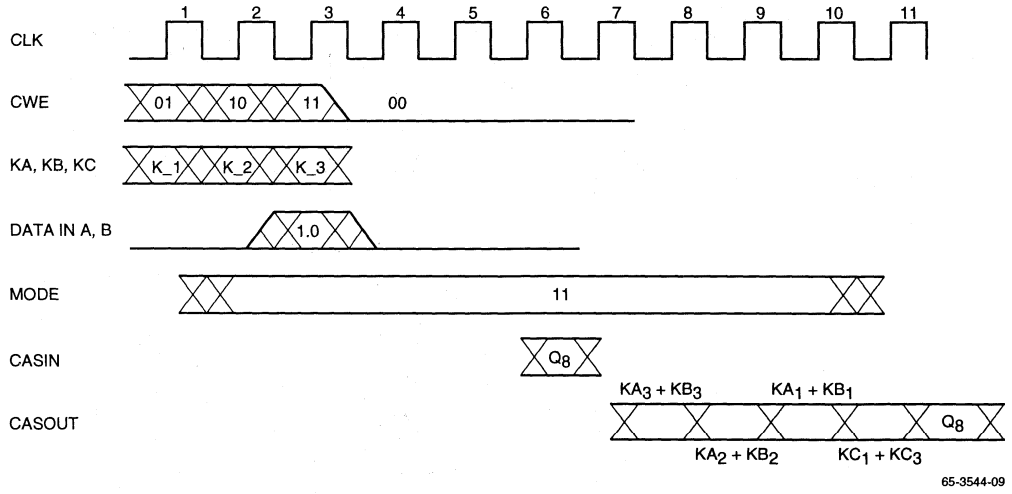


Figure 7. 4 x 2-Pixel Convolver Impulse Response (Mode 11)

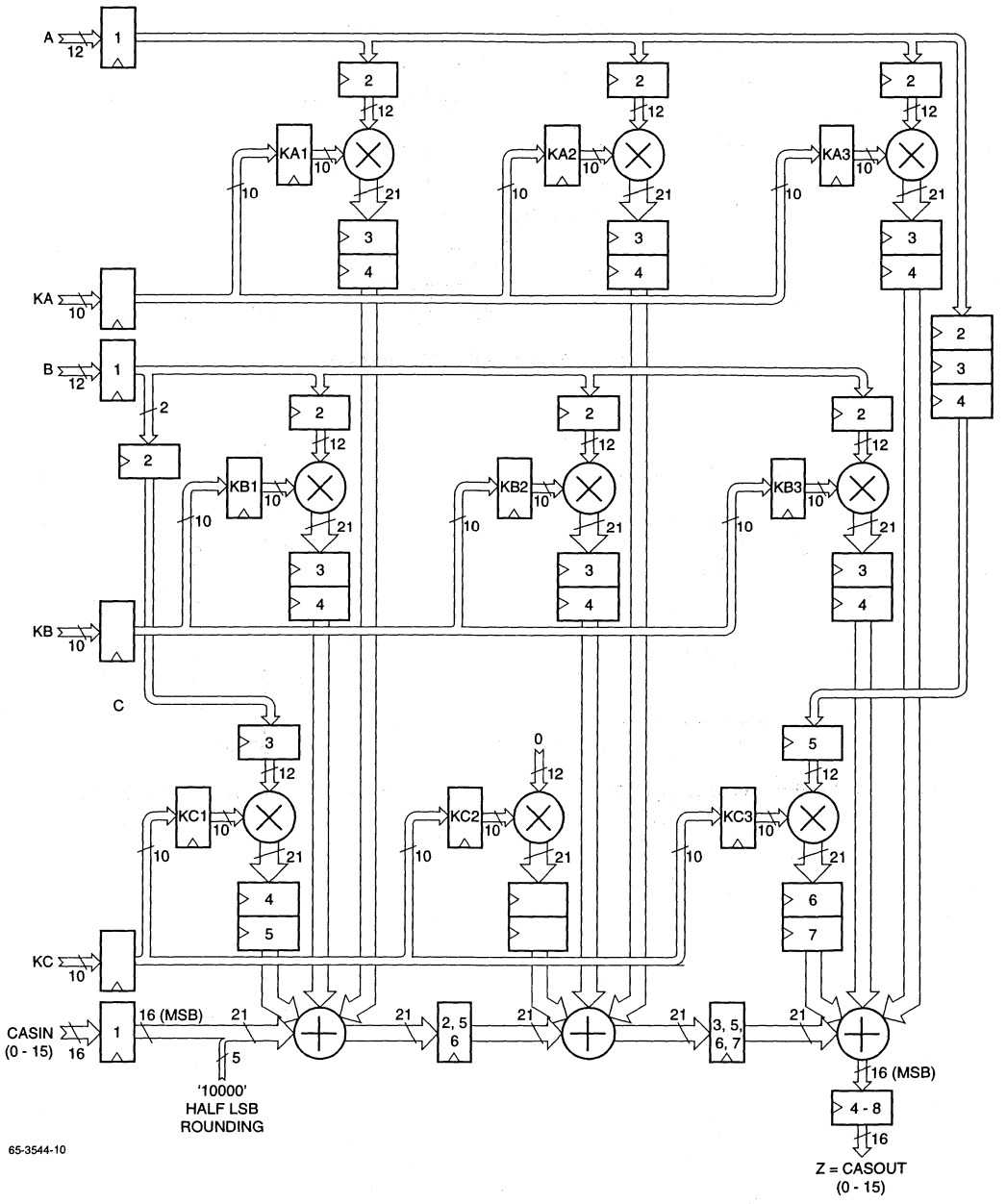


Figure 8. 4 x 2-Pixel Convolver Configuration (Mode 11)

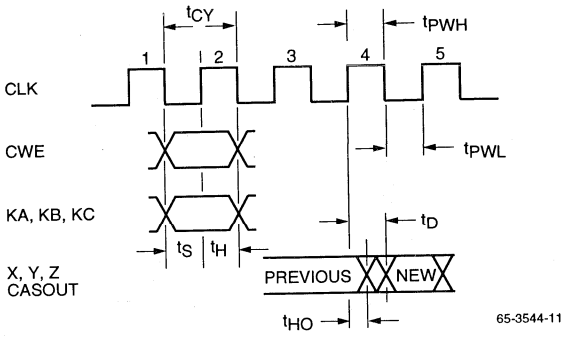


Figure 9. Input/Output Timing Diagram

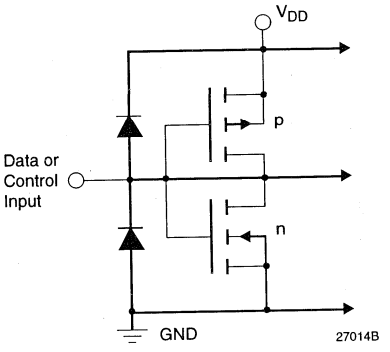


Figure 10. Equivalent Digital Input Circuit

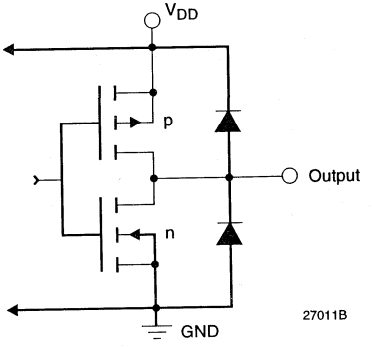


Figure 11. Equivalent Digital Output Circuit

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage	-0.5		7.0	V
Input Voltage	-0.5		V_{DD} + 0.5	V
Applied Voltage[2]	-0.5		V_{DD} + 0.5	V
Externally Forced Current[3,4]	-3.0		6.0	mA
Short Circuit Duration (single output in HIGH state to ground)			1	sec
Operating, Ambient Temperature	-20		110	°C
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering Temperature (10 seconds)			300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock Frequency	TMC2250A			30	MHz
		TMC2250A-2			40	MHz
		TMC2250A-3			50	MHz
t_{PWH}	CLK pulse width, HIGH		6			ns
t_{PWL}	CLK pulse width, LOW		8			ns
t_S	Input Data Setup Time		6			ns
t_H	Input Data Hold Time		2			ns
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Total Power Supply Current	V_{DD} = Max, C_{LOAD} = 25pF, f_{CLK} = Max				
		TMC2250A			125	mA
		TMC2250A-2			140	mA
		TMC2250A-3			155	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = HIGH, f_{CLK}=Max				
		TMC2250A			120	mA
		TMC2250A-2			135	mA
		TMC2250A-3			150	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			12	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH[1]	V_{DD} = Max, V_{IN} = V_{DD}			±5	µA
I_{IL}	Input Current, LOW[1]	V_{DD} = Max, V_{IN} = 0 V			±5	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH[2]	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW[2]	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = Max, V_{DD} = Min	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max, V_{DD} = Min			0.4	V

Notes:

1. Except pins XC_{11-0}, YC_{11-8}.
2. Pins XC_{11-0}, YC_{11-8}.

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			15	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	3			ns

Application Notes

Performing Large-Kernel Pixel Interpolation

The Cascade Input and Output Ports of the TMC2250A allow the user to stack multiple devices to perform larger interpolation kernels with no decrease in pixel throughput. Figure 12 illustrates a basic application utilizing Mode 11 to realize a 4 x 4-pixel kernel, also called Cubic Convolution.

This example utilizes the TMC2011A Variable-Length Shift Register to compensate for the internal latency of each TMC2250A. Alternatively, some applications may utilize RAM, FIFO's, or other methods to store multiple-line pixel data. In these cases the user may compensate for latency by simply offsetting the access sequencing of the storage devices.

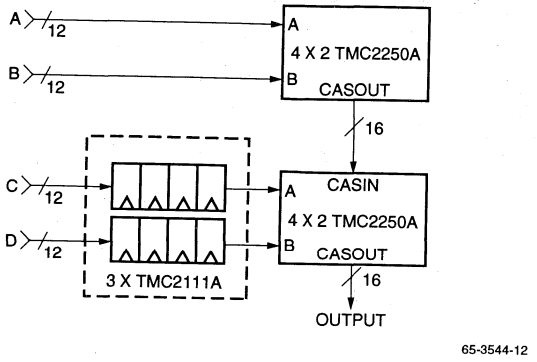


Figure 12. Performing Cubic Convolution with Two TMC2250A's

Related Products

- TMC2301 Image Resampling Sequencer
- TMC2302 Image Manipulation Sequencer
- TMC2249A Video Mixer
- TMC2242B Half-Band Filter

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2250AH5C	0°C to 70°C	30 MHz	Commercial	120 Pin Plastic Pin Grid Array	2250AH5C
TMC2250AH5C2	0°C to 70°C	40 MHz	Commercial	120 Pin Plastic Pin Grid Array	2250AH5C2
TMC2250AH5C3	0°C to 70°C	50 MHz	Commercial	120 Pin Plastic Pin Grid Array	2250AH5C3
TMC2250AKEC	0°C to 70°C	30 MHz	Commercial	120 Lead Plastic Quad Flatpack	2250AKEC
TMC2250AKEC2	0°C to 70°C	40 MHz	Commercial	120 Lead Plastic Quad Flatpack	2250AKEC2
TMC2250AKEC3	0°C to 70°C	50 MHz	Commercial	120 Lead Plastic Quad Flatpack	2250AKEC3

TMC2255

CMOS 3 x 3, 5 x 5 Image Convolver

8 x 8 Bits, 12 MHz Data Rate

Features

- 8-bit data and coefficient input precision
- Triple 3x1 matrix-vector multiplication mode
- 3x3 and 5x5 two-dimensional convolution modes
- TTL-compatible I/O with three-state output bus
- Offered in 68-contact plastic chip carrier (PLCC)
- Built-in 8-, 9-, and 12-bit arithmetic limiter
- Two's complement, unsigned, or mixed data formats

Applications

- RGB to/from YUV/YIQ color space conversion
- 3x3 or 5x5 two-dimensional FIR filtering
- Edge enhancement and general image processing
- Robotics and image recognition
- Electronic darkroom
- Desktop publishing

Description

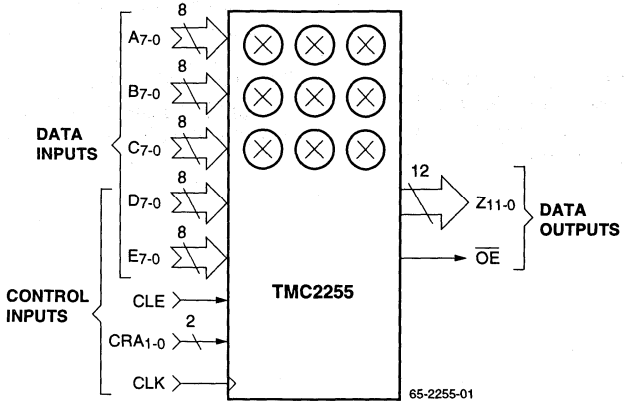
Like the faster TMC2250, the low-cost TMC2255 can perform a triple 3x1 matrix-vector multiplication or a 3x3 convolution. It can also perform a 5x5 convolution with bidimensionally symmetrical coefficients. The on-chip coefficient memory stores four sets of nine 8-bit two's complement coefficients. The device accepts unsigned and/or two's complement data at 1/3 of the applied clock rate.

The 3 (3x1) matrix multiply mode supports various 3-space numerical operations, such as video standards conversion (e.g. YIQ to RGB) or three-dimensional perspective transformation. Three input ports accept the 8-bit two's complement and/or unsigned magnitude data. The two remaining input ports can be loaded with coefficients and/or device control parameters "on-the-fly." In this mode, an output is generated on every clock cycle.

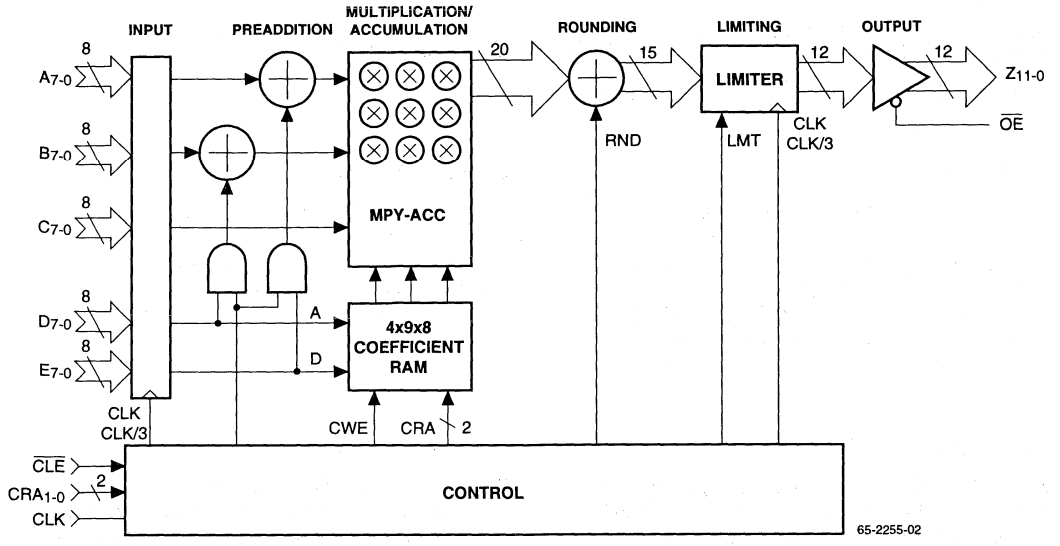
The 3x3 and 5x5 pixel image convolver modes support numerous functions, including static filtering and edge detection. On every third clock cycle, the TMC2255 accepts three (3x3 mode) or five (5x5 mode) data inputs. In the 5x5 mode, the coefficient kernel must be symmetric both horizontally and vertically. Outputs from the device are generated on every third clock cycle, matching the input pixel data rate, and can be limited ("clipped") to 8, 9, or 12 bits.

The TMC2255 will operate at clock rates of 0 to 36 MHz over the full commercial temperature (0°C to 70°C) and supply voltage ranges.

Logic Symbol



Structural Block Diagram



Functional Description

The TMC2255 contains an array of multipliers and adders, four 9x8-bit coefficient "pages" and a global control block, all of which can be initialized or reconfigured through ports D and E when $\overline{CLE}$ is LOW. Device parameters include matrix coefficient, internal device configuration (mode), rounding precision, and input/output data formats (two's complement, unsigned, or mixed). After the control parameters have been loaded, device operation commences with the next clock rising edge on which $\overline{CLE}$ returns HIGH. Depending on the mode selected, three or five data are input in parallel and proceed through a sequence of operations: Input, Preaddition, Multiply-Accumulation, Rounding, Limiting, and Output. See Figures 1–3 and the Structural Block Diagram.

Input Stage

Inputs are supplied to ports A through C in all operating modes on every third clock cycle, beginning with the clock rising edge that contains the most recent $\overline{CLE}$ LOW-to-HIGH transition. Control and/or coefficient parameters can be input through ports D and E during any of the three master clock cycles that make up each data cycle. In the 5x5 convolution mode, data enter the device through ports A–E. Control and/or coefficients may be updated through ports D and E on the remaining two cycles of each clock triplet.

Input data formats may be unsigned and/or two's complement, as identified in the mode select field of port E.

Preaddition

In and only in 5x5 convolution, the horizontal and vertical symmetry of the coefficient permits nine multipliers to do the work of 25. To facilitate this, the data input into ports A and E are pre-added before multiplication, as are the B and D inputs. See Figure 3, the 5x5 Block Diagram.

Coefficient Memory

The TMC2255 contains enough memory to store four "pages" of nine 8-bit two's complement coefficients each.

When $\overline{CLE}$ is LOW, a new coefficient is written through port E to the page and location address identified on port D. On every third clock cycle, the coefficient page to be read and used in the immediate 3-cycle computation set is selected by CRA_0 and CRA_1. Of the nine coefficients per page, K1,i (i = 1 to 3) process the port A (and E) data; K2,i, the port B and (D) data; and K3,i, the port C data.

Multiplication and Accumulation

The device computes nine products during every three clock cycles, accumulating them internally to full precision.

Rounding

Accumulated sums of products are rounded before the last 5 or 6 bits are truncated. Rounding is performed by adding "010000" or "100000" to the emerging data stream, according to the desired precision of the output results. When $\overline{CLE}$ = 0 and D = 0XXX1111, pin E_6 sets the chip's rounding position, viz: E_6 = 0: add .010000 and use Z_0 as least significant bit; E_6 = 1: add .100000 and use Z_1 as least significant bit, ignoring Z_0.

Output Limiting

The device provides programmable output limiting in unsigned (UN) and/or two's complement (TC) format and for 8, 9, or 12 bits of output precision (including Z_0). In 3 (3x1) mode, for an RGB-to-YIQ transformation, the device can limit Z_1 (Y) to 9 bits unsigned while limiting Z_3 (I) and Z_3 (Q) to 9 bits two's complement.

Outputs

Output is through the 12-bit Z port, which provides 1/2 or 1 LSB precision, relative to the input format. In the 3 (3x1) mode, three outputs will appear consecutively at the Z port during each triple clock cycle; for data input on clock rising edge 0, these results will emerge t_{DO} after clock rising edges 7, 8, and 9. In both convolution modes the results are output at 1/3 the device master clock rate, with the first point of the impulse response emerging after clock rising edge 9. To facilitate connection to a bus, the output buffers are enabled and disabled (placed in high-impedance state) by asynchronous control $\overline{OE}$.

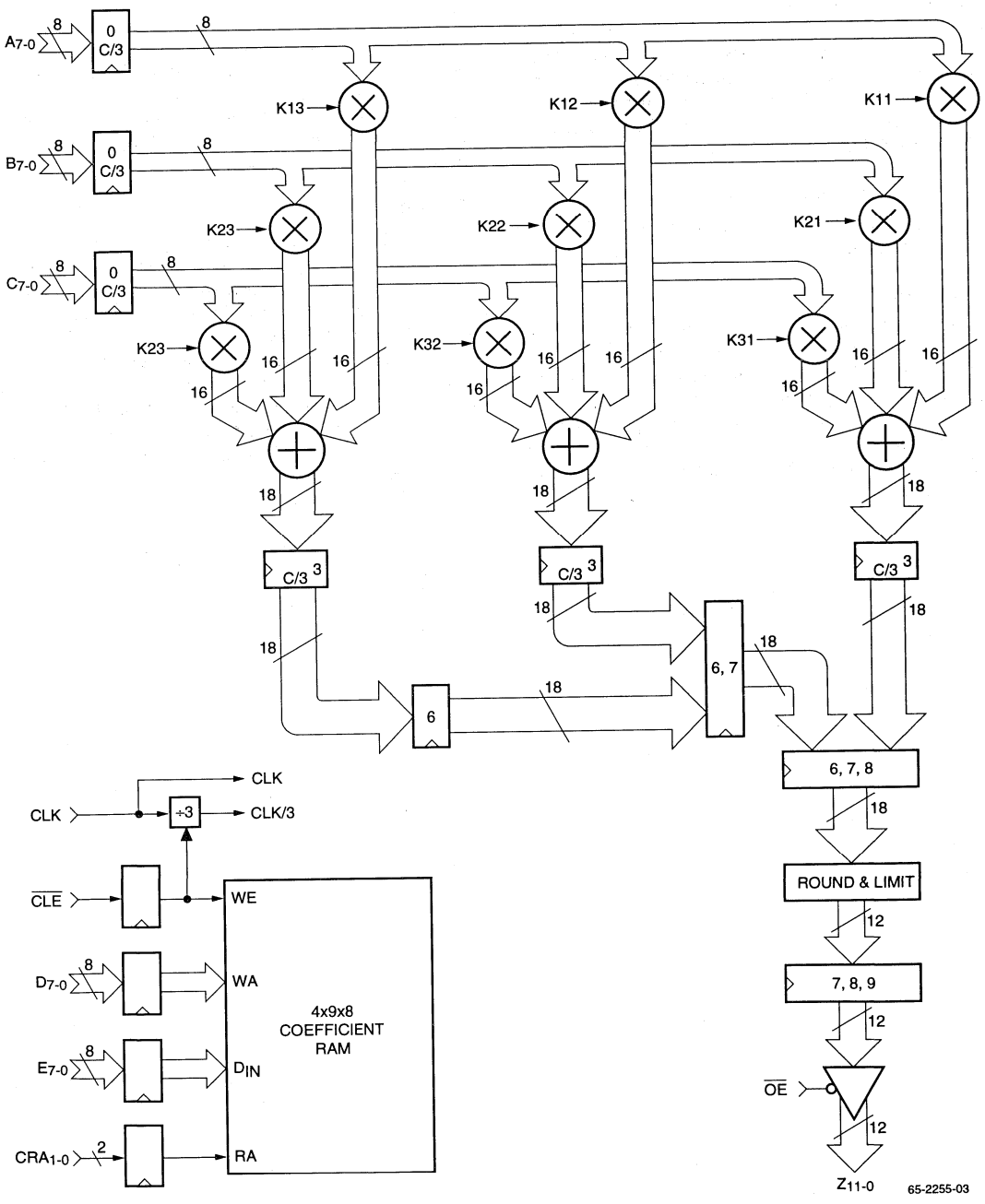


Figure 1. Functional Block Diagram, 3 (3x1) Mode

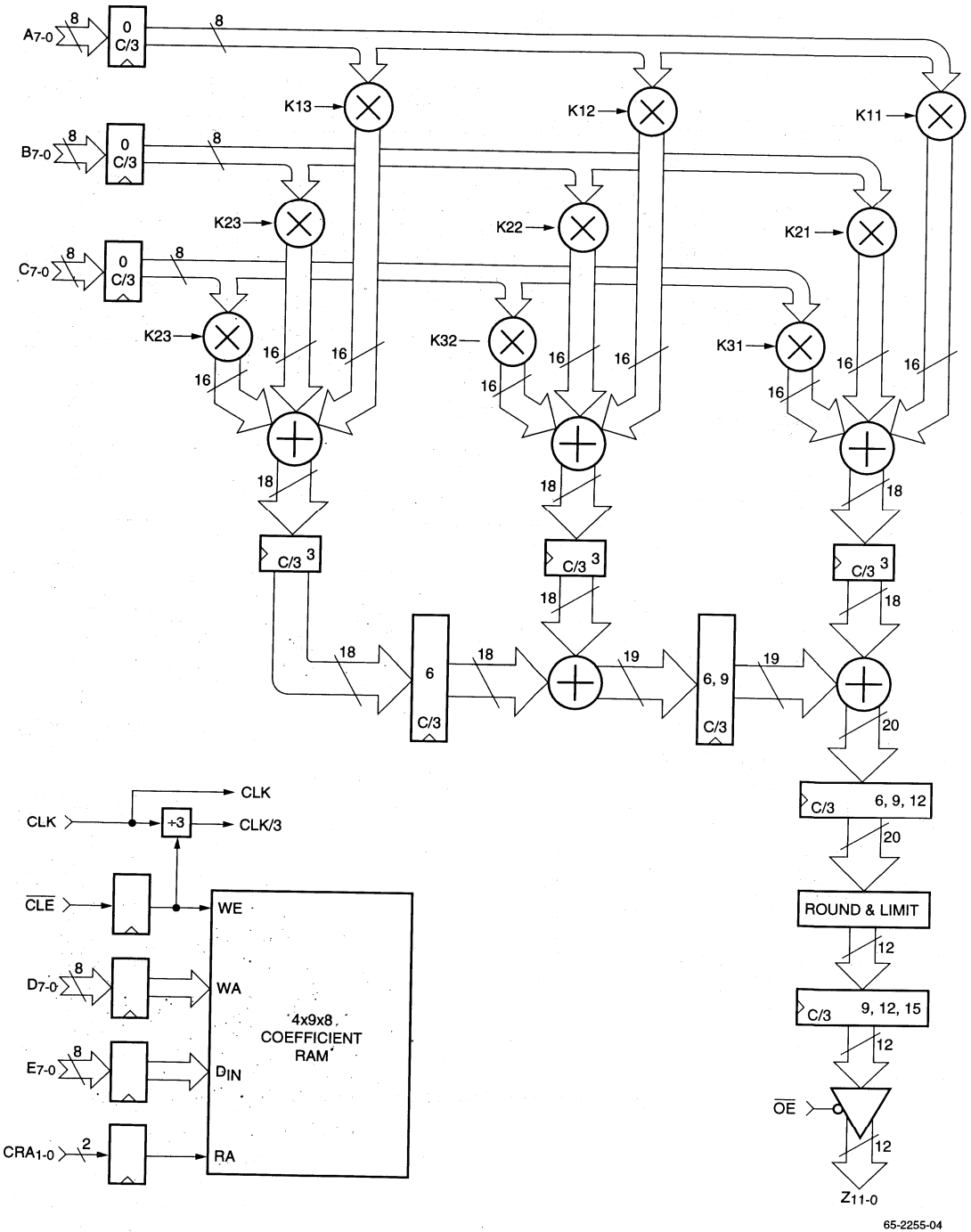


Figure 2. Functional Block Diagram, 3x3 Mode

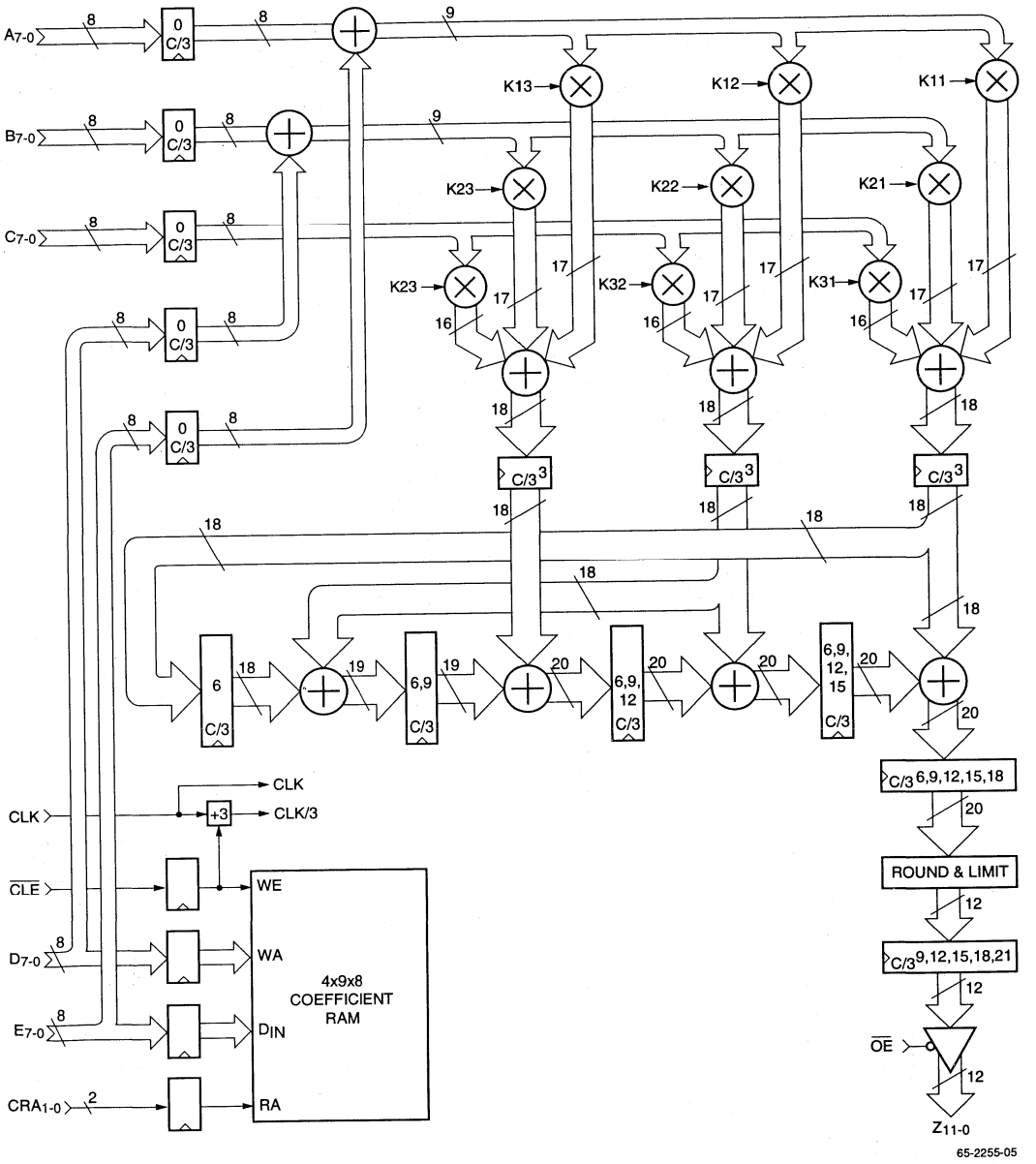
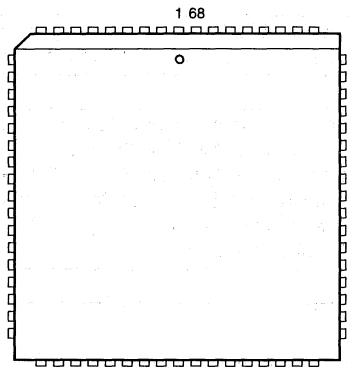


Figure 3. Functional Block Diagram, 5x5 Mode

Pin Assignments



65-2255-06

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	18	GND	35	GND	52	GND
2	V_{DD}	19	Z_6	36	D_7	53	V_{DD}
3	A_2	20	Z_5	37	D_6	54	B_7
4	A_1	21	Z_4	38	D_5	55	B_6
5	A_0	22	Z_3	39	D_4	56	B_5
6	$\overline{CLE}$	23	Z_2	40	D_3	57	B_4
7	$\overline{OE}$	24	Z_1	41	D_2	58	B_3
8	CLK	25	Z_0	42	D_1	59	B_2
9	GND	26	GND	43	D_0	60	B_1
10	V_{DD}	27	E_7	44	C_7	61	B_0
11	Z_{11}	28	E_6	45	C_6	62	CRA_1
12	Z_{10}	29	E_5	46	C_5	63	CRA_0
13	GND	30	E_4	47	C_4	64	A_7
14	Z_9	31	E_3	48	C_3	65	A_6
15	Z_8	32	E_2	49	C_2	66	A_5
16	Z_7	33	E_1	50	C_1	67	A_4
17	V_{DD}	34	E_0	51	C_0	68	A_3

Pin Descriptions

Pin Name	Pin Number	Pin Function Description
Inputs		
CLK	8	**Master chip clock, 0 to 30MHz.** All operations are referenced to the rising edges of CLK.
A_{0-7}, B_{0-7}, C_{0-7}, D_{0-7}, E_{0-7}	5-3, 68-64; 61-54; 51-44; 43-36; 34-27	**Data inputs.** Of the device's five 8-bit data input ports, A, B, and C are used exclusively as data inputs, whereas D and E are also used to program the device (see description of $\overline{CLE}$ pin). For 5x5 convolution, all five ports accept incoming data. In the other modes, only ports A-C accept incoming data, leaving D and E dedicated to control and coefficient values, which may be updated at any time. In all modes, data are loaded on every third rising edge for which $\overline{CLE}$ makes a 0-to-1 transition. Bits A_7, B_7,... are the two's complement sign bits or most significant unsigned bitsl bits A_0, B_0,... are the least significant bits (LSBs).
$\overline{CLE}$	6	**Active-LOW coefficient and control load enable.** When $\overline{CLE}$ is LOW, E becomes the input port for the coefficients, and D becomes the coefficient write address and control port. When $\overline{CLE}$ is HIGH, all coefficients are held unchanged. A LOW-to-HIGH transition at $\overline{CLE}$ also synchronizes the TMC2255, ushering in a new data input.
CRA_{1-0}	62-63	**Coefficient read address.** The chip can hold four "pages" of nine coefficients each. These two pins determine which of the four coefficient sets is to be used with the data entering during that cycle. The timing of coefficient selection by CRA is mode dependent. In the 3 (3x1) mode, CRA influences all coefficients simultaneously. In the 3x3 and 5x5 convolution modes, however, CRA selects the coefficients for each multiplier column individually, i.e. three per clock cycle from left to right (see Figure 3). CRA should be changed only on "data input" clock cycles to avoid corrupting 3x3 or 3 (3x1) work in progress. CRA should not be updated during a 5x5 operation whose result is needed. When updating coefficients on-the-fly, the user should not set CRA_{1-0} and D_{5-4} to the same page, but should read from one page while writing to another.

Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
$\overline{OE}$	7	**Asynchronous, active-LOW output enable.** When $\overline{OE}$ is LOW, the output drivers are enabled. When $\overline{OE}$ is HIGH, they are disabled (high-impedance).
Outputs		
Z_{11-0}	25-19, 16-14, 12-11	**Data outputs.** Outputs available on the Z port are enabled by $\overline{OE}$. Z_{11} is the unsigned MSB or two's complement MSB/sign bit; Z_1 is the integer LSB ("ones' digit"). Z_0 is the 1/2 fractional digit. In the 3 (3x1) mode (E = XXXXX0XX), a new valid result will emerge t_{DO} after every rising edge of CLK. In the other modes (E = XXXXX1XX), a result emerges after every third rising edge of CLK. Then 9-bit limiting is used, bits Z_{11} through Z_8 will be identical.
Power		
GND	1, 9, 13, 26, 35, 52	Ground.
VDD	2, 10, 17, 53	Supply Voltage (+5).

Operation and Timing

Before operation, the TMC2255 must be initalized, i.e. loaded with coefficients and set to the desired operating mode, data format, and rounding precision. The chip is programmed via ports D and E, which double as data input ports in 5x5 mode.

Initialization

Chip Select

This control is accessed through bit 7 of port D. When $\overline{CLE}$ is LOW, D_7 must be LOW to allow the coefficient/control information to be updated. If D_7 is HIGH when $\overline{CLE}$ is force LOW, the device will not allow the coefficient or control information to be updated, and device execution will begin or continue as commanded on the previous LOW-to-HIGH transition of $\overline{CLE}$. Holding D_7 HIGH (at least when $\overline{CLE}$ is LOW) permits the system to resynchronize the chip without changing any coefficients or configuration parameters.

Coefficient Loading

When $\overline{CLE}$ and D_7 are LOW, the coefficient values presented to port 6 are loaded into the coefficient position and page registers selected by port D, as shown in Table 1.

Each of the four "pages" YY comprises a full set of nine coefficients (one per filter tap).

Table 1. Coefficient Loading

When D_{7-0} =	Update from E_{7-0}: Coef	Page
0XYY0000	1,1	YY
0XYY0001	1,2	YY
0XYY0010	1,3	YY
0XYY0100	2,1	YY
0XYY0101	2,2	YY
0XYY0110	2,3	YY
0XYY1000	3,1	YY
0XYY1001	3,2	YY
0XYY1010	3,3	YY
0XXX0X11	Hold all coefficients	
0XXXX011	Hold all coefficients	
0XXX110X	Hold all coefficients	
0XXX11X0	Hold all coefficients	
0XXX1111	Control information	
1XXXXXXX	Hold all coefficients	

X = Don't Care

Mode Selection

When $\overline{CLE}$ = 0 and D = 0XXX1111, pins E_{2-0} select the chip's operating MODE and input data formats, as shown in Table 2.

Table 2. Mode Selection

When E_{7-0} =	Mode =	Data Formats		
		A	B	C
0XXXX000	3 (3x1) mat mpy	TC	TC	TC
0XXXX001	3 (3x1) mat mpy	UN	TC	TC
0XXXX010	RESERVED—Do not use			
0XXXX011	3 (3x1) mat mpy	UN	UN	UN
Z1 = A*K1,1 + B*K2,1 + C*K3,1		First of 3 results		
Z2 = A*K1,2 + B*K2,2 + C*K3,2				
Z3 = A*K1,3 + B*K2,3 + C*K3,3		Last of 3 results		
0XXXX100	3x3 convolution	TC	TC	TC
0XXXX101	3x3 convolution	UN	UN	UN
Z = A1*K1,1 + B1*K2,1 + C1*K3,1 + A2*K1,2 + B2*K2,2 + C2*K3,2 + A3*K1,3 + B3*K2,3 + C3*K3,3				
0XXXX110	5x5 convolution	TC	TC	TC
0XXXX111	5x5 convolution	UN	UN	UN
Z = A1*K1,3 + B1*K2,3 + C1*K3,3 + D1*K2,3 + E1*K1,3 + A2*K1,2 + B2*K2,2 + C2*K3,2 + D2*K2,2 + E2*K1,2 + A3*K1,1 + B3*K2,1 + C3*K3,1 + D3*K2,1 + E3*K1,1 + A4*K1,2 + B4*K2,2 + C4*K3,2 + D4*K2,2 + E4*K1,2 + A5*K1,3 + B5*K2,3 + C5*K3,3 + D5*K2,3 + E5*K1,3				
1XXXXXXX	Unchanged from previous setting			

Coefficients are always 8-bit two's complement.

Rounding

All computations are rounded internally following the final accumulation of products. Rounding position depends on the output format. If the user desires outputs with 1/2 LSB precision (relative to the inputs) then rounding is performed into Z_{-1}, just to the right of the LSB of the output port, Z_0. For 1 LSB precision, rounding is into Z_0, and the output is on pins Z_{11-1} only.

Table 3. Rounding

When E_{7-0} =	Outputs are	Rounded at
00XXXXXX	Z_{11}–Z_0 (12 bits)	Z_{-1}
01XXXXXX	Z_{11}–Z_1 (11 bits)	Z_{-0}
1XXXXXXX	Unchanged from previous setting	

Output Limiting

When $\overline{CLE}$ = 0 and D = 0XXX1111, pins E_{5-3} tell the chip to which numerical format(s) to limit the emerging results. Unsigned (UN), two's complement (TC), and mixed data formats of 8, 9, or 12 bits (including Z_0) are supported, as shown in Table 4. Limit "Z" applies to 3x3 and 5x5 convolutional modes; limits Z1, Z2, Z3 apply to 3(3x1) mode.

Prior to output, the limiter (if enabled) tests the leading bits of the emerging result. In the unsigned limit modes, if the MSB = 1, denoting a negative value, the output is forced to 0; if the MSB = 0 but any other bit above the 8, 9, or 12 bit output field = 1, the output is forced to 11111111111.1. In the TC9 limit mode, values above 127.5 (00001111111.1) are forced to 00001111111.1 and values below -128 become 11110000000.0. In the TC12 limit mode, values above 1023.5 (01111111111.1) are forced to 01111111111.1, and values below -1024 become 10000000000.0. If full LSB rounding (E_6 = 1) is used, output bit Z_0 is ignored, each data format is correspondingly 1 bit narrower than shown in Table 4, and the .5 fractions disappear from the range limits.

Table 4. Output Limiting

E_{7-0} =	Limit Z1 or Z	Limit Z2	Limit Z3	Range (RND = 0)
0X000XXX	Limiter disabled			
0X001XXX	UN9	UN9	UN9	0, 255.5
0X010XXX	TC12	TC12	TC12	-1024, 1023.5
0X011XXX	UN12	UN12	UN12	0, 2047.5
0X100XXX	TC9	TC9	TC9	-128, 127.5
0X101XXX	UN9	TC9	TC9	(Mixed)
0X110XXX	Reserved—Do not use			
0X111XXX	UN8	UN8	UN8	0, 127.5
1XXXXXXX	Unchanged from previous setting			

Timing

Result Latency

Device operating mode affects when valid results are available at the output port Z_{11-0}. The three results of a 3x1 triple dot product whose inputs enter on clock rising edge 0 will be available t_{DO} after clock rising edges 7, 8, and 9. In a 3x3 and 5x5 convolution, the first three impulse response points will emerge after clock rising edges 9, 12, and 15. The last two points of a 5-point response (5x5 mode) will follow after rising edges 18 and 21.

Instructions, Inputs, and Synchronization

Each rising edge of CLK which bears a $\overline{CLE}$ LOW-to-HIGH transition resynchronizes the device. If $\overline{CLE}$ goes from LOW to HIGH on clock rising edge N, then the chip will resynchronize, starting a new 3-cycle sequence on that edge. It will look for incoming data at clock rising edges N+3i, where i = 1, 2, ... (see Figures 4 through 10). If $\overline{CLE}$ is brought LOW while an operation is already in progress (e.g., to update coefficients), it should be brought HIGH only on a regular data input clock cycle (N+3i), to avoid corrupting pending results.

IF $\overline{CLE}$ is LOW, control and/or coefficient information enetering on a rising edge of CLK will affect all subsequent data inputs until the control parameters are again updated. Internal pipelining of the controls ensures that "in progress" operations on data previously input into the device will continue unaffected, as long as $\overline{CLE}$ is brought HIGH only on data input clock edges.

System Timing

Because the TMC2255's data throughput rate is 1/3 of its incoming clock rate, the user must synchronize the data inputs with the chip's control inputs and internal operation. Figures 4 through 7 illustrate four ways to use rising edges of $\overline{CLE}$ to align data inputs in the 3 (3x1) and 3x3 modes, whereas Figures 8 through 10 show how to use $\overline{CLE}$ in the 5x5 mode.

In Figure 4, the $\overline{CLE}$ 0-to-1 transition on CLK rising edge 3 (t = 3) initialized the chip. The final configuration and coefficient values are loaded through ports D and E at t = 2 and the first incoming data enter ports A, B, and C on rising edge 6. In 3 (3x1) mode, the three results from the t = 6 input data emerge after t = 13, 14, and 15. In 3x3 mode, the first result from the edge 6 input data appears after edge 15 and remains until t = 18, when the second result using t = 6 inputs (which is the first result using t = 9 inputs) emerges. After t = 18, the convolution of the t = 6, t = 9, and t = 12 inputs, the last output involving the t = 6 input, appears. The part operates continuously, with inputs read on every third rising clock edge and a new output available t_{DO} after each rising clock edge (3 (3x1) mode) or every third rising edge (3x3 mode).

In Figure 5, CLK rising edges at t = 3, 6, 9, ... resynchronize the chip, with configuration or coefficient updates at t = 2, 5, 8, ... Data input/output timing is unchanged from Figure 3.

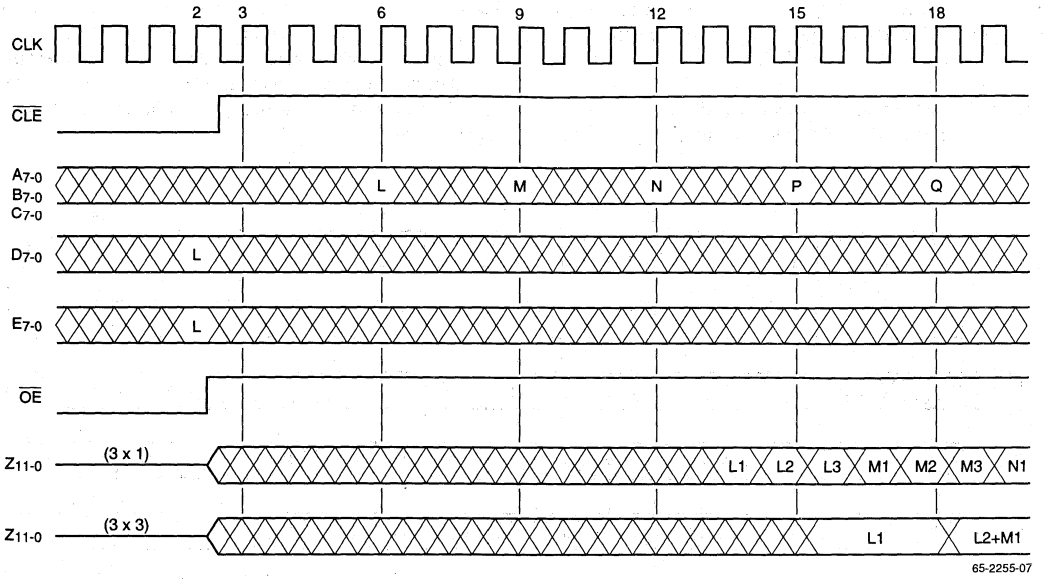


Figure 4. 3 (3x1), 3x3 Timing Diagram, Single $\overline{CLE}$ Rising Edge

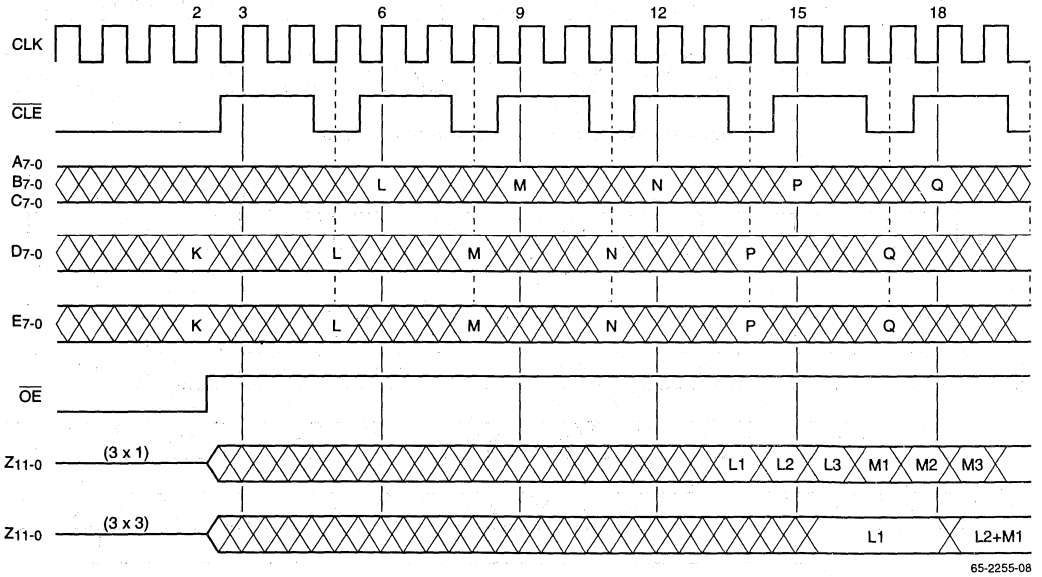


Figure 5. 3xX Modes, Periodic Long $\overline{CLE}$ Pulses

In Figure 6, CLK rising edges at t = 3, 6, 9, ... again resynchronize the chip, but configuration and coefficients my be changed twice as often, at t = 1, 2, 4, 5, 7, 8, ...

In Figure 7, data timing is the sames as that of Figure 4. However, since $\overline{CLE}$ is left LOW after the one-cycle initialization pulse, instructions and coefficients may be updates on every clock cycle, or three times per data input. Instructions entering between data values, e.g. at t = 4 or t = 5, affect the next data value (i.e., that entering at t = 6). Instructions entering with a given data value (e.g., t = 6) affect the next data input (i.e., at t = 9).

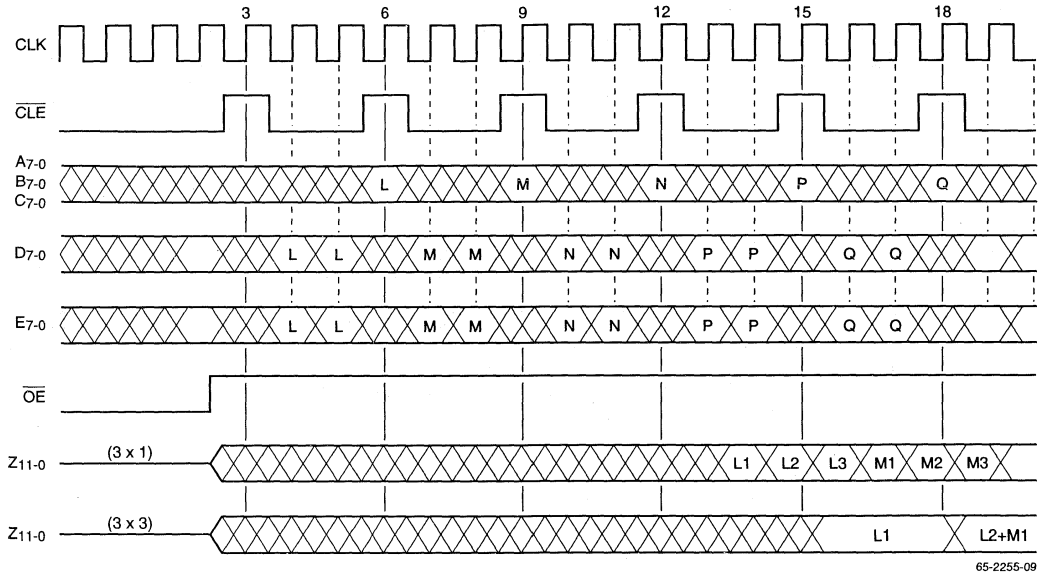


Figure 6. 3xX Modes, Periodic Short $\overline{CLE}$ Pulses

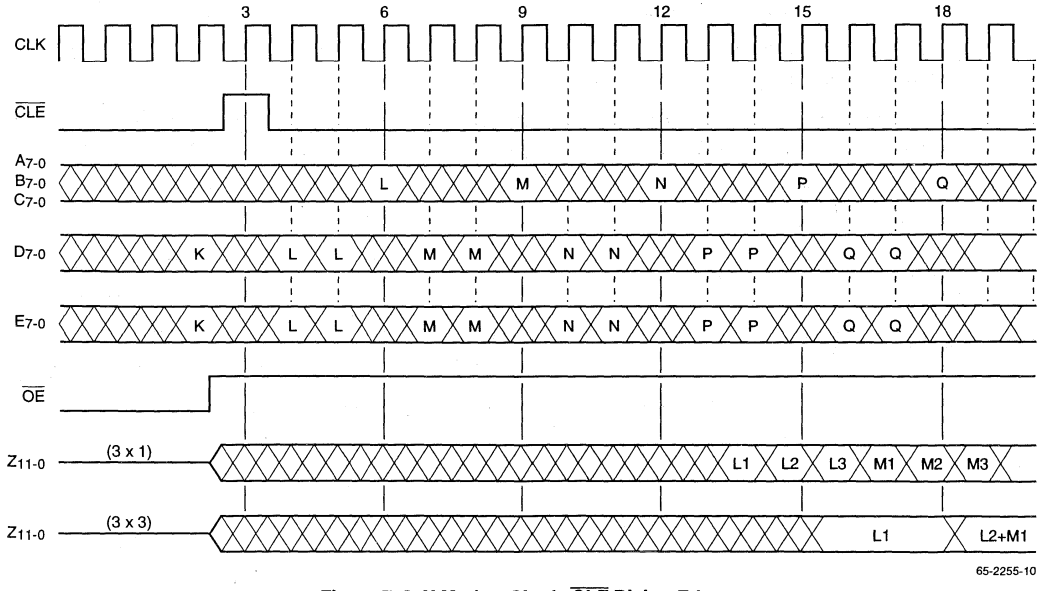


Figure 7. 3xX Modes, Single $\overline{CLE}$ Rising Edge

In Figure 8, the CLK rising edge at t = 3 synchronizes the operation. The final configuration and coefficient values are loaded through ports D and E at t = 2, and the first incoming data enter ports A through E at t = 6. The first results using the t = 6 input appears after t = 15 and remains until t = 18. The last result using the t = 6 input emerge after t = 27 and remains until t = 30. The part operates continuously, with data inputs read on every third rising edge of CLK and a new output available t_{DO} after every third rising edge of CLK.

In Figure 9, one new coefficient or configuration value can be input for every data input, at t = 5, 8, 11, … .

In Figure 10, two new coefficients or configuration values can be loaded for every incoming data point, at t = 4, 5, 7, 8, 10, 11, … .

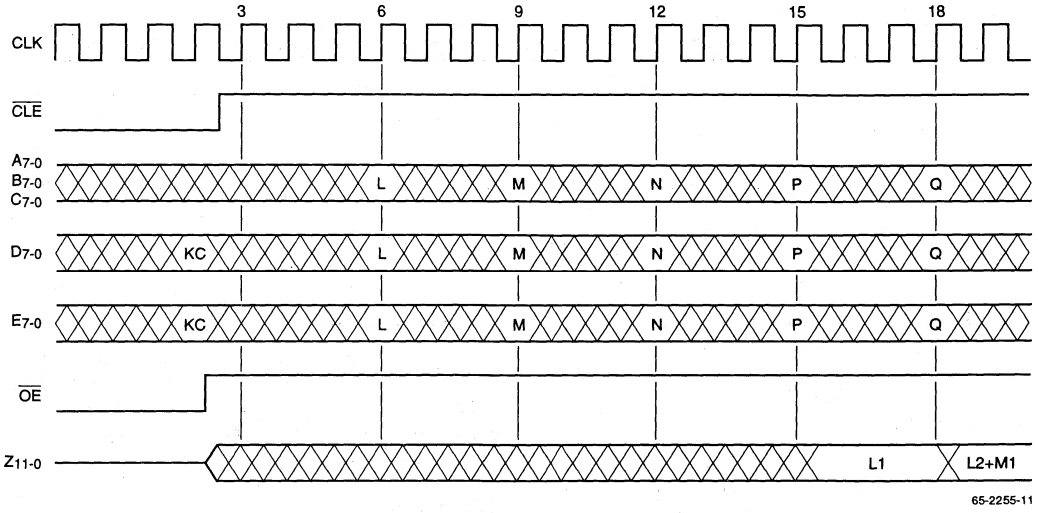


Figure 8. 5x5 Convolution, Single $\overline{CLE}$ Rising Edge

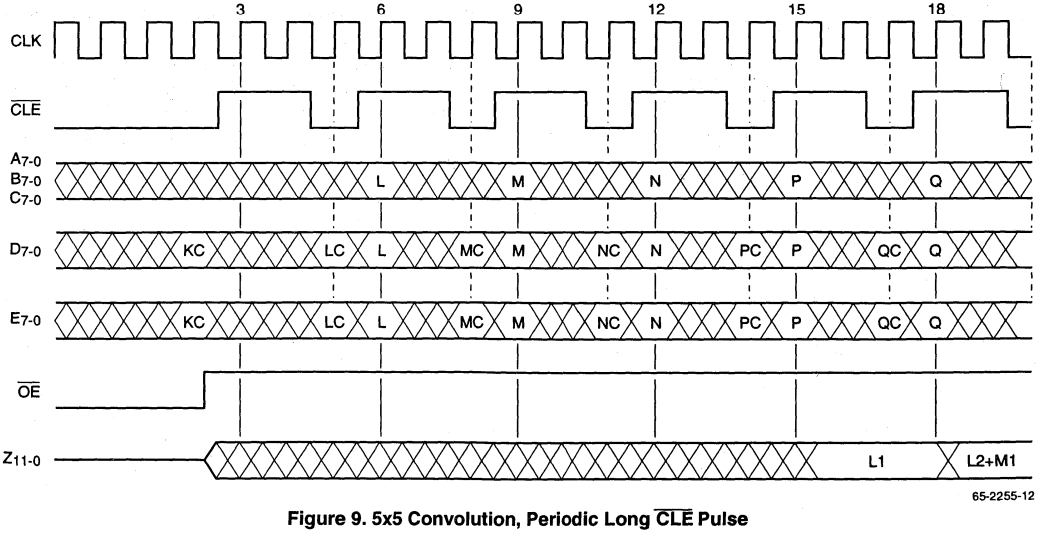


Figure 9. 5x5 Convolution, Periodic Long $\overline{CLE}$ Pulse

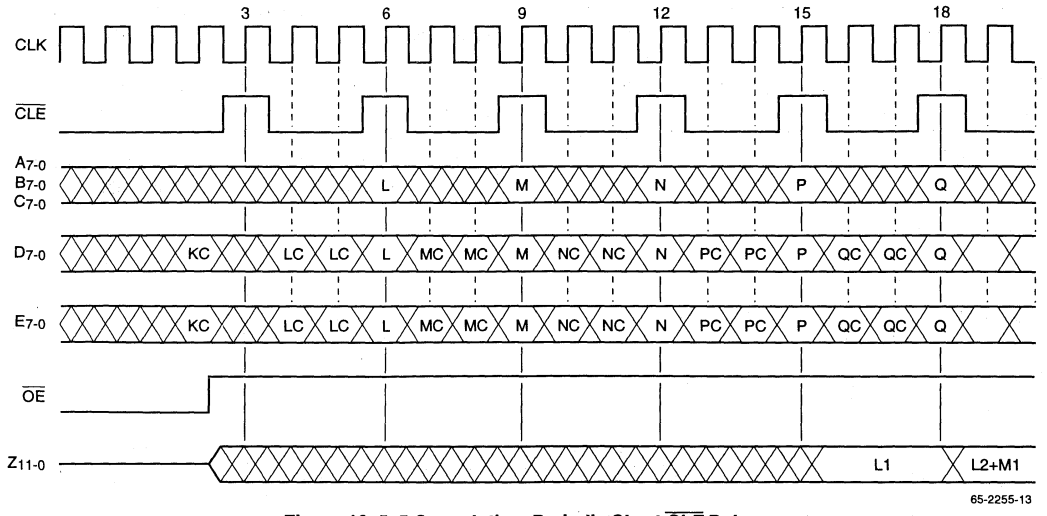


Figure 10. 5x5 Convolution, Periodic Short $\overline{CLE}$ Pulse

In 5x5 mode, $\overline{CLE}$ should not be left LOW continuously, since ports D and E must serve as data inputs on every third clock cycle. If $\overline{CLE}$ is LOW on a data input cycle, the chip will interpret the current D and E inputs as both data and instructions/coefficients.

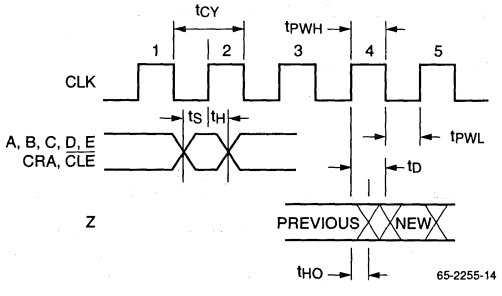


Figure 11. I/O Timing Diagram

Power-Up Sequence

To ensure proper operation, the TMC2255 should receive at least two clock rising edges soon after power-up, with $\overline{CLE}$ making a 0-to-1 transition on edge 4, 5, or 6. Otherwise, some of the internal multiplexers will power up in disallowed states and draw excessive power.

Data Formats

Figure 12 summarizes the TMC2255's data and coefficient formats for all operating modes. Although integer weighting of input data is shown, the binary point may be moved anywhere to the left, as long as the binary point of the output is moved the same distance. Likewise, the coefficient binary point can be moved, as long as the output binary point is moved equally or the data input binary point is moved in the opposite direction. In all coefficients and in all two's complement data, the most significant bit carries a negative weighting.

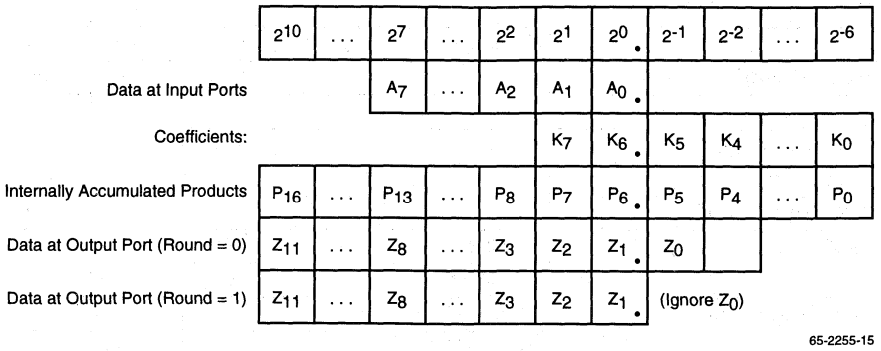


Figure 12. Data Formats and Bit Alignment

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage	-0.5		7.0	V
Input Voltage	-0.5		V_{DD} + 0.5	V
Output Applied Voltage[2]	-0.5		V_{DD} + 0.5	V
Output Forced Current[3,4]	-6.0		6.0	mA
Short Circuit Duration (single output in HIGH state to ground)			1	sec
Operating Case Temperature	-60		130	°C
Junction Temperature			175	°C
Storage Temperature	-65		150	°C
Lead Soldering Temperature (10 seconds)			300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Package	Min	Nom	Max	Unit
V_{DD}	Supply Voltage		4.75	5.0	5.25	V
V_{IL}	Input Voltage LOW				0.8	V
V_{IH}	Input Voltage HIGH		2.0			V
I_{OL}	Output Current LOW				4.0	mA
I_{OH}	Output Current HIGH				-2.0	mA
t_{CY}	Cycle Time	TMC2255	33			ns
		TMC2255-1	27			
t_{PWL}	Clock Pulse Width LOW	TMC2255	16			ns
		TMC2255-1	14			
t_{PWH}	Clock Pulse Width HIGH	TMC2255	13			ns
		TMC2255-1	10			
t_S	Input Setup Time	TMC2255	8			ns
		TMC2255-1	6			
t_H	Input Hold Time		0			ns
t_A	Ambient Temperature		0	25	70	°C

Electrical Characteristics

Parameter		Test Conditions	Min	Max	Unit
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max., V_{IN} = 0		15	mA
I_{DDU}	Supply Current, No Load	V_{DD} = Max., t_{CY} = 50ns		100	mA
I_{IL}	Input Current LOW			-10	µA
I_{IH}	Input Current, HIGH			10	µA
V_{OL}	Output Voltage, LOW			0.4	V
V_{OH}	Output Voltage, HIGH		2.0		V
I_{OS}	Short-Circuit Output Current			-100	µA
C_I	Input Capacitance			10	pF
C_O	Output Capacitance			10	pF

Note: Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching Characteristics

Parameter		Test Conditions	Package	Min	Max	Unit
t_D	Output Delay	V_{DD} = Min., C_L = 25pF	TMC2255		22	ns
			TMC2255-1		19	
t_{HO}	Output Hold	V_{DD} = Max., C_L = 25pF			6	ns
t_{ENA}	Output Enable	V_{DD} = Min., C_L = 25pF	TMC2255		18	ns
			TMC2255-1		15	
t_{DIS}	Output Disable	V_{DD} = Min., C_L = 25pF	TMC2255		21	ns
			TMC2255-1		20	

Equivalent Circuits and Transition Levels

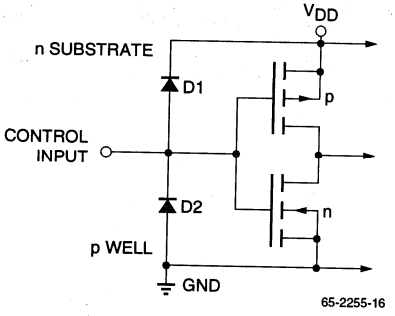


Figure 13. Equivalent Input Circuit

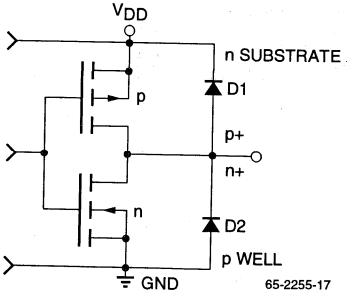


Figure 14. Equivalent Output Circuit

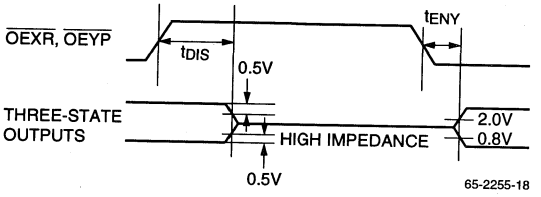


Figure 15. Transition Levels for Three-State Measurements

Related Products

- TMC2011 Variable Length Shift Resistor
- TMC2302 Image Manipulation Sequencer

BROADCAST VIDEO

Ordering Information

Product Number	Data Rate (MHz)	Temperature Range	Screening	Package	Package Marking
TMC2255R1C	10	0°C to 70°C	Commercial	68 Pin PLCC	2255R1C
TMC2255R1C1	12.5	0°C to 70°C	Commercial	68 Pin PLCC	2255R1C1

TMC2272A

Digital Colorspace Converter

36 Bit Color, 50 MHz

Features

- 50 MHz (20ns) pipelined throughput
- 3 Simultaneous 12-bit input and output channels (64 Giga $\{2^{36}\}$ colors)
- Two's complement inputs and outputs
- Overflow headroom available in lower resolution
- 10-bit user-defined coefficients
- TTL compatible input and output signals
- Full precision internal calculation
- Output rounding
- On-board coefficient memory
- Submicron CMOS process

Applications

- Translation between component color standards (RGB, YIQ, YUV, etc.)
- Broadcast composite color encoding and decoding (all standards)
- Broadcast composite color standards conversion and transcoding
- Camera tube and monitor phosphor colorimetry correction
- White balancing and color-temperature conversion
- Image capture, processing and storage
- Color matching between systems, cameras and monitors
- Three-dimensional perspective translation

Description

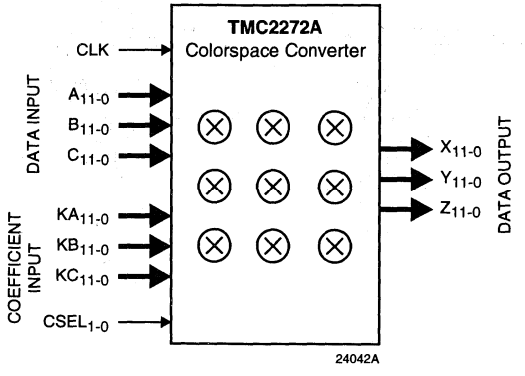
A 50-MHz, three-channel, 36 bit (three 12-bit components) colorspace converter and color corrector, the TMC2272A uses 9 parallel multipliers to process high-resolution imagery in real time.

The TMC2272A also operates at any slower clock rate and with any smaller data path width, allowing it to handle all broadcast and consumer camera, frame-grabber, encoder/decoder, recorder and monitor applications as well as most electronic imaging applications.

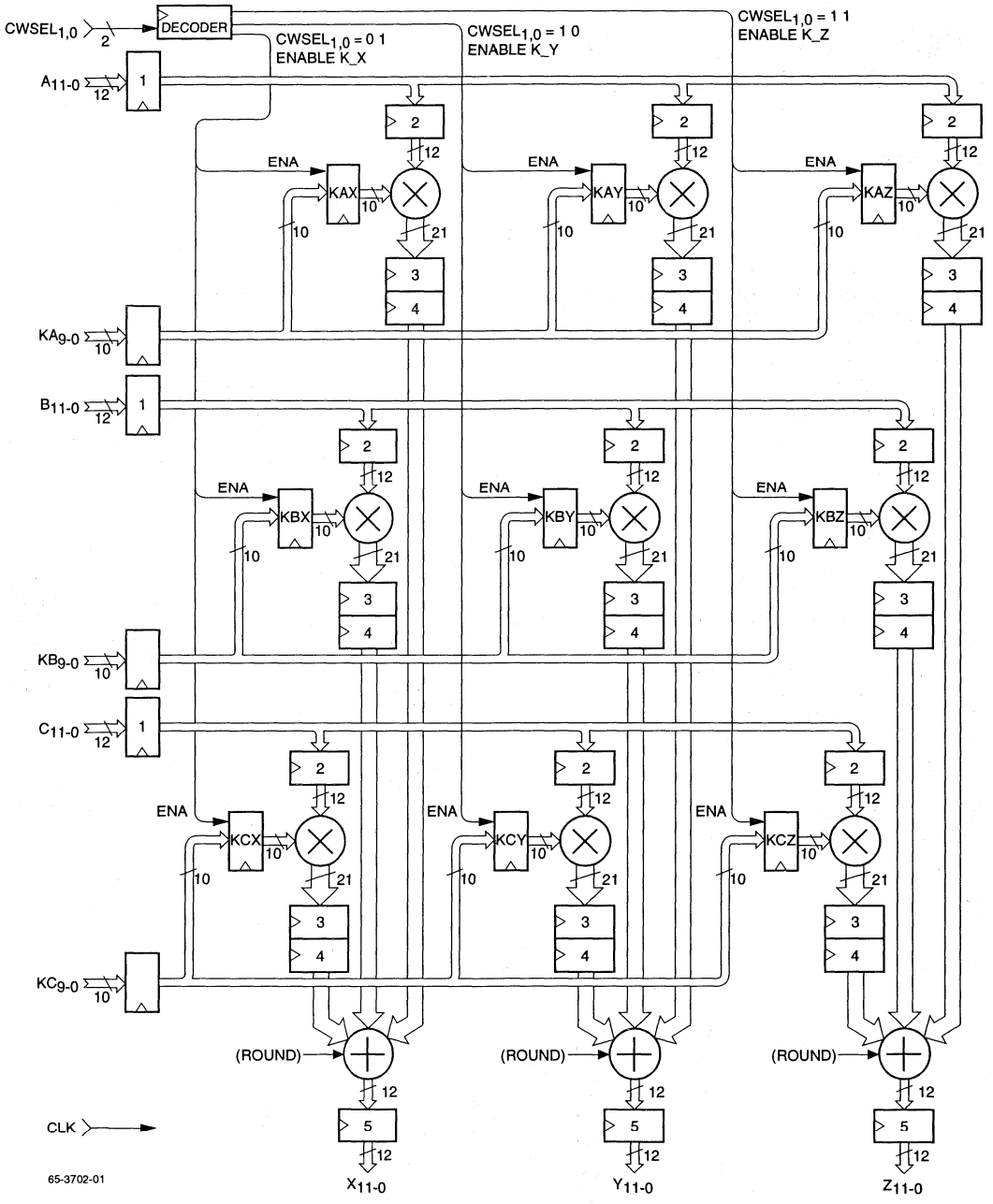
A complete set of three 12-bit samples is processed on every clock cycle, with a five-cycle pipeline latency. Full 23-bit (for each of three components) internal precision is provided with 10-bit user-defined coefficients. The coefficients may be varied dynamically, with three new coefficients loaded every clock cycle. (The full set of nine can be replaced in three clock cycles.) Rounding to 12 bits per component is performed only at the final output. This allows full accuracy with correct rounding and overflow headroom for applications that require less than 12 bits per component.

The TMC2272A is fabricated in a submicron CMOS process and performance is guaranteed over the full operating temperature range. It is available in a 120-pin Plastic Pin-Grid Array (PPGA) package and 120-pin Plastic Quad FlatPack (PQFP) in three speed grades.

Logic Symbol



Block Diagram



Functional Description

The TMC2272A is a nine–multiplier array with the internal bus structure and summing adders needed to implement a 3 x 3 matrix multiplier (triple dot product). With a 50MHz guaranteed maximum clock rate, this device offers video and imaging system designers a single–chip solution to numerous common image and signal–processing problems.

The three data input ports ($A_{11\text{-}0}$, $B_{11\text{-}0}$, $C_{11\text{-}0}$) accept 12-bit two's complement integer data, which is also the format for the output ports ($X_{11\text{-}0}$, $Y_{11\text{-}0}$, $Z_{11\text{-}0}$). Other format and path width options are discussed in the numeric format and overflow section. The coefficient input ports (KA, KB, KC) are always 10-bit two's complement fractional. Table 2 details the bit weighting.

Full precision is maintained throughout the TMC2272A. Each output is accurately rounded to 12 bits from the 23 bits entering the final adder.

Signal Definitions

A(n), B(n), C(n)

Indicates the data word presented to that input port during the specified clock rising edge (n). Applies to input ports $A_{11\text{-}0}$, $B_{11\text{-}0}$, and $C_{11\text{-}0}$.

KAX(n) thru KCZ(n)

Indicates coefficient value stored in the specified one of the nine onboard coefficient registers KAX through KCZ, input during or before the specified clock rising edge (n).

X(n), Y(n), Z(n)

Indicates data available at that output port t_{DO} after the specified clock rising edge (n). Applies to output ports $X_{11\text{-}0}$, $Y_{11\text{-}0}$, and $Z_{11\text{-}0}$.

The TMC2272A utilizes six input and output ports to realize a "triple dot product", in which each output is the sum of all three input words, multiplied by the appropriate stored coefficients. The three corresponding sums of products are available at the outputs five clock cycles after the input data are latched, and three new data words rounded to 12-bits are then available every clock cycle. See the Applications Discussion regarding encoded video standard conversion matrices.

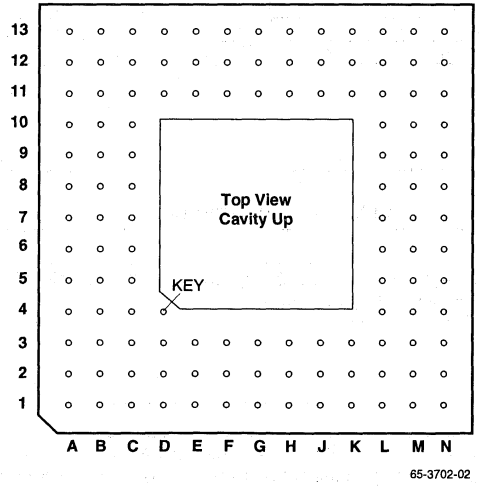
$$X(5)=A(1)KAX(1)+B(1)KBX(1)+C(1)KCX(1)$$

$$Y(5)=A(1)KAY(1)+B(1)KBY(1)+C(1)KCY(1)$$

$$Z(5)=A(1)KAZ(1)+B(1)KBZ(1)+C(1)KCZ(1)$$

Pin Assignments

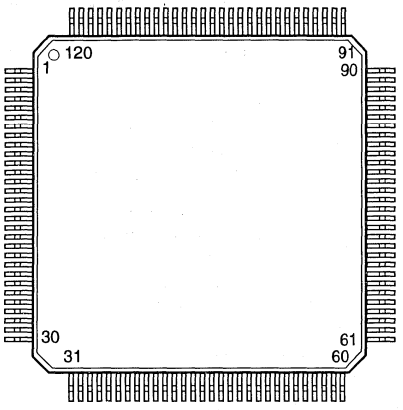
120 Pin Plastic Grid Array, H5 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	X_7	C5	GND	G11	A_3	L10	KB_8
A2	X_9	C6	C_{10}	G12	A_2	L11	KA_1
A3	X_{10}	C7	GND	G13	A_4	L12	KA_5
A4	GND	C8	V_{DD}	H1	Y_4	L13	KA_6
A5	C_{11}	C9	C_0	H2	Y_0	M1	Z_2
A6	C_8	C10	B_8	H3	V_{DD}	M2	Z_7
A7	C_7	C11	B_5	H11	GND	M3	Z_9
A8	C_5	C12	B_3	H12	A_0	M4	Z_{11}
A9	C_3	C13	B_1	H13	A_1	M5	KC_2
A10	C_1	D1	Y_{11}	J1	Y_1	M6	KC_4
A11	B_{10}	D2	X_0	J2	Y_2	M7	KC_6
A12	B_7	D3	X_3	J3	GND	M8	KC_9
A13	B_4	D11	CLK	J11	KA_8	M9	KB_2
B1	X_4	D12	B_0	J12	$CWSEL_1$	M10	KB_5
B2	X_5	D13	A_{10}	J13	$CWSEL_0$	M11	KB_9
B3	X_8	E1	Y_9	K1	Y_3	M12	KA_2
B4	X_{11}	E2	Y_{10}	K2	Z_0	M13	KA_3
B5	GND	E3	GND	K3	Z_3	N1	Z_5
B6	C_9	E11	A_{11}	K11	KA_4	N2	Z_8
B7	C_6	E12	A_9	K12	KA_7	N3	Z_{10}
B8	C_4	E13	A_8	K13	KA_9	N4	KC_1
B9	C_2	F1	Y_7	L1	Z_1	N5	KC_3
B10	B_{11}	F2	Y_8	L2	Z_4	N6	KC_5
B11	B_9	F3	V_{DD}	L3	Z_6	N7	KC_7
B12	B_6	F11	A_7	L4	GND	N8	KC_8
B13	B_2	F12	A_6	L5	KC_0	N9	KB_1
C1	X_1	F13	A_5	L6	GND	N10	KB_3
C2	X_2	G1	Y_5	L7	V_{DD}	N11	KB_6
C3	X_6	G2	Y_6	L8	KB_0	N12	KB_7
C4	V_{DD}	G3	GND	L9	KB_4	N13	KA_0

Pin Assignments (continued)

120 Pin Metric Quad Flat Pack (MQFP), KE Package



65-3702-03

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	X_6	31	Z_6	61	KA_1	91	B_5
2	X_5	32	Z_7	62	KA_2	92	B_6
3	X_4	33	Z_8	63	KA_3	93	B_7
4	X_3	34	GND	64	KA_4	94	B_8
5	X_2	35	Z_9	65	KA_5	95	B_9
6	X_1	36	Z_{10}	66	KA_6	96	B_{10}
7	X_0	37	Z_{11}	67	KA_7	97	B_{11}
8	GND	38	KC_0	68	KA_8	98	C_0
9	Y_{11}	39	KC_1	69	KA_9	99	C_1
10	Y_{10}	40	KC_2	70	$CWSEL_1$	100	C_2
11	Y_9	41	KC_3	71	$CWSEL_0$	101	C_3
12	V_{DD}	42	GND	72	GND	102	V_{DD}
13	Y_8	43	KC_4	73	A_0	103	C_4
14	Y_7	44	KC_5	74	A_1	104	C_5
15	Y_6	45	KC_6	75	A_2	105	C_6
16	GND	46	V_{DD}	76	A_3	106	GND
17	Y_5	47	KC_7	77	A_4	107	C_7
18	Y_4	48	KC_8	78	A_5	108	C_8
19	Y_0	49	KC_9	79	A_6	109	C_9
20	V_{DD}	50	KB_0	80	A_7	110	C_{10}
21	Y_1	51	KB_1	81	A_8	111	C_{11}
22	Y_2	52	KB_2	82	A_9	112	GND
23	Y_3	53	KB_3	83	A_{10}	113	GND
24	GND	54	KB_4	84	A_{11}	114	GND
25	Z_0	55	KB_5	85	B_0	115	X_{11}
26	Z_1	56	KB_6	86	B_1	116	X_{10}
27	Z_2	57	KB_7	87	B_2	117	X_9
28	Z_3	58	KB_8	88	CLK	118	V_{DD}
29	Z_4	59	KB_9	89	B_3	119	X_8
30	Z_5	60	KA_0	90	B_4	120	X_7

Pin Descriptions

Pin Name	H5 Pin Number	KE Pin Number	Pin Function Description
Power			
V_{DD}	F3, H3, L7, C8, C4	12, 20, 46, 102, 118	**Supply Voltage.** The TMC2272A operates from a single +5V supply. All pins must be connected.
GND	E3, G3, J3, L4, L6, H11, C7, C5, A4, B5	8, 16, 24, 34, 42, 72, 106, 112, 113, 114	**Ground**
Clock			
CLK	D11	88	**System Clock.** The TMC2272A operates from a single system clock input. All timing specifications are referenced to the rising edge of clock.
Controls			
$CWSEL_{1,0}$	J12, J13	70, 71	**Coefficient Write Select.** This input selects which three of the 9 coefficient registers, if any, will be updated on the next clock cycle from the KA_{9-0}, KB_{9-0}, AND KC_{9-0} inputs. See Table 4 and the Functional Block Diagram.

Pin Descriptions (continued)

Pin Name	H5 Pin Number	KE Pin Number	Pin Function Description
Inputs			
A_{11-0}	E11, D13, E12, E13, F11, F12, F13, G13, G11, G12, H13, H12	84, 83, 82, 81, 80, 79, 78, 77, 76, 75, 74, 73	**Data Input A.** This is one of three 12-bit wide data input ports.
B_{11-0}	B10, A11, B11, C10, A12, B12, C11, A13, C12, B13, C13, D12	97, 96, 95, 94, 93, 92, 91, 90, 89, 87, 86, 85	**Data Input B.** This is one of three 12-bit wide data input ports.
C_{11-0}	A5, C6, B6, A6, A7, B7, A8, B8, A9, B9, A10, C9	111, 110, 109, 108, 107, 105, 104, 103, 101, 100, 99, 98	**Data Input C.** This is one of three 12-bit wide data input ports.
KA_{9-0}	K13, J11, K12, L13, L12, K11, M13, M12, L11, N13	69, 68, 67, 66, 65, 64, 63, 62, 61, 60	**Coefficient Input KAX, KAY, or KAZ.** These are the 10-bit wide coefficient input ports. The value at each of these three inputs will update one coefficient register as selected by the coefficient write select ($CWSEL_{1-0}$) on the next clock. See Table 1 and the Functional Block Diagram.
KB_{9-0}	M11, L10, N12, N11, M10, L9, N10, M9, N9, L8	59, 58, 57, 56, 55, 54, 53, 52, 51, 50	**Coefficient Input KBX, KBY, OR KBZ.** These are the 10-bit wide coefficient input ports. The value at each of these three inputs will update one coefficient register as selected by the coefficient write select ($CWSEL_{1-0}$) on the next clock. See Table 1 and the Functional Block Diagram.
KC_{9-0}	M8, N8, N7, M7, N6, M6, N5, M5, N4, L5	49, 48, 47, 45, 44, 43, 41, 40, 39, 38	**Coefficient Input KCX, KCY, OR KCZ.** These are the 10-bit wide coefficient input ports. The value at each of these three inputs will update one coefficient register as selected by the coefficient write select ($CWSEL_{1-0}$) on the next clock. See Table 1 and the Functional Block Diagram.
Outputs			
X_{11-0}	B4, A3, A2, B3, A1, C3, B2, B1, D3, C2, C1, D2	115, 116, 117, 119, 120, 1, 2, 3, 4, 5, 6, 7	**Output X.** These are the data outputs. Data are available at the 12-bit registered Output Ports X,Y and Z t_{DO} after every clock rising edge.
Y_{11-0}	D1, E2, E1, F2, F1, G2, G1, H1, K1, J2, J1, H2	9, 10, 11, 13, 14, 15, 17, 18, 23, 22, 21, 19	**Output Y.** These are the data outputs. Data are available at the 12-bit registered Output Ports X,Y and Z t_{DO} after every clock rising edge.
Z_{11-0}	M4, N3, M3, N2, M2, L3, N1, L2, K3, M1, L1, K2	37, 36, 35, 33, 32, 31, 30, 29, 28, 27, 26, 25	**Output Z.** These are the data outputs. Data are available at the 12-bit registered Output Ports X,Y and Z t_{DO} after every clock rising edge.

Table 1. Coefficient Loading

		$CWSEL_{1,0}$			
		00	**01**	**10**	**11**
Input	KA_{9-0}	Hold All	Load KAX	Load KAY	Load KAZ
Input	KB_{9-0}	Hold All	Load KBX	Load KBY	Load KBZ
Input	KC_{9-0}	Hold All	Load KCX	Load KCY	Load KCZ

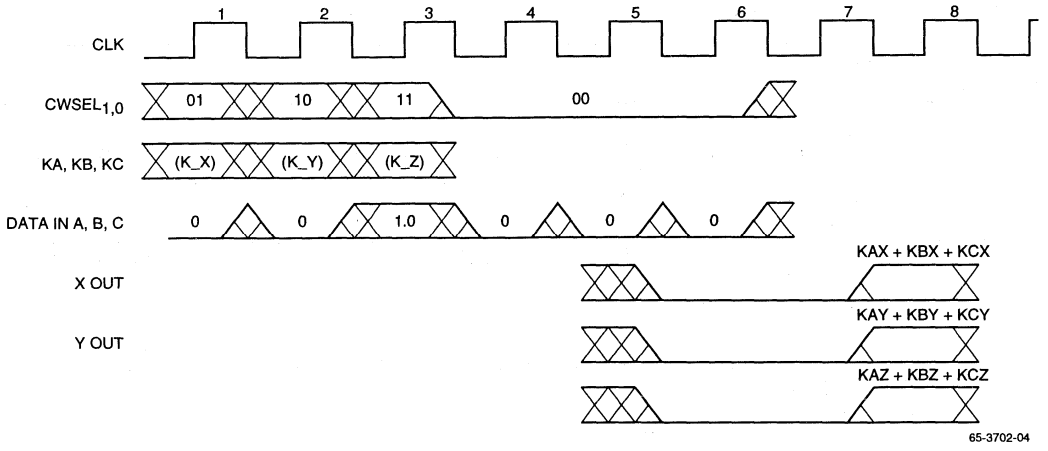


Figure 1. Impulse Response

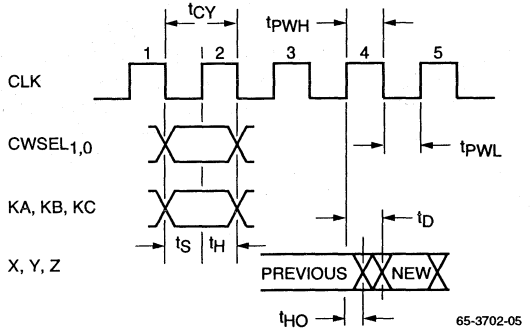


Figure 2. Input/Output Timing

Numeric Format and Overflow

Table 2 shows the binary weightings of the input and output ports of the TMC2272A. Although the internal sums of products could grow to 23 bits, the outputs X, Y, and Z are rounded to yield 12-bit integer words. Thus the output format is identical to the input data format. Bit weighting is easily adjusted by applying the same scaling correction factor to both input and output data words.

As shown in Table 2, the TMC2272A's matched input and output data formats accommodate 0dB (unity) gain. Therefore the user must be aware of input conditions that could lead to numeric overflow. Maximum input data and coefficient word sizes must be taken into account with the specific translation performed to ensure that no overflow occurs.

Use with Fewer than 12 Bits

The TMC2272A can be configured to provide several format and overflow options when used in systems with fewer than 12 bits of resolution. An 8-bit system will be used as an example, however these concepts apply to any other word width.

The most apparent mode of operation is to left justify the incoming data and to ground the unused input LSBs. Hoever, the outputs will still be rounded to the least significant bit of the TMC2272A, having little if any effect on the top 8 bits actually used. Because the TMC2272A carries out all calculations to full precision, the preferred mode of operation is to right jusitfy and sign extend the data as shown in Figure 3. Since all the LSBs are used, the desired output will be rounded correctly, and overflow will be accommodated by bits 7 through 10.

The TMC2272A may also be used in unsigned binary 8-bit systems as shown in Figure 4. Bits 11 through 8 will handle overflow.

In all applications, a digital zero (ground) should be connected to all unused inputs.

Table 2. Bit Weightings for Input and Output Data Words

Bit Weights	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	•	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}
Inputs																						
All Modes Data A, B, C	$-I_{11}$	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	•									
Coefficients KA, KB, KC												$-K_9$	•	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0
Internal Sum	$-X_{20}$	X_{19}	X_{18}	X_{17}	X_{16}	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	•	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
Outputs																						
X, Y, Z	$-O_{11}$	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	•									

A minus sign indicates a two's complement sign bit.

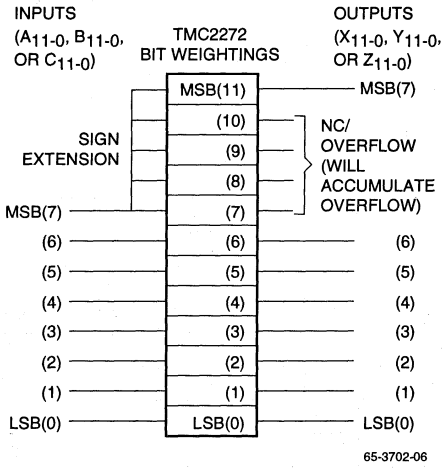


Figure 3. Two's Complelent 8-bit Application

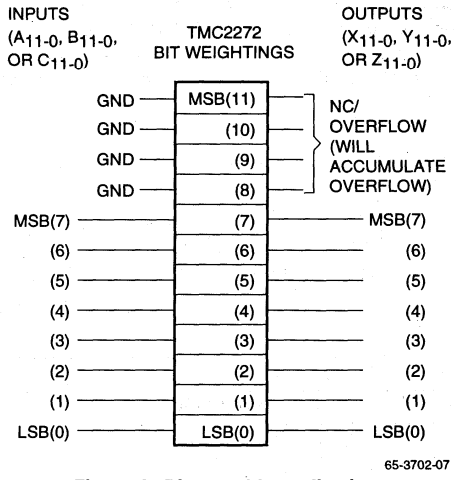


Figure 4. Binary 8-bit Application

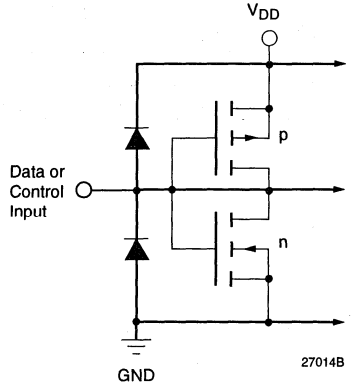


Figure 5. Equivalent Digital Input Circuit

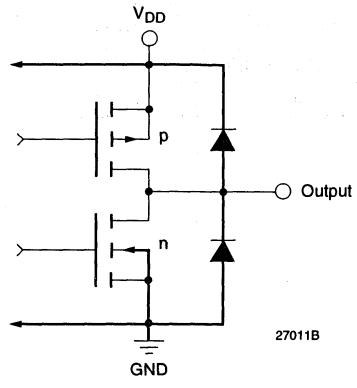


Figure 6. Equivalent Digital Output Circuit

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage	-0.5		7.0	V
Input Voltage	-0.5		V_{DD} + 0.5	V
Applied Voltage[2]	-0.5		V_{DD} + 0.5	V
Externally Forced Current[3,4]	-3.0		6.0	mA
Short Circuit Duration (single output in HIGH state to ground)			1	sec
Operating, Ambient Temperature	-20		110	°C
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering Temperature (10 seconds)			300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock Frequency	TMC2272A			30	MHz
		TMC2272A-2			40	MHz
		TMC2272A-3			50	MHz
t_{PWH}	CLK pulse width, HIGH		6			ns
t_{PWL}	CLK pulse width, LOW		8			ns
t_S	Input Data Setup Time		6			ns
t_H	Input Data Hold Time		2			ns
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Total Power Supply Current	V_{DD} = Max, C_{LOAD} = 25pF, f_{CLK} = Max				
		TMC2272A			125	mA
		TMC2272A-2			140	mA
		TMC2272A-3			155	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, f_{CLK}=Max				
		TMC2272A			120	mA
		TMC2272A-2			135	mA
		TMC2272A-3			150	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			12	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH[1]	V_{DD} = Max, V_{IN} = V_{DD}			±5	µA
I_{IL}	Input Current, LOW[1]	V_{DD} = Max, V_{IN} = 0 V			±5	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH[2]	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW[2]	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = Max, V_{DD} = Min	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max, V_{DD} = Min			0.4	V

Notes:

1. Except pins XC_{11-0}, YC_{11-8}.
2. Pins XC_{11-0}, YC_{11-8}.

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			15	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	3			ns

Applications Discussion

The TMC2272A can convert between any two three-coordinate colorspaces with the selection of the proper coefficients. Sets of coefficients for some popular colorspace conversions are presented below.

By concatenating coefficient matrices of single transformations, the user can program the TMC2272A to perform compound transforms efficiently. For example, given an RGB input, correction of the relative values of R and B, for color temperature, conversion to YIQ, modification of contrast by changing Y, and conversion back to RGB can be performed as quickly and easily as any simple transformation. To calculate the final set of coefficients from the coefficients of the individual transformations, the procedure in Figure 7 (concatenation) is used. If more than two matrices are to be combined, the result from the concatenation of the first two matrices is concatenated with the third. If more matrices must be incorporated in the final function, the last step is repeated.

$$\begin{vmatrix} A & B & C \\ D & E & F \\ G & H & I \end{vmatrix} \begin{vmatrix} J & K & L \\ M & N & O \\ P & Q & R \end{vmatrix} = \begin{vmatrix} AJ + BM + CP & AK + BN + CQ & AL + BO + CR \\ DJ + EM + FP & DK + EN + FQ & DL + EO + FR \\ GJ + HM + IP & GK + HN + IQ & GL + HO + IR \end{vmatrix}$$

65-3702-08

Figure 7. Concatenation

Converting from GBR to YC_BC_R

With the right coefficients, two external NOT gates, and an external 4-bit half-adder, the TMC2272A can convert video data from 8-bit full-scale (e.g. VGA) GBR components to 10-bit YC_BC_R components.

Table 2. 10-bit component formats and inclusive ranges.

Color Space Term		Range	Format
Y	Luminance	64-940	magnitude
Y'	Y - 64	0-876	magnitude
C_B	Color difference, Blue	64-960	magnitude
U'	C_B - 512	±448	2's comp
C_R	Color difference, Red	64-960	magnitude
V'	C_R - 512	±448	2's comp
GBR	Green, Blue, Red components	0-255	magnitude, 8-bits

The analog defining equations for 1 Volt luminance and ±0.5 Volt color difference components are:

$$Y = +0.5870\,(G) + 0.1140\,(B) + 0.2990\,(R)$$

$$B - Y = -0.3313\,(G) + 0.5000\,(B) - 0.1687\,(R)$$

$$R - Y = -0.4187\,(G) - 0.0813\,(B) + 0.5000\,(R)$$

To translate these equations into the digital domain, note that the ranges of R, G, and B are 0 to 255 instead of 0 to 1, the range of Y is 64 to 940 instead of 0 to 1, and the ranges of U and V are 64 to 960 instead of +/-0.5:

$$Y = (876/255)(0.587(G)+0.114(B)+0.299(R))+64$$
$$= 2.01652\,(G)+0.39162(B)+1.02715(R)+64$$

$$C_B = (896/255)(0.3313(G)+0.5(B)-0.1687(R))+512$$
$$= -1.16397(G)+1.75686(B)-0.59289(R)+512$$

$$C_R = (896/255)(-0.4187(G)-0.0813(B)+0.5(R))+512$$
$$= -1.47115(G)-0.28571(B)+1.75686(B))+512$$

Let Y'=Y-64, U'=C_B-512, and V'=C_R - 512. The TMC2272A will compute Y', U', and V'. Adding 64 (040_h) externally to Y' will then yield Y, whereas inverting the most significant bits of U' and V', U'9 and V'9, will yield C_B and C_R, respectively. Multiplying the equations immediately above by 128 and rounding each coefficient to the nearest integer yields the recommended set of coefficients for GBR to YUV conversion.

128 (Y')	=	258 (G)	+50 (B)	+131 (R)	dec.
		102	032	083	hex
128 (U')	=	-149 (G)	+225 (B)	-76 (R)	dec
		36B	0E1	3B4	hex
1281 (V')	=	-188 (G)	-37 (B)	+225 (R)	dec.
		344	3DB	0E1	hex

If the TMC2272A input data alignment for 8-bit GBR is:

0 0 G7 G6 G5 G4 G3 G2 G1 G0 0 0

0 0 B7 B6 B5 B4 B3 B2 B1 B0 0 0

0 0 R7 R6 R5 R4 R3 R2 R1 R0 0 0

then the output data alignment for 10-bit Y'U'V' is:

0 0 Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0

U9 U9 U9 U8 U7 U6 U5 U4 U3 U2 U1 U0

V9 V9 V9 V8 V7 V6 V5 V4 V3 V2 V1 V0

where the tripled U9 and V9 sign bits denote two's complement sign extensions. The factors of 4 in the input data format and 128 in the equations are absorbed by the internal 9-bit (factor of 512) right-shifting of the emerging results.

At the output of the TMC2272A, invert the most significant bits, U9 and V9, of the chrominance components, and add 1 at Y6 of the luminance to obtain the true CCIR Rec. 601 values.

Converting from GBR to 8-bit Full-Scale YUV

With the right coefficients and two external NOT gates, the TMC2272A can convert video data from 8-bit full-scale (e.g. VGA) GBR components to 8-bit full-scale YUV components.

Table 3. 8-bit component formats and inclusive ranges:

Color Space Term		Range	Format
Y	Luminance	0-255	magnitude
U	Color difference, Blue	128 to -127	2's comp
U'	U + 128	0-255	magnitude
V	Color difference, Red	128 to -127	2's comp
V'	V + 128	0-255	magnitude
G,B,R	Green, Blue, Red components	0-255	magnitude

As in the previous RGB to YC_BC_R case, begin with the defining equations, but without the range compensation factors of 255/876 and 255/896:

Y = 0.5870 (G) +0.1140 (B) +0.2990 (R)

U = -0.3313 (G) +0.5000 (B) -0.1687 (R)

V = -0.4187 (G) -0.0813 (B) +0.5000 (R)

The TMC2272A will compute Y, U, and V directly, whereas inverting the most significant bits of U and V, U7 and V7 will yield U' and V', respectively. Multiplying the equations immediately above by 512 and rounding each coefficient to the nearest integer yields the recommended set of coefficients for GBR to YUV conversion.

512 (Y) = 301 (G) + 58 (B) + 153 (R) dec.
12D 03A 099 hex

512 (U) = –170 (G) + 256 (B) – 86 (R) dec.
356 100 3AA hex

512 (V) = –214 (G) – 42 (B) + 256 (R) dec.
32A 3D6 100 hex

If the TMC2272A input data alignment for 8-bit GBR is:

0 0 0 0 G7 G6 G5 G4 G3 G2 G1 G0

0 0 0 0 B7 B6 B5 B4 B3 B2 B1 B0

0 0 0 0 R7 R6 R5 R4 R3 R2 R1 R0

then the output data alignment for 8-bit YUV is:

0 0 0 0 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0

U7 U7 U7 U7 U7 U6 U5 U4 U3 U2 U1 U0

V7 V7 V7 V7 V7 V6 V5 V4 V3 V2 V1 V0

where the quintupled U9 and V9 sign bits denote two's complement sign extensions. The factor of 512 in the equations above is absorbed by the internal 9-bit right shift of each emerging result.

At the output of the TMC2272A, invert the most significant bits, U7 and V7, of the chrominance components, to obtain the 8-bit offset format.

Converting From YC_BC_R to GBR

Following the notation employed earlier, the TMC2272A will be used to convert data in Y'U'V' format into GBR format.

Since Y' = 876, U' = V' = 0, and G = B = R = 255 for saturated white output, every Y' coefficient will be 225/876 = 0.29110. The full analog matrix for Y'U'V' to GBR conversion is:

G = 0.29110 (Y') – 0.09794 (U') – 0.20324 (V')

B = 0.29110 (Y') + 0.50431 (U')

R = 0.29110 (Y') + 0.39901 (V')

Since the largest element is just over 0.5 and the largest permissible coefficient is 511, multiply all elements of the matrix by 512 to obtain the values to load into the TMC2272A.

G = 149 (Y') – 50 (U') – 04 (V') dec.
095 3CE 398 hex

B = 149 (Y') + 258 (U') dec.
095 100 hex

R = 149 (Y') + 204 (V') dec.
095 0CC hex

Decrease the incoming luminance at the input to the TMC2272A by 64 by adding 1's at positions Y9, Y8, Y7, and Y6. Invert U9 and V9 and their sign extensions, to accommodate CCIR Rec. 601 data. Instead of reducing Y by 64, an alternate is to reduce each of the G, B, and R outputs by (255) (64 / 876) = 19.

For the Y'U'V' to RGB conversion, the TMC2272A input data alignment for 10-bit Y'U'V' is:

0 0 Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0

U9 U9 U9 U8 U7 U6 U5 U4 U3 U2 U1 U0

V9 V9 V9 V8 V7 V6 V5 V4 V3 V2 V1 V0

where the tripled U9 and V9 sign bits denote two's complement sign extensions. The TMC2272A output data alignment for 8-bit GBR is then:

0 0 0 0 G7 G6 G5 G4 G3 G2 G1 G0

0 0 0 0 B7 B6 B5 B4 B3 B2 B1 B0

0 0 0 0 R7 R6 R5 R4 R3 R2 R1 R0

Converting From 8-bit Full Scale YUV to GBR

Following the notation employed earlier, the TMC2272A will be used to convert data in 8-bit YUV format into 8-bit GBR format.

Since Y = 256, U = V = 0, and G = B = R = 255 for saturated white output, every Y coefficient will be 255 / 255=1.0. The full matrix for YUV to GBR conversion is:

G = 1.0 (Y) -0.3443 (U) -0.7142 (V)

B = 1.0 (Y) +1.7727 (U)

R = 1.0 (Y) +1.3965 (V)

Since the largest element is over 1.0 and the largest permissible coefficient is 511, multiply all elements of the matrix by 256 to obtain the values to load into the TMC2272A:

G = 256 (Y')	- 88 (U')	- 83 (V')	dec.
100	3A8	349	hex
B = 256 (Y')	+ 454 (U')		dec.
100	1C6		hex
R = 256 (Y')	+ 359 (V')		dec.
100	167		hex

For the YUV to RGB conversion, the TMC2272A input data alignment for 10-bit Y'U'V' is:

0 Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 0

U9 U9 U8 U7 U6 U4 U4 U3 U2 U1 U0 0

V9 V9 V8 V7 V6 V5 V4 V3 V2 V1 V0 0

where the doubled U9 and V9 sign bits denote two's complement sign extensions. The TMC2272A output data alignment for 8-bit GBR is then:

0 0 0 0 G7 G6 G5 G4 G3 G2 G1 G0

0 0 0 0 B7 B6 B5 B4 B3 B2 B1 B0

0 0 0 0 R7 R6 R5 R4 R3 R2 R1 R0

Note that the inputs have to be doubled because the coefficient gain is 256, whereas the internal gain is 1 / 512, for a net gain of 1/2.

Table 4. Summary of Colorspace Conversion Coefficients

Conversion	KAX	KAY	KAZ	KBX	KBY	KBZ	KCX	KCY	KCZ
RGB to YUV	099	3AA	100	12D	356	32A	03A	100	3D6
RGB to YC_BC_R	083	3B4	0E1	102	36B	344	032	0E1	3DB
YUV to RGB	100	100	100	000	3A8	1C6	167	349	000
YC_BC_R to RGB	149	149	149	000	3CE	102	0CC	398	000

Table 5. Conversion Port Assignments and Alignments

Port	AIN	BIN	CIN	XOUT	YOUT	ZOUT
RGB to YUV	R_{7-0}	G_{7-0}	B_{7-0}	Y_{7-0}	$U_{7-0}(e)$	$V_{7-0}(e)$
RGB to YC_BC_R	R_{7-0}	G_{7-0}	B_{7-0}	Y_{9-0}	$U_{9-0}(e)$	$V_{9-0}(e)$
YUV to RGB	$Y_{8-1}(e)$	$U_{8-1}(e)$	$V_{8-1}(e)$	R_{7-0}	G_{7-0}	B_{7-0}
YC_BC_R to RGB	Y_{9-0}	$C_{B9-0}(e)$	$C_{R9-0}(e)$	R_{7-0}	G_{7-0}	B_{7-0}

Where X_{Y-0} denotes right-justified, (e) denotes sign extension, and X_{Y-1} denotes shifted one bit leftward from a right-justified position.

HSV (HSI) Format Conversions

HSV (or HSI) refers to Hue (color), Saturation (vividness), and Value (intensity or brightness), quantities which are directly related to the human perception of light and color. The V (or I) levels are simply the Y (or luminance) levels. Hue and Saturation are derived from the R-Y and B-Y color difference values of a signal.

HSV Calculations:

Value (V) = Intensity (I) = Y

Hue (H) = Arctan (B-Y/R-Y)

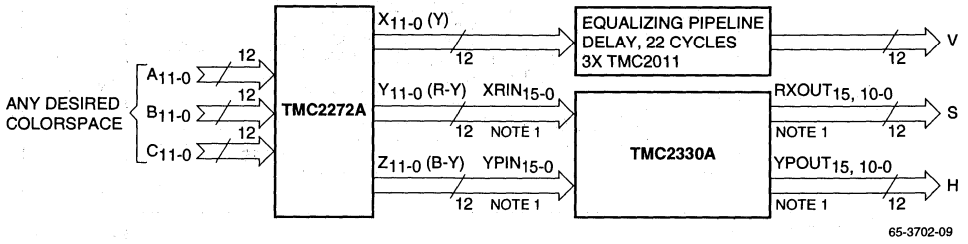
Saturation (S) = $\sqrt{(R-Y)^2 + (B-Y)^2}$

R-Y = S*cos(H)

B-Y = S*sin(H)

One may use two 64Kx8 ROM look-up-tables to calculate Hue and Saturation from R-Y and B-Y in an 8-bit system. However, the finite size of this LUT may limit performance, especially if the TMC2272A's full precision is used. The TMC2330A, developed to translate between rectangular and polar coordinates, can perform the trigonometric transformations to 16 bit precision at 50MHz. These calculations are the same as required in HSV calculations. A 4 Gigabyte x 32 bit LUT can achieve the same accuracy and precision as the TMC2330A, if it is programmed correctly.

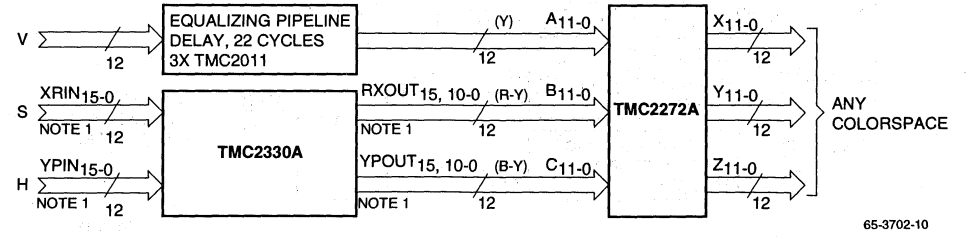
To convert between Y, R-Y, B-Y and HSV, the TMC2272A isn't needed at all; simply use the TMC2330A. To convert between HSV and any other format, use the TMC2330A to translate between HSV and Y, R-Y, B-Y, and use the TMC2272A to translate between Y, R-Y, B-Y and the other format. See Figures 8 and 9.



Notes:

1. Connect TMC2272A MSBs (Bits 11) to TMC2330A MSBs (Bits 15) and also to TMC2330A Bits 14-11. Connect TMC2272A LSBs (Bits 10-0) to TMC2330A LSBs (Bits 10-0). TMC2330A output bits 14-11 are overflow.
2. TMC2272A Y_{11-0} outputs should not be confused with the designation "Y" used to signify the intensity components. The assignment of components to TMC2272A inputs and outputs may be altered through the selection of appropriate coefficients.

Figure 8. Conversion to HSV



Notes:

1. Connect input MSBs (Bits 11) to TMC2330A MSBs (Bits 15) and also to TMC2330A Bits 14-11. Connect input LSBs (Bits 10-0) to TMC2330A LSBs (Bits 10-0).
2. TMC2272A Y_{11-0} outputs should not be confused with the designation "Y" used for an intensity component. Component assignment depends on the coefficient used.

Figure 9. Conversion from HSV

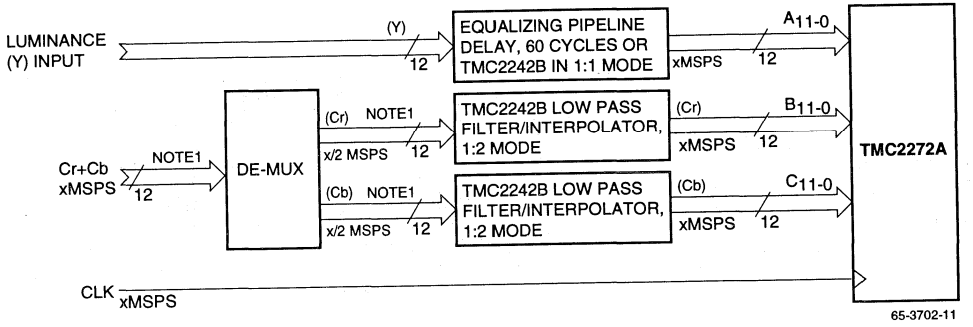
Input Interpolation/Output Decimation and Filtering

In some applications the two color-difference signals (R-Y/B-Y or Cr/Cb, for example) are transmitted at one-half the rate of the luminance (Y) signal. These two color-difference signals are often multiplexed to one signal which is at the same sample rate as the luminance signal.

In many applications, if the color difference signals are already band-limited, it is satisfactory to use the same color difference sample for each two luminance samples. Little improvement is obtained with a simple averaging ([A+B]/2) interpolation filter. If the color difference signal is not band-limited, either of these two methods may yield unsatisfactory results due to aliasing. In this case, a Raytheon TMC2242B digital low-pass (half-band) interpolating filter will correctly band-limit each color difference signal as it is interpolated. See Figure 10.

The same methods are used to decimate the color difference outputs. Simple decimation by removing every other sample of color information may yield unsatisfactory results due to aliasing. This is a problem because the color difference signals have not been transformed with the higher-bandwidth luminance signals and therefore have higher bandwidths than they had before the transform. The best performance is obtained by using a precise low-pass (half-band) decimation filter such as the TMC2242B to remove aliasing components. See Figure 11.

The TMC2242B is a bi-directional, selectable rate filter/interpolator/decimator.



Notes:

1. Width of input paths will vary with source.
2. See TMC2242B Datasheet for further information.

Figure 10. Input Interpolation and Filtering

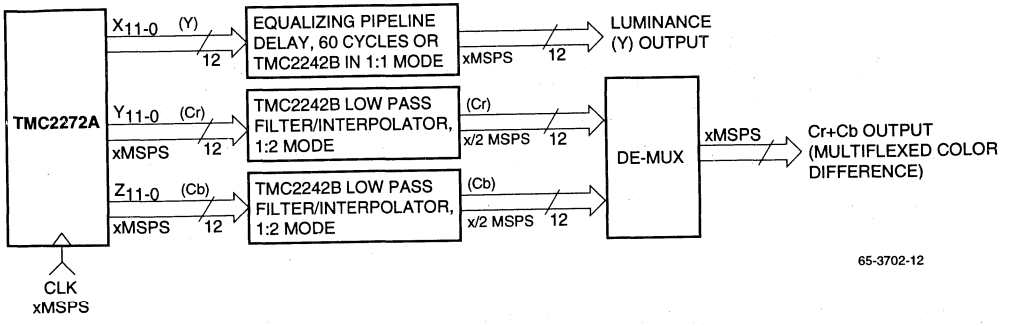


Figure 11. Output Decimation and Filtering

Related Products

- TMC1175 8 bit 40 Msps A/D Converter
- TMC2301 Image Resampling Sequencer
- TMC2302 Image Manipulation Sequencer
- TMC2249A Video Mixer
- TMC2242B Half–Band Filter
- TMC2330A Coordinate Transformer

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2272AH5C	0°C to 70°C	30 MHz	Commercial	120 Pin Plastic Pin Grid Array	2272AH5C
TMC2272AH5C	0°C to 70°C	40 MHz	Commercial	120 Pin Plastic Pin Grid Array	2272AH5C2
TMC2272AH5C	0°C to 70°C	50 MHz	Commercial	120 Pin Plastic Pin Grid Array	2272AH5C3
TMC2272AKEC	0°C to 70°C	30 MHz	Commercial	120 Lead Plastic Quad Flatpack	2272AKEC
TMC2272AKEC	0°C to 70°C	40 MHz	Commercial	120 Lead Plastic Quad Flatpack	2272AKEC2
TMC2272AKEC	0°C to 70°C	50 MHz	Commercial	120 Lead Plastic Quad Flatpack	2272AKEC3

TMC2302

Image Manipulation Sequencer

40 MHz

Features

- Asynchronous loading of control parameters
- Rapid (25ns per pixel) rotation, warping, panning, and scaling of images
- Three-dimensional image addressing capability
- General third-order polynomial transformations in two dimensions on-chip
- Three-dimensional transformation of up to order 1.5 also supported
- Flexible, user-configurable pixel datapath timing structure
- Static convolutional filtering of up to 16 x 16 Pixel (one-pass), 256 x 256 pixel (two-pass) or 256 x 256 x 256 pixel (three-pass) windows
- User-selectable source image subpixel resolution of 2^{-8} to 2^{-16}
- 24-bit (optional 36-bit) positioning precision within the source image space, 48-bit internal precision
- Low power CMOS process
- Available in a 120-pin Plastic Pin Grid Array and 120-lead Metric Quad Flat Pack

Applications

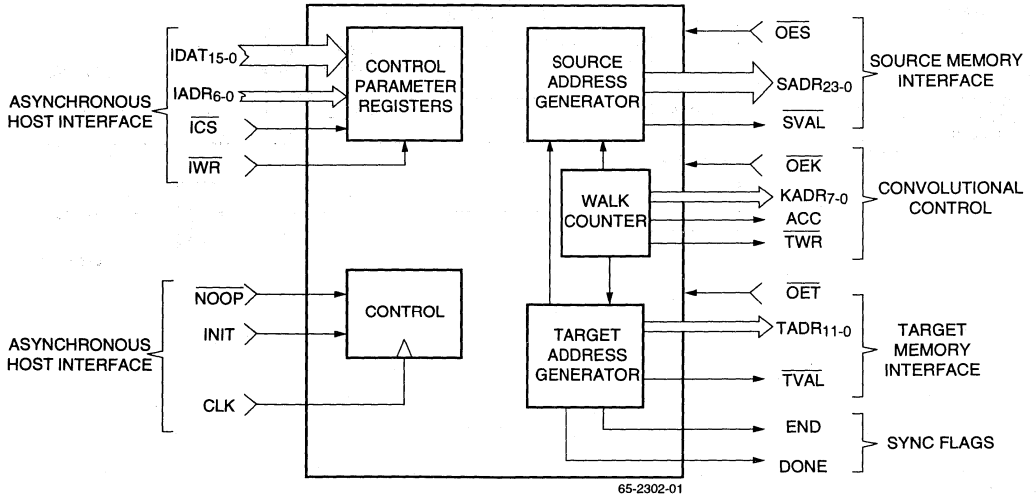
- High-performance video special-effects generators
- Guidance systems
- Image recognition
- Robotics
- High-precision image registration (LANDSAT processing)

Description

The TMC2302 is a high-speed self-sequencing VLSI circuit address generator which supports image resampling, rotation, rescaling, warping, and filtering. It generates input bit plane, interpolation coefficient lookup table, and output bit plane memory addresses along with pixel interpolator control signals.

Similar in architecture to the TMC2301 Image Resampling Sequencer, the TMC2302 features numerous enhancements. In addition to an increase in the maximum clock rate to 40 MHz, the device offers three-dimensional address generation and implements two-dimensional image transformation polynomials of up to third order.

Simplified Block Diagram



Rev. 1.1.1

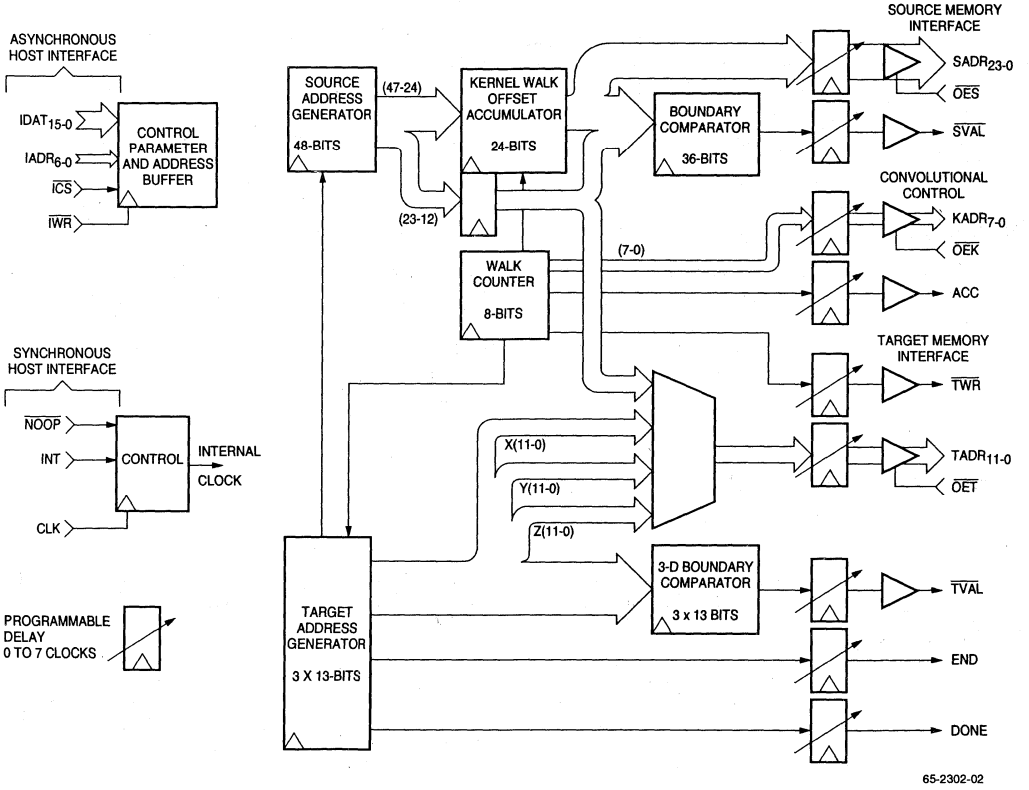
Description (continued)

The TMC2302 can process image data fields with up to 24 bits of binary resolution (2^{24} pixels) per dimension, with 0 to 16-bit subpixel resolution.

A system based on two TMC2302s can nearest-neighbor resample a two-dimensional 512 x 512 pixel image in 6.5 milliseconds, translating, rotating, or warping it, depending on the user-selected transformation parameters. A complete bilinear interpolation of the sample image can be completed in 26 milliseconds (or 6.5ms with a TMC2246A companion chip), while a nearest-neighbor resampling of a 3D image 128 pixels on a side takes only 53 milliseconds with three TMC2302s. Image resampling speed is independent of angle of rotation, degree of warp, or amount of zoom specified.

Along with its original Plastic Pin Grid Array (PPGA) package, the TMC2302 is now offered in a 120-lead Metric Quad FlatPack (MQFP) as well. MQFP Pin assignments, package drawing, and ordering information follow. All electrical, functional, and environmental specifications remain unchanged.

Block Diagram



Functional Description

General Information

The TMC2302 is a versatile, high-performance address generator which can control, under user direction, filtering or remapping of two or three-dimensional images by resampling them from one set of Cartesian coordinates (x, y, z) into a new, transformed set (u, v, w). Most applications utilize two identical devices for two-dimensional, or three devices for three-dimensional, image processing. The host CPU initializes the system by loading the input image buffer RAM with the source image pixel data and the TMC2302s with the image transformation and system configuration control parameters. These parameters are loaded by a separate, asynchronous input clock. The IMS-based system then executes the entire transformation as programmed, generating a DONE flag upon completion of the transform. The user can program the chip to repeat the transform continuously or to halt at the end.

The IMSs continuously compute the target bit plane (u, v) or bit space addresses (u, v, w) in typical line-by-line, raster-scan serial sequence. For each output pixel address, they compute the corresponding remapped source image coordinates, each of whose upper 24 bits become the source bit plane addresses (x, y). An additional lower twelve bits are available through the target address port in the optional extended address mode. Source image addresses may be generated at up to 40MHz, with the corresponding target image addresses then appearing at up to (40/k)MHz, where "k" is the size of the interpolation kernel implemented. In the two-device system, one TMC2302 computes the horizontal coordinates x and u while the other generates the y and v (vertical) addresses. In a three-dimensional system, one additional device would provide the z and w (depth or time) coordinates.

To support a wide range of image transformations, the "row" or x/u device implements a 16-term polynomial of the form:

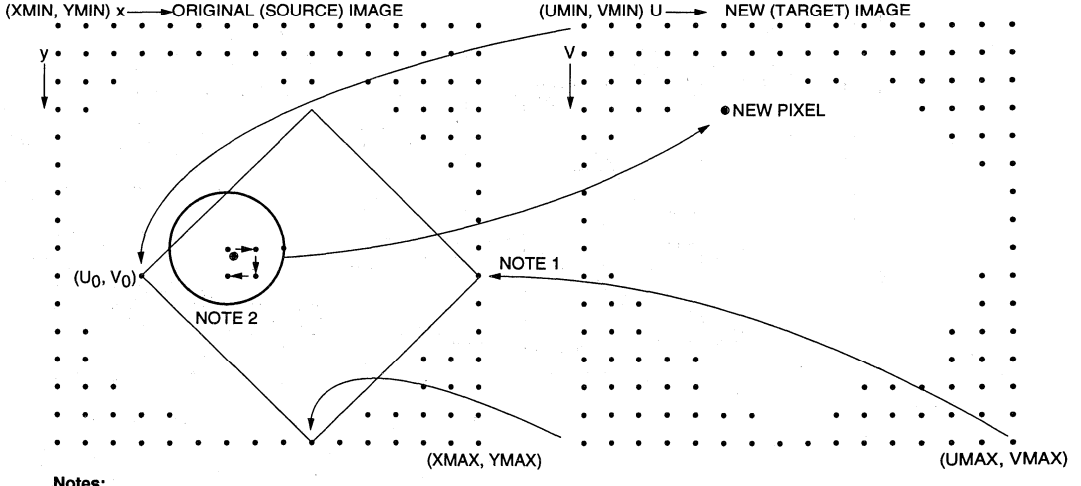
$$x = a + bu + cu^2 + du^3 + ev + fvu + gvu^2 + hvu^3 + iv^2 + jv^2u + kv^2u^2 + lv^2u^3 + mv^3 + nv^3u + ov^3u^2 + pv^3u^3$$

where a through p are the user-defined image transformation parameters. The TMC2302 steps sequentially through the pixels within a user-defined rectangle in the target image space, computing the "old" source image address (x, y, z) corresponding to each "new" target image pixel (u, v, w). User-programmable flags are available to indicate when the source and target image addresses have fallen outside of a defined rectangular area, simplifying the generation of complex images or image windows. Here, u = U-UMIN and v = V-VMIN, where (u,v) is the target address output by the TMC2302.

In the three-dimensional mode, the x/u transformation equation is:

$$x = a + bu + ev + kw + fuv + ivw + luw + juvw$$

See "The Image Transformation Polynomial" section of the Applications Discussion.



Notes:
1. Coordinate transformation U, V pixel mapped into X, Y coordinates.
2. Bilinear pixel interpolation walk. New U, V pixel intensity calculated from surrounding X, Y pixel neigborhood.

Figure 1. Image resampling geometry showing two-dimensional image rotation and expansion

The TMC2302 utilizes an external multiplier-accumulator or interpolator, connected to the system clock, to calculate the interpolated pixel value for each color. The products of the original source image pixel values surrounding the remapped pixel location (interpolation kernel) and the appropriate weights stored in the coefficient lookup table are summed. The resulting new interpolated image pixel value is then stored in the corresponding (U, V, W) memory location in the target image memory buffer. Next, the target image address is incremented by one in the "u" direction until UMAX is reached (end of line), when U is reset to UMIN, and the V counter is incremented to give the first pixel location in the next line. The process is repeated, proceeding line-by-line through the image, until VMAX is reached. In the case of three-dimensional images, the IMS system also steps through each page in the image, incrementing in the "w" direction with the completion of each image plane until WMAX is reached, and the transformation is complete.

The Image Manipulation Sequencer can support any nearest-neighbor, bilinear interpolation, or cubic convolution resampling, according to the user's requirements. Interpolation kernels of more than one pixel require an external interpolation coefficient lookup table and multiplier-accumulator or multiple multiplier array. One, two, and three-pass algorithms are supported. For each output point in a typical two-dimensional single-pass static image filter, the TMC2302 implements a spiralling pixel resampling algorithm, "walking" around the resampling neighborhood in two dimensions and generating the appropriate coefficient table addresses to sum up the interpolated pixel value in the external pixel interpolator. At the end of each walk, the TMC2302 will advance one pixel along the output scan line and then execute the walk for that next pixel. When performing multiple-pass interpolation, the TMC2302 system proceeds along only one dimension per pass, which requires dimensionally separable, preferably orthogonal, coefficients.

A basic, two-dimensional TMC2302-based system is shown in Figure 2. In this typical arrangement, two Image Manipulation Sequencers process the image. The only other components needed beyond the source and target image buffer memories are a multiplier-accumulator or pixel interpolator such as the TMC2246A Image Mixer or TMC2250A Matrix Multiplier, and the Interpolation Coefficient Lookup Table RAM or ROM.

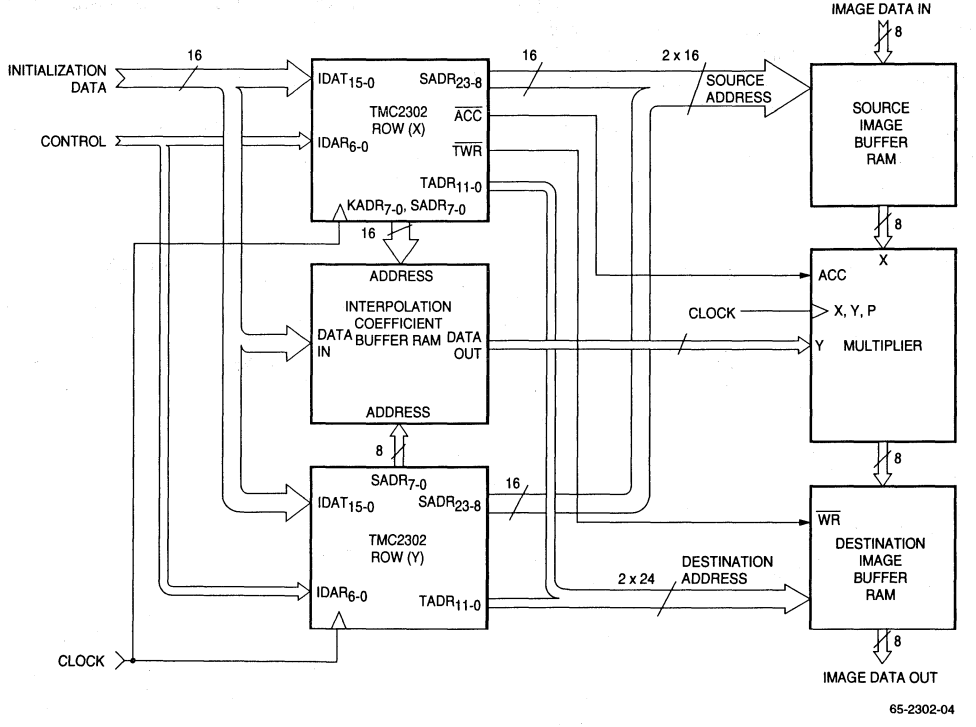
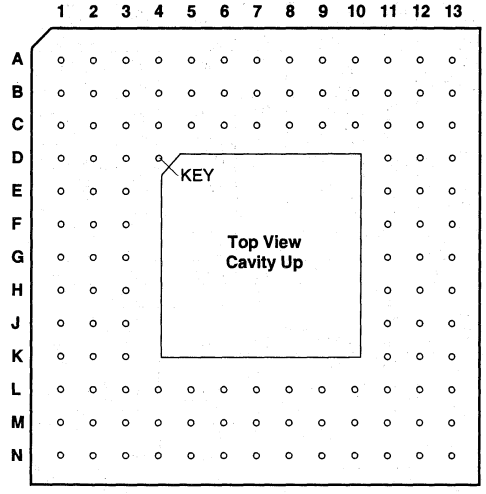


Figure 2. Basic two-dimensional image convolver using TMC2302 IMS with typical 8-bit data path

Pin Assignments

120 Pin Plastic Pin Grid Array, H5 Package

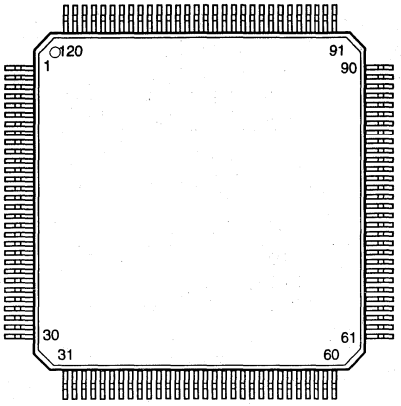


65-2302-05

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	GND	C5	$SADR_{19}$	G11	GND	L10	DONE
A2	$SADR_{16}$	C6	$SADR_{22}$	G12	V_{DD}	L11	V_{DD}
A3	$SADR_{17}$	C7	$IADR_5$	G13	$IDAT_0$	L12	GND
A4	V_{DD}	C8	$IADR_1$	H1	$SADR_5$	L13	$\overline{NOOP}$
A5	$SADR_{21}$	C9	$IDAT_{14}$	H2	$SADR_4$	M1	ACC
A6	$\overline{OES}$	C10	$IDAT_{10}$	H3	GND	M2	$\overline{OEK}$
A7	$IADR_6$	C11	GND	H11	GND	M3	$KADR_6$
A8	$IADR_3$	C12	GND	H12	V_{DD}	M4	$KADR_4$
A9	$IADR_0$	C13	$IDAT_6$	H13	SYNC	M5	$KADR_2$
A10	$IDAT_{15}$	D1	$SADR_{11}$	J1	$SADR_3$	M6	$\overline{OET}$
A11	$IDAT_{12}$	D2	$SADR_{12}$	J2	$SADR_2$	M7	$TADR_0$
A12	$IDAT_9$	D3	GND	J3	V_{DD}	M8	$TADR_3$
A13	V_{DD}	D11	V_{DD}	J11	V_{DD}	M9	$TADR_6$
B1	$SADR_{14}$	D12	$IDAT_5$	J12	CLK	M10	$TADR_9$
B2	$SADR_{15}$	D13	$IDAT_4$	J13	$\overline{IWR}$	M11	GND
B3	V_{DD}	E1	$SADR_9$	K1	$SADR_1$	M12	GND
B4	$SADR_{18}$	E2	$SADR_{10}$	K2	$SADR_0$	M13	$\overline{TVAL}$
B5	$SADR_{20}$	E3	GND	K3	GND	N1	GND
B6	$SADR_{23}$	E11	GND	K11	V_{DD}	N2	$KADR_7$
B7	$IADR_4$	E12	$IDAT_3$	K12	INIT	N3	$KADR_5$
B8	$IADR_2$	E13	$IDAT_2$	K13	GND	N4	$KADR_3$
B9	$\overline{ICS}$	F1	$SADR_7$	L1	$\overline{SVAL}$	N5	$KADR_1$
B10	$IDAT_{13}$	F2	$SADR_8$	L2	V_{DD}	N6	$\overline{TWR}$
B11	$IDAT_{11}$	F3	V_{DD}	L3	NC	N7	$TADR_1$
B12	$IDAT_8$	F11	V_{DD}	L4	V_{DD}	N8	$TADR_2$
B13	$IDAT_7$	F12	GND	L5	GND	N9	$TADR_5$
C1	$SADR_{13}$	F13	$IDAT_1$	L6	$KADR_0$	N10	$TADR_7$
C2	V_{DD}	G1	$SADR_6$	L7	V_{DD}	N11	$TADR_{10}$
C3	V_{DD}	G2	GND	L8	$TADR_4$	N12	$TADR_{11}$
C4	GND	G3	V_{DD}	L9	$TADR_8$	N13	ENDD

Pin Assignments (continued)

120 Lead Metric Quad Flat Pack, KE Package



65-2302-06

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	31	$\overline{OEK}$	61	V_{DD}	91	GND
2	$SADR_{15}$	32	$KADR_7$	62	GND	92	$IDAT_8$
3	$SADR_{14}$	33	V_{DD}	63	$\overline{TVAL}$	93	$IDAT_9$
4	GND	34	$KADR_6$	64	V_{DD}	94	$IDAT_{10}$
5	V_{DD}	35	$KADR_5$	65	GND	95	$IDAT_{11}$
6	$SADR_{13}$	36	$KADR_4$	66	$\overline{NOOP}$	96	$IDAT_{12}$
7	$SADR_{12}$	37	GND	67	INIT	97	$IDAT_{13}$
8	GND	38	$KADR_3$	68	V_{DD}	98	$IDAT_{14}$
9	$SADR_{11}$	39	$KADR_2$	69	GND	99	$IDAT_{15}$
10	$SADR_{10}$	40	$KADR_1$	70	CLK	100	$\overline{ICS}$
11	$SADR_9$	41	$KADR_0$	71	$\overline{IWR}$	101	$IADR_0$
12	V_{DD}	42	$\overline{OET}$	72	GND	102	$IADR_1$
13	$SADR_8$	43	$\overline{TWR}$	73	V_{DD}	103	$IADR_2$
14	$SADR_7$	44	$TADR_0$	74	SYNC	104	$IADR_3$
15	GND	45	V_{DD}	75	V_{DD}	105	$IADR_4$
16	V_{DD}	46	$TADR_1$	76	GND	106	$IADR_5$
17	$SADR_6$	47	$TADR_2$	77	$IDAT_0$	107	$IADR_6$
18	$SADR_5$	48	$TADR_3$	78	$IDAT_1$	108	$\overline{OES}$
19	$SADR_4$	49	$TADR_4$	79	GND	109	$SADR_{23}$
20	GND	50	$TADR_5$	80	V_{DD}	110	$SADR_{22}$
21	$SADR_3$	51	$TADR_6$	81	$IDAT_2$	111	$SADR_{21}$
22	$SADR_2$	52	$TADR_7$	82	$IDAT_3$	112	$SADR_{20}$
23	$SADR_1$	53	$TADR_8$	83	$IDAT_4$	113	V_{DD}
24	V_{DD}	54	$TADR_9$	84	GND	114	$SADR_{19}$
25	$SADR_0$	55	$TADR_{10}$	85	$IDAT_5$	115	$SADR_{18}$
26	$\overline{SVAL}$	56	$TADR_{11}$	86	$IDAT_6$	116	$SADR_{17}$
27	ACC	57	DONE	87	$IDAT_7$	117	$SADR_{16}$
28	GND	58	GND	88	V_{DD}	118	GND
29	V_{DD}	59	NC	89	GND	119	V_{DD}
30	GND	60	ENDD	90	V_{DD}	120	GND

Pin Descriptions

Pin Name	Pin Number		Pin Function Description
	H5 Package	KE Package	
Power			
V_{DD}	C3, C2, F3, G3, J3, L2, L4, L7, L11, K11, J11, H12, G12, F11, D11, A13, A4, B3	1, 5, 12, 16, 24, 29, 33, 45, 61, 64, 68, 73, 75, 80, 88, 90, 113, 119	**Supply Voltage.** The TMC2302 operates from a single +5V supply. All pins must be connected.
GND	D3, E3, G2. H3, K3, N1, L5, M11, M12, L12, K13, H11, G11, F12, E11, C12, C11, C4, A1	4, 8, 15, 20, 28, 30, 37, 58, 62, 65, 69, 72, 76, 79, 84, 89, 91, 118, 120	**Ground.**

Pin Descriptions (continued)

Pin Name	Pin Number		Pin Function Description
	H5 Package	KE Package	
Clocks			
CLK	J12	70	**System Clock .** The pixel clock of the TMC2302 strobes all internal registers except the control parameter preload registers. All timing specifications except those are referenced to the rising edge of CLK.
$\overline{IWR}$	J13	71	**Input Parameter Write Clock.** The internal image transformation and configuration control parameter registers are double buffered to simplify interfacing with system controllers. Depending on the state of the chip selects $\overline{ICS}$, control words input to $IDAT_{15-0}$ and the corresponding addresses presented to $IADR_{6-0}$ are strobed into the outer preload registers on the rising edge of the Input parameter Write clock $\overline{IWR}$. The last parameter must be loaded twice on two consecutive rising edges of $\overline{IWR}$.
Inputs			
$IDAT_{15-0}$	A10, C9, B10, A11, B11, C10, A12, B12, B13, C13, D12, D13, E12, E13, F13, G13	99, 98, 97, 96, 95, 94, 93, 92, 87, 86, 85, 83, 82, 81, 78, 77	**Input Parameter Data.** Configuration and transformation parameter Input Data is presented, along with the appropriate input register address word $IADR_{6-0}$, to the parameter Input Data port, and is latched into the preload registers on the next rising edge of $\overline{IWR}$. Preload register updates are disabled by the chip select control $\overline{ICS}$. See Figure 3.
$IADR_{6-0}$	A7, C7, B7, A8, B8, C8, A9	107, 106, 105, 104, 103, 102, 101	**Input Parameter Address.** The input parameter preload register currently indicated by the Input parameter register Address $IADR_{6-0}$ is loaded with the data presented to input port IDAT on the rising edge of $\overline{IWR}$, as demonstrated in Figure 3.
Outputs			
$SADR_{23-0}$	B6, C6, A5, B5, C5, B4, A3, A2, B2, B1, C1, D2, D1, E2, E1, F2, F1, G1. H1, H2, J1, J2, K1, K2	109, 110, 111, 112, 114, 115, 116, 117, 2, 3, 6, 7, 9, 10, 11, 13, 14, 17, 18, 19, 21, 22, 23, 25	**Source Address.** The 24-bit address of one dimension (X, Y, Z) of the source image pixel value currently being resampled is output through the Source Address port $SADR_{23-0}$. This port can be forced to the high-impedance state by the enable control $\overline{OES}$.
$KADR_{7-0}$	N2, M3, N3, M4, N4, M5, N5, L6	32, 34, 35, 36, 38, 39, 40, 41	**Coefficient Address.** The integer address steps for each dimension of the spiral interpolation walk performed by the TMC2302, as determined by the transform parameter KERNEL, are generated by the internal walk counter and output at the Coefficient Address output port $KADR_{7-0}$. This port can be forced to the high-impedance state by the enable control $\overline{OEK}$.

Pin Descriptions (continued)

Pin Name	Pin Number		Pin Function Description
	H5 Package	KE Package	
$TADR_{11-0}$	N12, N11, M10, L9, N10, M9, N9, L8, M8, N8, N7, M7	56, 55, 54, 53, 52, 51, 50, 49, 48, 47, 46, 44	**Target Address.** The 12-bit address of one dimension (U, V, W) of the target image pixel value just resampled is output through the Target Address Port $TADR_{11-0}$. This port is forced into the high-impedance state by the enable control $\overline{OET}$. $TADR_{11-0}$ can be delayed up to seven clock cycles after the nominal sequence shown in Table 1 by utilization of the pipeline delay parameter PIPTAD. For systems requiring greater spatial resolution in the source image than that offered by the $SADR_{23-0}$ alone, the Target Address Port can be reconfigured to output 12 additional LSBs of the source address by placing the device into the Extended mode, in which case the pipeline delay parameter must be set to 0 to maintain alignment with the current source address port output. See the Device Configuration and Control Parameters section.
Controls			
INIT	K12	67	**Initialize.** The TMC2302 control logic is cleared and initialized for the start of a new image transformation, and the internal working registers are updated with the contents of the current control parameter preload registers when the registered control input INIT is HIGH. The image transformation then commences with the first source image pixel address nine clocks later.
SYNC	H13	74	**Run/Halt.** The user can select between continuous or one-frame operation with the registered input control SYNC. Assuming that INIT remains LOW and $\overline{NOOP}$ remains HIGH, if SYNC remains HIGH at the end of a transform the TMC2302 will begin the next image transformation without interruption. This assumes either that the user is not changing the parameter set, or that a new set of parameters has already been loaded into the preload registers midframe, prior to the beginning of the last line in the transform. If SYNC is LOW during the last clock cycle of a transform, the device will complete the image, having loaded the new transform parameter set during the first clock of the final line of the transform, and halt in the state set on the first clock cycle of the next transform. These outputs are held until SYNC is again brought HIGH, and operation resumes on the next clock. See Figure 5.
$\overline{ICS}$	B9	100	**Input Parameter Chip Select.** The input parameter preload register write clock $\overline{IWR}$, and thus the preloading of all configuration and transformation parameters, is disabled on the next clock when the registered Input parameter Chip Select input is HIGH. When $\overline{ICS}$ returns LOW, they are enabled on the next clock. See Figure 3.
ACC	M1	27	**Accumulate.** The external pixel interpolator or multiplier-accumulator is initialized for a new accumulation of products by the registered Accumulator Control output ACC. On the first cycle of each interpolation walk, this output goes LOW for one cycle, effectively clearing the register by loading in only the first new resampled pixel value. When performing nearest-neighbor resampling, this control will remain LOW throughout the entire transform. This output can be delayed up to seven clock cycles after the nominal sequence shown in Table 1 by the pipeline delay parameter PIPACC. See the Device Configuration and Control Parameters section.

Pin Descriptions (continued)

Pin Name	Pin Number		Pin Function Description
	H5 Package	KE Package	
$\overline{TWR}$	N6	43	**Target Memory Write Enable.** On the last cycle of each interpolation walk, the Target Write Enable goes LOW for one clock cycle, returning HIGH for all but the last cycle of the next walk. When performing nearest-neighbor resampling, this control will remain LOW throughout the entire transform. This output can be forced to the high-impedance state by the enable control $\overline{OET}$, and can be delayed up to seven clock cycles after the nominal sequence shown in Table 1 by the pipe-line delay parameter PIPTWR. See the Device Configuration and Control Parameters section.
$\overline{NOOP}$	L13	66	**No Operation.** Assuming that INIT remains LOW, the internal system clock of the TMC2302 will be disabled on the next clock, halting the current transform, when the registered control input $\overline{NOOP}$ goes LOW. When $\overline{NOOP}$ returns HIGH, normal operation resumes on the next clock. This control does not affect the loading of the configuration and transformation parameter preread registers.
$\overline{OES}$	A6	108	**Source Address Output Enable.** The source address port $SADR_{23-0}$ is enabled when the asynchronous output enable $\overline{OES}$ is LOW. When $\overline{OES}$ is HIGH, the port is in the high-impedance state.
$\overline{OEK}$	M2	31	**Coefficient Address Output Enable.** The interpolation coefficient address port $KADR_{7-0}$ is enabled when the asynchro- nous output enable $\overline{OEK}$ is LOW. When $\overline{OEK}$ is HIGH, the port is in the high-impedance state.
$\overline{OET}$	M6	42	**Target Address Output Enable.** The target address port $TADR_{11-0}$ and target write enable $\overline{TWR}$ are enabled when the asynchronous Target Output Enable $\overline{OET}$ is LOW. When $\overline{OET}$ is HIGH, these outputs are in the high-impedance state. This control functions in both the normal and extended addressing modes.
Flags			
$\overline{SVAL}$	L1	26	**Source Address Valid.** When the current source image address component output is within the working space defined by the parameters XMIN and XMAX (or YMIN, YMAX for the column (Y/V) device or ZMIN, ZMAX for the page (Z/W) device), the Source Address Valid flag $\overline{SVAL}$ for that device is LOW. This flag will go HIGH on the clock in which the corresponding component address falls outside the defined region. In a typical system, the $\overline{SVAL}$ outputs of all IMS devices are OR'ed together to generate a global boundary violation flag. The user might then insert zeroes into the pixel interpolator to ignore that portion of the image outside the defined space, or insert a background color or image. This output can be delayed up to seven clock cycles after the nominal sequence shown in Table 1 by the pipeline delay parameter PIPSVA. See the Device Configuration and Control Parameters section.

Pin Descriptions (continued)

Pin Name	Pin Number		Pin Function Description
	H5 Package	KE Package	
$\overline{TVAL}$	M13	63	**Target Address Valid.** When the current target image addresses are within the working space defined by the parameters UMINI and UMAXI, and VMINI and VMAXI (and WMINI and WMAXI for systems processing three-dimensional images), the Target Address Valid flag $\overline{TVAL}$ for that device is LOW. This flag will go HIGH on the clock in which the current target address outputs fall outside the defined region, which must fall inside the target area defined by UMIN, UMAX, etc. Since each TMC2302 device is programmed with distinct MINI/MAXI parameters and generates a separate $\overline{TVAL}$ flag, the user may define separate two or three-dimensional target space windows for each device. $\overline{TVAL}$ can be delayed up to seven clock cycles after the nominal sequence shown in Table 1 by the pipeline delay parameter PIPTVA. See the Device Configuration and Control Parameters section.
ENDD	N13	60	**End of Dimension.** During the last pixel interpolation walk of a row (X/U device), the last row in a page (Y/V device), or the last page in a three-dimensional transform (Z/W device), the flag ENDD goes HIGH for the entire walk, indicating End of the transform in that dimension. It remains LOW otherwise. This output can be delayed up to seven clock cycles after the nominal sequence shown in Table 1 by the pipeline delay parameter PIPEND. See the Device Configuration and Control Parameters section.
DONE	L10	57	**Done.** On the last clock cycle of the current image transform, the DONE flags on all TMC2302s go HIGH for one clock cycle. On the next clock cycle, all devices output the first addresses and control signals for the next image transform. If SYNC is LOW, the IMS system halts. If SYNC is HIGH, operation continues without interruption. See "SYNC," in the Controls section. This flag can be delayed up to seven clock cycles after the nominal sequence shown in Table 1 by the pipeline delay parameter PIPDON. Also see "PFLS," in the Device Configuration and Control Parameters section.
No Connects			
NC	L3	59	**No Connect.**
	D4	—	**Index Pin.**

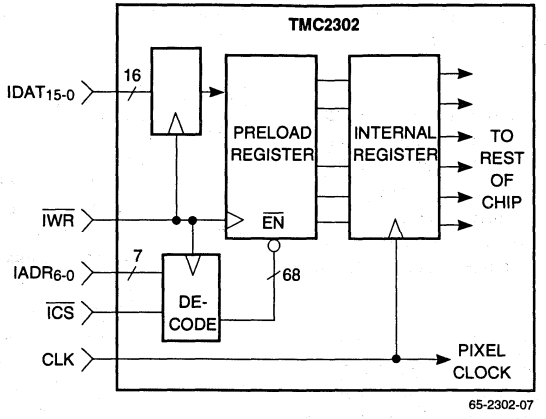


Figure 3. Image transformation and configuration control parameters register structure

Table 1. Nominal Output Signal Timing

$SADR_{23-0}$[1]	ACC	$TADR_{11-0}$	$\overline{TWR}$	END	DONE
$X_{I-1,J,0}$	0	$U_{L-1,M}$	1	0	0
$X_{I-1,J,1}$	1	$U_{L-1,M}$	1	0	0
$X_{I-1,J,2}$	1	$U_{L-1,M}$	1	0	0
•					
•					
•					
$X_{I-1,J,K}$	1	$U_{L-1,M}$	0	1	0
$X_{I,J,0}$	0	$U_{L,M}$	1	1	0
$X_{I,J,1}$	1	$U_{L,M}$	1	1	0
$X_{I,J,2}$	1	$U_{L,M}$	1	1	0
•					
•					
•					
$X_{I,J,K}$	1	$U_{L,M}$	0	1	1

Note:
1. $KADR_{7-0}$ timing identical.

The nominal sequence of address and control signals of a two-dimensional, single-pass-programmed TMC2302 system, with all PIPE parameters set to 0, is shown in Table 1. Here, the values of the last two new target image pixels $U_{L-1,M}$ and $U_{L,M}$ are being calculated, and the beginning and end of the interpolation walks of length K which sample source image pixels in the neighborhod of locations ($X_{I-1,J}$, $X_{I,J}$) can be seen. Utilizing the arrival of the source image address ($SADR_{31-0}$) as a reference point, the other signals shown can be delayed up to seven clock cycles from the nominal timing shown here, allowing the user to configure these outputs to match the timing latencies of his pixel data path structure. Considerable speed and timing variations in image buffer memory, data register, and pixel interpolator structure can thus be accomodated, with minimal corresponding support hardware. Also see "PFLS," in the Device Configuration and Control Parameters section.

Transformation Coefficient and Configuration and Control Parameters

The TMC2302 is intended to act as a co-processor, requiring only that the user program the device to perform the image transformation desired by loading in the appropriate device configuration and transformation control parameters discussed in this section. The user then issues an "Init" command, allowing his system to run unattended until the completion of the image when a "Done" flag is generated to inform the host system.

The capabilities and flexibility of the TMC2302 Image Manipulation Sequencer are apparent when reviewing the following tables which define the transformation coefficient and configuration and control parameters. These tables are broken up into two separate groups. The first parameters discussed are the control words which select the dimension calculated, the functional configuration of each device, the working space in which they will operate, the size of the interpolation kernel desired, and the timing of the various address and control signals involved in handling the pixel data pipeline. The second parameters are the polynomial transform coefficients used in performing image manipulation. The TMC2302 utilizes three levels of internal 48-bit accumulators to calculate these values by forward difference accumulation, generating no significant cumulative spatial error for most applications. The user must be aware that all internal parameter and coefficient registers must be set by the user, including resetting after powerup any unused control words or coefficients.

A major difference between the TMC2302 and the TMC2301 is the elimination of the device interconnects. Instead, the user programs all X, U, V, and W boundaries into all TMC2302 devices. The system's progress through the image is monitored by each device independently and in parallel.

The boundary values are usually identical in all devices in order to maintain synchronous operation.

As mentioned above, the TMC2302 also features user-programmable image data pipeline configuration controls. All output signals except the source and coefficient address outputs can be individually delayed by the user up to seven clocks after the nominal system timing illustrated in Table 1. This allows the user to software-configure the TMC2302s in his system to match his pixel interpolator, image buffer, and interpolation coefficient RAM structure timing.

The user can also program the device to continue into the next image for a set number of clock cycles after the Done flag has appeared. First, this "flushes" the final resampled pixel data word through the interpolation pipeline, all the way to the target image RAM. Also, valid pixel data will then appear on the first clock of the next transform independent of the length of the pixel pipeline, incurring no lost clock cycles.

Device Configuration and Control Parameters

UMIN, VMIN, WMIN — The memory addresses of the target image boundaries corresponding to the top, left side, and front page of the new image being generated are defined in all devices of the user's system by the parameters UMIN, VMIN, and WMIN, respectively. At the beginning of the transformation, the initial source image coordinate (X_0, Y_0, Z_0) will be mapped to this coordinate set. The numeric format assumed is 12-bit unsigned binary integer.

UMAX, VMAX, WMAX — The memory addresses of the target image boundaries corresponding to the bottom, right side, and last page of the image being generated are defined in all devices by the parameters UMAX, VMAX, and WMAX, respectively. These values should be greater than the UMIN/VMIN/WMIN values defined above. Numeric format assumed is unsigned 12-bit binary integer.

Note: The parameter UMAX must exceed UMIN so as to ensure that a minimum of 5 system clock cycles in two-dimensional operation, or 15 clock cycles in three-dimensional operation, pass between the periods in which these two target address values are generated. Thus in 2D nearest neighbor operation UMAX must be 5 greater than UMIN. In 2D bilinear interpolation mode (4-pixel two-dimensional kernel) the distance must be two pixels in the target image (actually enforcing a spacing of 8 system clocks).

UMINI, VMINI, WMINI — The target image addresses corresponding to those of the top, left side, and front page of the 2 or 3 dimensional region indicated by the valid target address flag $\overline{TVAL}$ are UMINI, VMINI, and WMINI, respectively. Thus, to define a valid region beginning at "m," the MINI parameter value is "m," These parameters are assumed to be in 12-bit unsigned binary integer format. Proper $\overline{TVAL}$ operation requires UMIN < UMINI < UMAXI < UMAX, etc.

UMAXI, VMAXI, WMAXI — The target image addresses one more than those of the right side, bottom and back page of the region indicated by the valid target address flag $\overline{TVAL}$ are UMAXI, VMAXI, and WMAXI, respectively. Thus, to define a valid region ending at "n," the MAXI parameter value is "n+1". These parameters are assumed to be in 12-bit unsigned integer format.

XMIN, XMAX — The source image boundaries are defined for each device by the parameters XMIN and XMAX, in the case of the row device. The column device then contains YMIN and YMAX, and the page device (in systems performing three-dimensional operations) ZMIN and ZMAX. The value of XMAX should be greater than XMIN if the boundary violation flag $\overline{SVAL}$ is to operate correctly. These values are assumed to be in 32-bit unsigned binary integer format.

PFLS — The user can set the number of clock cycles that the TMC2302 continues in to the next image following the DONE flag, allowing his system to Flush all control and data pipeline paths and halt after a maximum of seven cycles. The numeric format assumed is three-bit unsigned binary integer.

PTAD, PDON, PEND, PTVA, PSVA, PTWR, PACC — As mentioned above, the control signals and target image pixel addresses generated by the TMC2302 can be delayed up to seven clock cycles after the nominal timing shown in Table 1 by setting the appropriate Pipeline delay word. The numeric format assumed for all delay words is three-bit unsigned binary integer.

XTND — When the user sets the control bit XTND to 1, the TMC2302 operates in an extended-resolution source address bus configuration. Assuming that the user has his own raster scan generator available elsewhere to manage the flow of output pixels from the TMC2302 system, the target address output bus $TADR_{11-0}$ is reconfigured internally into an extension of the source address bus, as $SADR_{11-0}$. The original source address bus $SADR_{23-0}$ is then $SADR_{35-12}$, providing 36 bits of spatial resolution in the source address space. An XTND of 0 puts the device in the standard 24-bit source, 12-bit target address configuration.

E3D — Setting this control bit to 0 indicates a two-dimensional image transform is to be performed. When the E3D is set to 1, a three-dimensional image is assumed, using three TMC2302 devices.

DIM — The user sets each TMC2302 to operate in a specific dimension as follows:

$DIM_{1,0}$	Dimension
00	X/U (Row) Device
01	Y/V (Column) Device
10	Z/W (Page) Device
11	No Operation

MODE — In systems performing the standard two-dimensional spiral interpolation walk, MODE is set to 11, indicating single-pass operation. When performing multiple-pass resampling, the user must set this two-bit control word pass-by-pass in all IMSs, to implement each pass direction. For instance, setting MODE to 00 causes the TMC2302 system to increment only in the X-direction, holding the Y (and Z) addresses constant until the end of that pixel walk. On the next pass through the image, the user sets MODE = 01, with the kernel increment in Y only. In 3D, the IMS system then proceeds again through the (U, V) target image space, walking kernels only along the Z direction.

$Mode_{1,0}$	Resampling Performed
00	X-Pass
01	Y-Pass
10	Z-Pass
11	Two-Dimension Spiral Walk

KERNEL — This parameter determines the size of the interpolation walk performed. To implement a convolutional sum of K+1 pixels, the parameter KERNEL is set to K, up to a maximum of 255. In single-pass operation, this value must be identical in all devices, giving a square interpolation kernel. In multiple-pass operation, however, non- square kernels may be implemented, with different K values in each dimension. Or, the user could utilize a banded memory architecture in two-pass mode to access an entire row or column of a kernel in one clock, completing the entire sum in a single pass through the other dimension of the kernel. Numeric format is 8-bit unsigned integer.

FOV — The user determines the size of each step in an interpolation walk, in terms of the number of source image pixels, by setting the Field Of View control. The binary weighting of the image transformation parameters and source address must be taken into account when determining this value. See Table 6 and the Applications Discussion section. The numeric format assumed is unsigned 16-bit integer.

Table 2. Control Parameter Registers Binary Format (Row, Column or Page Device)

Addr		Format														Limits	
Name	Hex	MSB													LSB	Dec	Hex
UMIN	30				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
UMAX	31				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
UMINI	32				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
UMAXI	33				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
VMIN	34				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
VMAX	35				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
VMINI	36				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
VMAXI	37				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
WMIN	38				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
WMAX	39				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
WMINI	3A				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
WMAXI	3B				2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
XMINL	3C	2^1_5	2^1_4	2^1_3	2^1_2	2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	0	00000000
XMINM	3D	2^3_1	2^3_0	2^2_9	2^2_8	2^2_7	2^2_6	2^2_5	2^2_4	2^2_3	2^2_2	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{32}-1	FFFFFFFF
XMAXL	3E	2^1_5	2^1_4	2^1_3	2^1_2	2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	0	00000000
XMAXM	3F	2^3_1	2^3_0	2^2_9	2^2_8	2^2_7	2^2_6	2^2_5	2^2_4	2^2_3	2^2_2	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{32}-1	FFFFFFFF
PFLS	40		2^2	2^1	2^0													7 0	7 0
PTAD	40					2^2	2^1	2^0										7 0	7 0
PDON	40								2^2	2^1	2^0							7 0	7 0
PEND	40											2^2	2^1	2^0				7 0	7 0
PTVA	40														2^2	2^1	2^0	7 0	7 0
PSVA	41		2^2	2^1	2^0													7 0	7 0
PTWR	41					2^2	2^1	2^0										7 0	7 0
PACC	41								2^2	2^1	2^0							7 0	7 0
XTND	41										XTND								
E3D	41											E3D							
DIM	41												DIM_1	DIM_0					
MODE	41															$MODE_1$	$MODE_0$		
KERNEL	42									2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	255 0	FF 00
FOV	43	2^1_5	2^1_4	2^1_3	2^1_2	2^1_1	2^1_0	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{16}-1 0	FFFF 0000

Transformation Parameter Registers

The Transformation Parameter Word storage register addresses for the X/U device are listed in Table 3, along with the differential terms for each polynomial coefficient for both two and three-dimensional transforms. The polynomial terms for the other IMS device(s) are found by replacing every "X" in the table with a Y (or Z). A TMC2302-based system can perform image manipulations of up to third order in two dimensions, and three-dimensional transforms of up to order 1.5 ("first-and-a-half order"). Also, see "The Image Transformation Polynomial", in the Applications Discussion section.

The notation used to define each polynomial coefficient term in Table 3 is easily interpreted. Each differential is of course defined by a differential in X, followed by the corresponding dependent U, V, or W terms. Thus,

DXUV is equivalent to $d^2X/dUdV$

and DXUUUV to d^4X/dU^3dV.

Table 3. Transformation Polynomial Coefficient Register Addresses

Name	Parameter		Coefficient Word Addresses (hex)		
	2D Term	3D Term	MSW	CSW	LSW
A	X_0	X_0	00	01	02
B	DXU	DXU	03	04	05
C	DXUU		06	07	08
D	DXUUU		09	0A	0B
E	DXV	DXV	0C	0D	0E
F	DXUV	DXUV	0F	10	11
G	DXUUV	X_0	12	13	14
H	DXUUUV	DXU	15	16	17
I	DXVV	DXVW	18	19	1A
J	DXUVV	DXUVW	1B	1C	1D
K	DXUUVV	DXW	1E	1F	20
L	DXUUUVV	DXUW	21	22	23
M	DXVVV		24	25	26
N	DXUVVV		27	28	29
O	DXUUVVV		2A	2B	2C
P	DXUUUVVV		2D	2E	2F

Note: The X_0 and DXU terms must each be loaded into two different registers when performing 3D transforms. Table 3 shows the binary weighting of all of the Transformation Parameter words, which are 48-bit signed fractional binary.

Table 4. Integer Binary Weighting of Transformation Parameters

	Format																Limits	
	MSB															LSB	Dec	Hex
MSB	-2^{47}	2^{46}	2^{45}	2^{44}	2^{43}	2^{42}	2^{41}	2^{40}	2^{39}	2^{38}	2^{37}	2^{36}	2^{35}	2^{34}	2^{33}	2^{32}	2^{48}-1	FFFFFFFFFFFF
CSW	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}		
LSW	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	0	000000000000

Note: A minus sign indicates a sign bit.

Equivalent Circuits and Threshold Levels

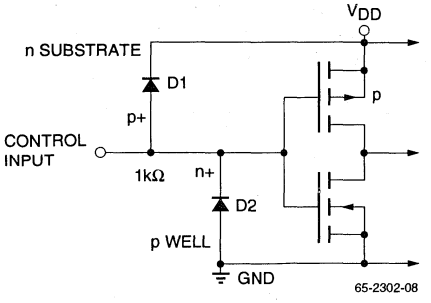


Figure 5. Equivalent Input Circuit

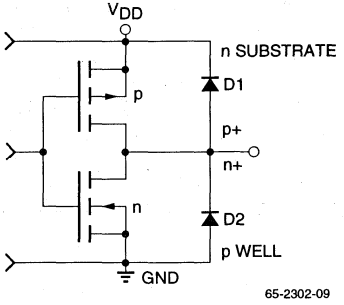


Figure 6. Equivalent Output Circuit

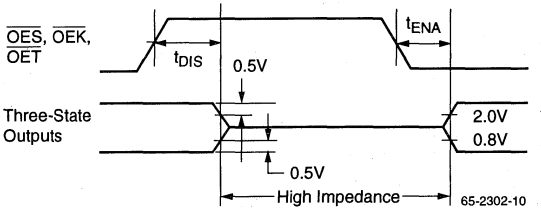


Figure 7. Threshold Levels for Three-State Measurements

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Max	Units
Supply Voltage	-0.5	+ 7.0	V
Input Voltage	-0.5	V_{DD} + 0.5	V
Output applied voltage[2]	-0.5	V_{DD} + 0.5	V
Short-circuit duration (single output in HIGH state to ground)		1	second
Operating, case temperature	-60	130°	C
Junction temperature		175°	C
Lead, soldering temperature (10 seconds)		300°	
Storage temperature	-65	+150°	C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.

Operating Conditions

Parameter		Test Conditions				-1			Units
			Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage		4.75	5.0	5.25	4.75	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW				0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			2.0			V
I_{OL}	Output Current, Logic LOW				8.0			8.0	mA
I_{OH}	Output Current, Logic HIGH				-4.0			-4.0	mA
t_{CY}	Cycle Time	V_{DD} = Min	33			25			ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	15			12.5			ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15			10			ns
t_S	Input Setup Time		10			8			ns
t_H	Input Hold Time		2			2			ns
T_A	Ambient Temperature, Still Air		0		70	0		70	°C

Electrical Characteristics[1]

Parameter		Test Conditions	Min	Max	Units
I_{DDQ}	Supply Current Quiescent	V_{DD} = Max, V_{IN} = 0V		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz, $\overline{OES}$ = $\overline{OEK}$ = $\overline{OET}$ = 5V		70	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	-10		µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		V
I_{OZL}	High-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	-40		µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40	µA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.	-20	-70	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10	pF

Note:

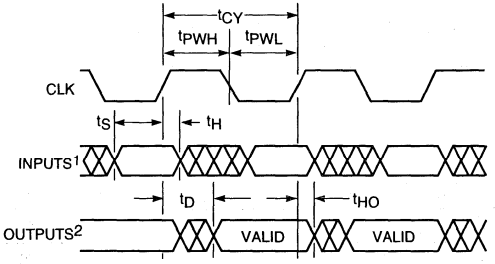
1. Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching Characteristics

Parameter		Test Conditions			-1		Units
			Min	Max	Min	Max	
t_{DO}	Output Delay	V_{DD} = Min, C_{LOAD} = 25pF		15		12	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 25pF	4		4		ns
t_{ENA}	Three-State Output Enable Delay[1]	V_{DD} = Min, C_{LOAD} = 25pF		12		12	ns
t_{DIS}	Three-State Output Disable Delay[1]	V_{DD} = Min, C_{LOAD} = 25pF		15		15	ns

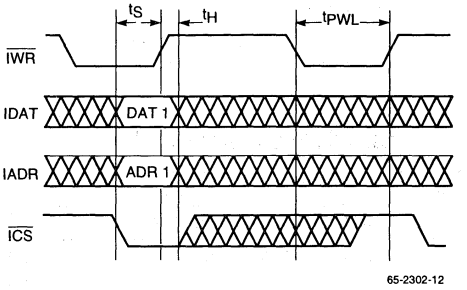
Note:
1. All transitions are measured at a 1.5V level except for t_{DIS} and T_{EMA}.

Timing Diagrams



Notes:
1. Except $\overline{OES}$, $\overline{OET}$, and $\overline{OEK}$.
2. Assumes $\overline{OES}$, $\overline{OET}$, and $\overline{OEK}$ = LOW. All pipeline latency parameters set to 0.

Figure 4a. Timing Diagram, Pixel Clock, Control, and Outputs



Value "DAT 1" is loaded into address "ADR 1" on the second rising edge of $\overline{IWR}$, since $\overline{ICS}$ = 0, having been acquired by the input register on the first edge.

Figure 4b. Timing Diagram, Preload Parameters

Applications Discussion

The Image Transformation Polynomial

On any given clock cycle, when performing a two-dimensional geometric transformation the addresses output by the row (X/U) TMC2302 are generated by forward difference accumulation according to the following third-order polynomial:

$$x(u,v) = a + bu + cu^2 + du^3 + ev + fvu + gvu^2 + hvu^3 + iv^2 + jv^2u + kv^2u^2 + Iv^2u^3 + mv^3 + nv^3u + ov^3u^2 + pv^3u^3 + FOV \bullet CAX(ca)$$

The polynomial utilized for three-dimensional transforms is:

$$x(u,v,w) = a + bu + ev + kw + fuv + ivw + luw + juvw + FOV \bullet CAX\ (ca)$$

where $0 \le u \le$ UMAX-UMIN, $0 \le v \le$ VMAX-VMIN, $0 \le w \le$ WMAX-WMIN, and the polynomials for the column or page devices are obtained by replacing the x by a y or z, as appropriate.

FOV is the 16-bit field-of-view parameter, normally set so that the spiral walk proceeds in single-pixel steps. FOV can be increased to expand the step size and thus the spiral walk, subsampling the image. See Table 2 and Table 6. Also, CAX(ca) is the current value of the coefficient address. See the Interpolation Coefficient Lookup Table Addressing. If the spiral walk isn't used, CAX = 0 and FOV is ignored.

We can reform the two-dimensional polynomial as:

$$x(u,v) = (a + ev + iv^2 + mv^3) + (b + fv + jv^2 + nv^3)u + (c + gv + kv^2 + ov^3)u^2 + (d + hv + Iv^2 + pv^3)u^3,$$

and retain the simpler three-dimensional form:

$$x(u, v, w) = a + bu + ev + kw + fuv + ivw + luw + juvw$$

and define each of the polynomial coefficients in arithmetic terms as shown in Table 5.

Table 5. Transformation Polynomial Coefficients

	Parameter			
	Two-Dimensional		Three-Dimensional	
Name	Term	Coefficient	Term	Coefficient
A	X_0	a	X_0	a
B	DXU	b + c + d	DXU	b
C	DXUU	2c + 6d	—	0
D	DXUUU	6d	—	0
E	DXV	e + i + m	DXV	e
F	DXUV	f + g + h + j + k + l + n + o + p	DXUV	f
G	DXUUV	2(g + k + o) + 6(h + l +p)	X_0	a
H	DXUUUV	6(h + l + p)	DXU	b
I	DXVV	2i + 6m	DXVW	i
J	DXUVV	2(j + k + l) + 6(n + o + p)	DXUVW	j
K	DXUUVV	4k + 12l + 12o + 36p	DXW	k
L	DXUUUVV	12l + 36p	DXUW	l
M	DXVVV	6m	—	0
N	DXUVVV	6(n + o + p)	—	0
O	DXUUVVV	12o + 36p	—	0
P	DXUUUVVV	36p	—	0

Understanding the Polynomial Coefficients

An Overview

As the formulae indicate, the source address is a polynomial function of the two (or three) dimensions of the target address. Each of the 16 terms of the equation is of the form:

$$\frac{d_m + n + p^x}{du^m\, dv^n\, dw^P},$$

and may be treated approximately as a mixed partial difference of order m, n, and p.

The simplest term, X_0, is a zeroeth (non-) function of the target addresses; it specifies the source address point corresponding to the upper left point in the target space. X_0 generates image translation or "pan."

The next-simplest terms, dX/dU and dY/dV, govern the relative scales of the source and target images, i.e., how large a step in source space corresponds to a unit step in the corresponding direction in the target space. As long as the cross-terms, dX/dV and dY/dU, are zero, this is a straight scale ("zoom") operation, without rotation or shear.

The first-order cross terms, dX/dV and dY/dU, generate source space displacements perpendicular to unit displacements in the target space, thereby causing shearing of the image. In conjunction with the parallel source terms described above, they govern rotation, shear, and scaling of the image.

Although the actions of the higher-order terms become progressively difficult to describe, all terms behave essentially as partial differences of various orders, and a little thought and common sense will generally lead the user to the proper conclusions. For example, the term dXUU (using the notation of Table 3) is a horizontal scale factor which increases as one progresses across each row, causing a quadratic horizontal warp. In fact, all terms of the form dmX/dUm or dnY/dVn cause only stretching of the image, never rotation.

Interpolation Coefficient Lookup Table Addressing

The external coefficient lookup table RAM stores the interpolation coefficient values used to calculate the value of the new pixel. These values are selected by the user, allowing maximum filtering flexibility. In simple filtering applications, the source and target pixel addresses map one-to-one, and only one interpolation coefficient set is required. These integer addresses are generated for each dimension by the internal walk counters of each TMC2302.

However, applications performing a coordinate transformation will almost always generate non-integer source pixel addresses; that is, the U (or V) locations will not map to the X (or Y) addresses exactly, and a fractional source address components are generated. The user must then expand the interpolation coefficient lookup table to include spatially-corrected values, as detemnined by the subpixel resolution of the system.

The TMC2301 Image Resampling Sequencer allows the user to trade subpixel resolution against interpolation step size by obtaining the interpolation coefficient addresses directly from the fractional part of the source address. The TMC2302 gives the user 16 different interpolation bit weighting positions. The complete Interpolation Coefficient Address for that dimension then consists of both the 8-bit interpolation walk address $KADR_{7-0}$, weighted to match the source address binary point by the parameter FOV, and the fractional portion of the source pixel address $SADR_{23-0}$, to the desired subpixel resolution. See Table 6.

Internal and External Data Formats

The source address value output by the TMC2302 is a 24-bit two's complement number, with binary point assignable by the user anywhere in the 16 lower bits. The Extended mode appends 12 additional fractional bits for greater output precision. All internal computations include these 24 plus 12 bits, plus an additional 12 lower bits, for 48-bit precision. See Table 6.

Intemally, each TMC2302's source address (X, Y,or Z) generator computes a 48-bit address through a mode-specific accumulation of the sixteen 48-bit user-specified resampling parameters. The 24 most significant bits of the final accumulation emerge via the source address port whereas the "extend" mode makes the 12 next most-significant bits available at the target address port. The 12 least significant bits are truncated internally.

Source Address Bit Weighting and Setting the Binary Point

When performing nearest-neighbor resampling, the user may arbitrarily trade source image size against subpixel resolution merely by adhering to a single binary point position for all resampling parameters. For example, if the binary point follows the 16 most significant bits in each resampling parameter, then it will appear following the source address'16 most significant bits, leaving 8 (20 in extended mode) bits of subpixel resolution on $SADR_n$.

Since the TMC2302 has no internal limiter, the user should select the source address weighting appropriately. Moving the source address connections to the right and reducing the resampling parameters accordingly, reduces the chance of arithmetic overflow while increasing arithmetic round-error.

In any filtering or resampling operation performing an interpolation walk, the user should set the Field or View (FOV) parameter according to the desired binary point position determined above, as follows. To provide 2^{24} integral pixel positions per dimension, with no subpixel resolution, set FOV = 001 (hex). For 2^{23} positions with 1-bit (0,5) subpixel resolution, FOV = 0010 (hex). Similarly, for 2^9 positions and 15-bit subpixel resolution. FOV = 8000 (hex). As shown in Table 6, using the parameter FOV the user effectively "shifts" the bit weight of the coefficient address word $KADR_{7-0}$ to match the established location of his source address binary point. In each case, the EXTEND mode provides 12 additional bits of subpixel resolution but eliminates the separate target or raster address, which must then be generated elsewhere in the user's system.

Table 6. Relative Bit Weighting – Source Address

Weight Word	2^{47} 2^{46}...2^{40}	2^{39} 2^{32}	2^{31}...2^{25} 2^{24}	2^{23}...2^{16}	2^{15}...2^{12}...2^{8}	2^{7}...2^{0}
Transform Parameters	-47 46					0
Internal Source Address Generator	-47 46					0
Source Address Output $SADR_{23-0}$	-23 22...16	15 8	7 ... 1 0			
Extended Mode Only $TADR_{11-0}$				11 ... 4	3 ... 0	
$KADR_{7-0}$						
FOV = 0001			2^{7} ... ... 2^{0}			
FOV = 0002		2^{7}	2^{6} ... 2^{0}			
• • •						
FOV = 8000	2^{7}...2^{1}	2^{0}				

Note: A minus sign indicates a sign bit.

Utilization of the Image Boundary Flags $\overline{SVAL}$ and $\overline{TVAL}$

As mentioned above, the TMC2302 provides two programmable valid address, or boundary flags. The source valid flag $\overline{SVAL}$ is asserted when the current source image address output for that device's source image dimension is within the space defined by the configuration parameters XMIN and XMAX, or YMIN and YMAX, or ZMIN and ZMAX, as appropriate. Also, the target valid flag $\overline{TVAL}$ is available to indicate when the current target image address values fall within the space defined by the configuration parameters UMINI, UMAXI, VMINI, VMAXI, and also WMINI and WMAXI in three-dimensional systems. Note that all of these parameters are each programmed into each individual TMC2302. Thus, the user could define two (or three) different working spaces, one indicated by each IMS device.

Figure 8 may help clarify the relationships among (X_0, Y_0, Z_0), (UMIN, VMIN, WMIN), and (UMAX, VMAX, WMAX), for the two-dimensional case. With positive first derivatives, (X_0, Y_0) and (UMIN, VMIN) represent the upper left corners of the original image and the new destination field, respectively. The lower right corner of the new transformed image is located at (UMAX, VMAX); the location of the corresponding corner of the original image depends on the values of the derivatives.

Not to be confused with (X_0, Y_0), the points (XMIN, YMIN) and (XMAX, YMAX) define the "usable" rectangular portion of the original image which is indicated by the valid address flag $\overline{SVAL}$; points (X, Y) lying outside this region are ignored in most resampling and filtering applications.

Specifically, the point (X_0, Y_0) is the location from which the TMC2302 system begins the image resampling sequence. Every step beyond that point in the source image space is defined by the address generators implementing the image transformation polynomials.

The valid source address flag feature permits one to construct a mosaic of several abutting subimages in the (X, Y) plane, without danger of edge effect interference between adjacent subimages. Note in the figure that the upper right corner of the resampled source image lies outside the admissible region; in practice, the values fetched at these locations will not be included in the convolutional sums. One might, for instance, program these boundary values to alert the system that an edge is being approached and to modify the interpolation coefficients appropriately, or simply to ignore pixel values outside the defined space.

The $\overline{TVAL}$ however is utilized somewhat differently. Working in unison with the target address working space defined by UMIN/UMAX, etc. the target address valid flag could be programmed to delineate image areas other than the immediate working space, and the flag of each TMC2302 to indicate the unique regions anywhere within the target image. With this flexibility, the user can generate windows, "picture-in-picture" composite multiple images, or simply switch to a background image or border color. To make $\overline{TVAL}$ function properly, the used must set UMIN < UMINI < UMAXI < UMAX; likewise for V and, if used, W.

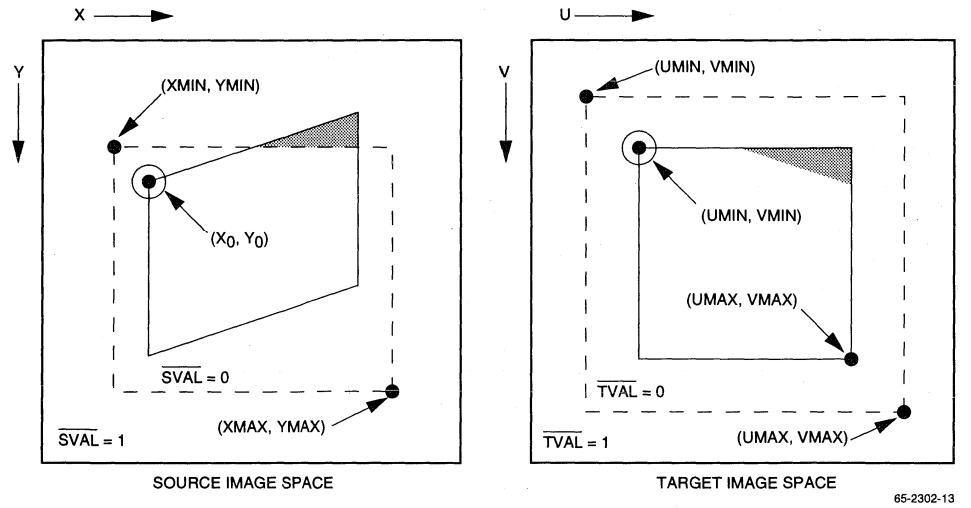
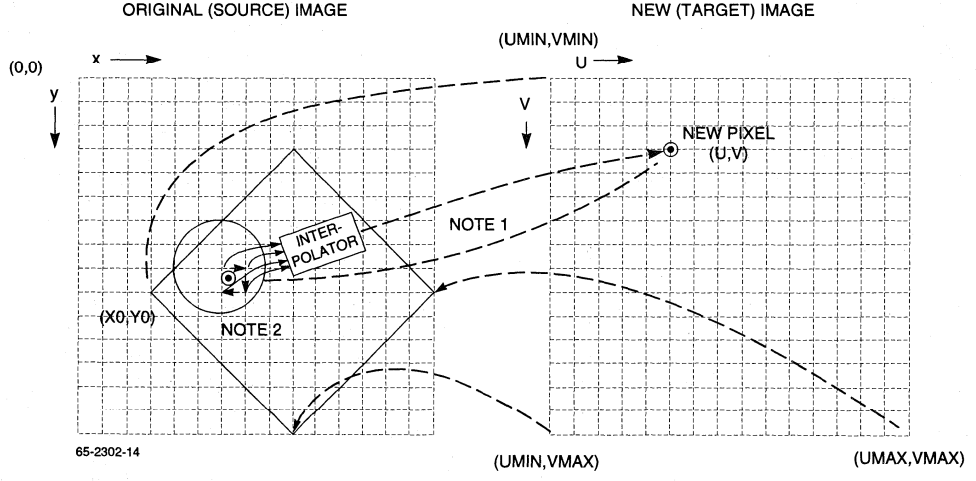


Figure 8. Pixel maps demonstrating source and destination image boundaries, violation flags, and image clipping (note shaded areas)

Real-Time Bilinear Interpolation Using the TMC2302 or TMC2301

Image transformations and translations in bit mapped systems are done by taking an original (source) image, performing coordinate remapping and interpolation, then restoring the image into a new (destination) image space. The coordinates are remapped according to a transformation polynomial. The polynomial, evaluated at destination pixel addresses, maps the transformed pixel addresses (U, V) to pixel addresses in the original image addresses (U,V) to pixel addresses in the original image (X, Y), i.e., (X, Y) is a polynomial function of (U, V).



Notes:

1. Coordinate transformation: Each pixel in (U, V) space is mapped to a location in (X,Y) space.
2. Interpolation: Unless the pixel in (U, V) space coincides with one in (X, Y) space, its amplitude must be estimated as a weighted average of these of the surrounding pixels in (X, Y) space. If the interpolation is done serially, throughput suffers in proportion to the size of the interpolation kernel. However, the interpolation can also be performed in parallel to preserve throughput, as discussed here.

The TMC2302 Image Manipulation Sequencer

The TMC2302 is a controller/address generator, around which an image filtering and resampling system can be built. Under limited supervision from an external controller, the TMC2302 will generate the sequence of memory read and write addresses to transform, resample, and/or filter an image. In all cases, it fetches data from one image buffer, governs its convolution with a user-specified kernel of coefficients, and directs the results to another image memory space. With 24-bit source address buses the device can operate from a source frame size of, for example, 64K X 64K pixels with spatial resolution of 1/256th pixel. A simplified block diagram of the TMC2302 is shown in Figure 9. Although the 24 source addresses bits of each TMC2302 can be designed arbitrarily with the source image address bus, assume for the current discussion that bits SADR (19:8) will correspond to the source image address and that SADR (7:4) therefore denote subpixel postponing to 1/16 pixel resolution.

The basic 2-D system, shown in Figure 10, consists of data source and destination memories, coefficient lookup table, multplier-accumulator, TMC2302 parameters to define the transform and starts the operation. It may also control the loading of the source image into RAM and provide the screen refresh, if needed.

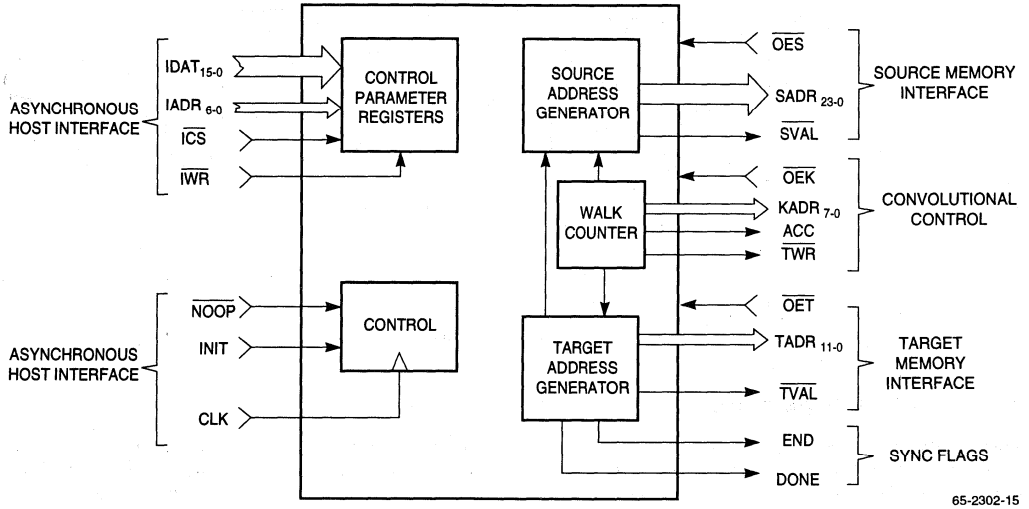


Figure 9. TMC2302 Block Diagram

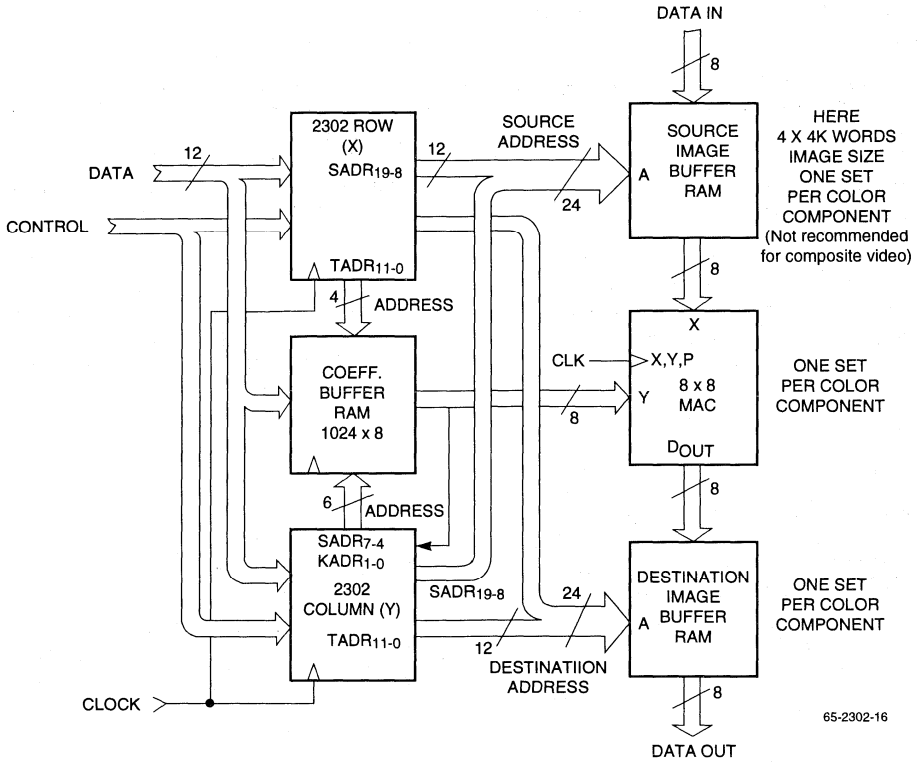


Figure 10. Basic 2-D Image Transformation Systems

Inexact Transformations

In many cases, evaluation of the transformation polynomial results in a non-integer result (non-integer address in the X, Y image space). In such cases, the mapping from original image to transformed image will be inexact. When this occurs, the user has the option of accepting the pixel "nearest" to the address generated, or performing interpolation, a weighted average of nearby pixel values. Using the pixel nearest the address generated is the fastest method since one transformed pixel can be generated on every cycle.
The resulting image will include jagged biasing artifacts, however. Performing several transformations on the same image will further degrade the resulting image.

One Cycle Bilinear Interpolation

A better image can be obtained by finding the four pixels nearest the address generated and performing a weighted averaging to determine the new pixel value. This is known as bilinear interpolation. The TMC2302 eases the control logic required for such a function by performing a "walk" around the four closest pixels in the source image space. Essentially, the TMC2302 generates the addresses of the four walk cycles, and the current source pixel is multiplied by a weighting factor and accumulated by the external multiplier accumulator. At the end of the walk, the accumulated result from the four nearest pixels is written into the destination image RAM and the TMC2302 proceeds to the next group. The obvious disadvantage to using bilinear interpolation is that one new destination pixel is generated only on every fourth cycle, reducing the output bandwidth by a factor of four.

One method of "real-time" bilinear interpolation consists of using four memories, each containing the entire source image. The storage arrangement of the pixels within each bank is staggered so that a single address fed to the memories will result in the access of the proper four pixel group. The TMC2302 is programmed to generate the nearest neighbor address and the four nearest pixels are accessed simultaneously and input to the four independent multipliers of a TMC2246 quad multiplier chip. The four pixels are multiplied by their associated weighting factors and added to determine the destination pixel sum. The major drawback of this method is the prohibitive cost for additional memory required to store four copies of the entire source image. For large images, the memory cost and additional board space makes this method unattractive.

A more efficient method is to divide the original source image into a "four-color checker board" and to store it into four separate pixel memory banks, each containing 14th of the source image. Since the image is separated into four memories rather than duplicated, no additional image memory is required. The goal is to separate the image so that any square of four adjacent pixel locations can be accesssed simultaneously. Thus, the user must organize the memory such that the four pixels of any cluster will reside in separate memory banks. With this method, only one set of address generators (TMC2302s) is necessary, and only a slight address modification is necessary to guarantee that the correct group of pixels is accessed and output to the multipliers. Since all pixels are accessed simultaneously, no "walk" is performed, and the TMC2302 system is able to generate one destination pixel on each clock cycle. For example, a 1024 x 768 image can be generated every 20ms for a frame refresh rate of 50Hz. This method which will be described below.

Using "Banded" Pixel Memory

The TMC2302 should be programmed to do "nearest-neighbor" transformations (Kernel, K = 0 and the X_0 and Y_0 start boundaries programmed without 1/2-LSB truncation debiasing to force address truncation when evaluating the transformation polynomial for the nearest-pixel address). The biased X_0 and Y_0 guarantee that when the exact pixel address falls within the region of four pixels, the upper leftmost pixel will always be selected as "nearest-neighbor."

The key to performing real-time bilinear interpolation is to arrange the pixels in memory so that the four pixels of every grouping will be stored in separate memories. The four nearest pixels will form a square. Figure 11 shows a sample 512 x 512 pixel image and the arrangement into four separate memory banks designated A, B, C, and D. It can be seen from the figure that any (square) grouping of four pixels will have one pixel located in each bank. Thus, one memory sector will hold even row-even column pixels, another, even-row-add column pixels, etc.

$A_{0,0}$ (0,0)	$B_{0,0}$ (1,0)	$A_{1,0}$ (2,0)	$B_{1,0}$ (3,0)	$A_{2,0}$ (4,0)	$B_{2,0}$ (5,0)	$A_{3,0}...A_{255,0}$ (6,0)...(510, 0)	$B_{255.0}$ (511, 0)
$C_{0,0}$ (0,1)	$D_{0,0}$ (1,1)	$C_{1,0}$ (2,1)	$D_{1,0}$ (3,1)	$C_{2,0}$ (4,1)	$D_{2,0}$ (5,1)	$C_{3,0}...C_{255,0}$ (6,1)...(510,1)	$D_{255,0}$ (511,1)
$A_{0,1}$ (0,2)	$B_{0,1}$ (1,1)	$A_{1,1}$ (2,1)	$B_{1,1}$ (3,2)	$A_{2,1}$ (4,2)	$B_{2,1}$ (5,2)	$A_{3,1}...A_{255,1}$ (6,2)...(510,2)	$B_{255,1}$ (511,2)
$C_{0,1}$ (0,3)	$D_{0,1}$ (1,3)	$C_{1,1}$ (2,3)	$D_{1,1}$ (3,3)	$C_{2,1}$ (4,3)	$D_{2,1}$ (5,3)	$C_{3,1}...C_{255,1}$ (6,3)...(510,3)	$D_{255,1}$ (511,3)
$A_{0,2}$ (0,4)	$B_{0,2}$ (1,4)	$A_{1,2}$ (2,4)	$B_{l,2}$ (3,4)	$A_{2,2}$ (4,4)	$B_{2,2}$ (5,4)	$A_{3,2}...A_{255,2}$ (6,4)...(510,4)	$B_{255,2}$ (511,4)
$C_{0,2}$ (0,5)	$D_{0,2}$ (1,5)	$C_{1,2}$ (2,5)	$D_{1,2}$ (3,5)	$C_{2,2}$ (4,5)	$D_{2,2}$ (5,5)	$C_{3,2}...C_{255,2}$ (6,5)...(510,5)	$D_{255,2}$ (511,5)
$A0_{0,255}$ (0,510)	$B_{0,255}$ (1,510)	$A_{1,255}$ (2,510)	$B_{1,255}$ (3,510)	$A_{2,255}$ (4,510)	$B_{2,255}$ (5,510)	$A_{3,255}...A_{255,255}$ (6,510)...(510,510)	$B_{255,255}$ (511,510)
$C_{0,255}$ (0,511)	$D_{0,255}$ (1,511)	$C_{1,255}$ (2,511)	$D_{1,255}$ (3,511)	$C_{2,255}$ (4,511)	$D_{2,255}$ (5,511)	$C_{3,255}...C_{255,255}$ (6,511)...(510,511)	$D_{255,255}$ (511,511)

Figure 11. Source Image Pixel Arrangement

Subscripts i, j for A, B, C, and D denote relative addresses in memory respectively.

The ordered pairs (a, b) denote the physical (X,Y) pixel locations and the TMC2302 SAPR(X) and SADR(Y) address outputs.

The pixels of the original image should be stored in the source RAM banks as shown in Figure 12. The original source image can be loaded by decoding the TMC2302 least significant address bits ($SADR_X(8)$. $SADR_Y(8)$ to determine the memory bank for the pixel while the most-significant address bits ($SADR_X(19:9)$, $SADR_Y(19:9)$) are used as common address lines to all four memory banks.

TMC2302 Address		Bank A	Bank B	Bank C	Bank D
XA μ,	YA_μ	$XA_0YA_0 = 00$	$XA_0YA_0 = 01$	$XA_0YA_0 = 10$	$XA_0YA_0 = 11$
0	0	$A_{0,0}$	$B_{0,0}$	$C_{0,0}$	$D_{0,0}$
0	1	$A_{0,1}$	$B_{0,1}$	$C_{0,1}$	$D_{0,1}$
0	2	$A_{0,2}$	$B_{0,2}$	$C_{0,2}$	$D_{0,2}$
0	255	$A_{0,255}$	$B_{0,255}$	$C_{0,255}$	$D_{0,255}$
1	0	$A_{1,0}$	$B_{1,0}$	$C_{1,0}$	$D_{l,0}$
1	1	$A_{1,1}$	$B_{1,1}$	$C_{1,1}$	$D_{1,1}$
1	2	$A_{1,2}$	$B_{1,2}$	$C_{1,2}$	$D_{1,2}$
255	254	$A_{255,254}$	$B_{255,254}$	$C_{255,254}$	$D_{255,254}$
255	255	$A_{255,254}$	$B_{255,254}$	$C_{255,254}$	$D_{255,254}$

Figure 12. Memory-Pixel Arrangement

In the following discussion, the TMC2302 address outputs $SADR_X$ and $SADR_Y$ will be designated as:

Horizontal Source

XA_0	Least-Significant Horizontal Source X-Address Bit $SADR_X$ (8)
XAμ	Upper Horizontal Source Address Bits $SADR_X$ (19:9)
YA_0	Least-Significant Vertical Source Y-Address Bit $SADR_X$(8)
Yaμ	Upper Vertical-Source Address Bits $SADR_Y$ (19:9)

Interpolation Kernel

$P_{i,j}$ $P_{i,j+1}$

* - actual Pixel

$P_{i+1,j}$ $P_{i+1,j+1}$

Figure 13. TMC2302 Serial Walk Sequence in real time bilinear resampling, this is executed in parallel

When the transformation polynomial is evaluated and the resulting pixel address falls within a group of four nearby pixels (non-integer result), the TMC2302 will always choose the upper leftmost pixel (P_{ij}) as the nearest neighbor (due to the fractional address truncation in the X and Y directions). Since the four pixels will reside in independent banks, the upper leftmost pixel might be located in any of the four memory banks (A,B,C, or D). The bank which contains the nearest neighbor must be known, since in each case, different memory address modification is required to select the correct pixel from each bank.

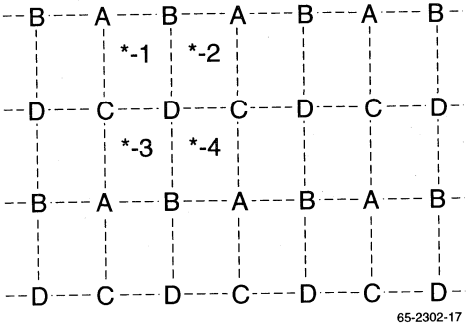


Figure 14. Possible Selections for Nearest Neighbor

Memory Address Modification

Using the address LSBs (XA_0, YA_0) from each TMC2302 external logic can determine which bank contains the nearest neighbor. (This same decoding is used when loading the original image into the source image RAMs.)

Case*	XA_0	YA_0	Nearest Neighbor (Upper Leftmost) Pixel
1	0	0	A Memory Bank contains Nearest Neighbor
2	0	1	B Memory Bank contains Nearest Neighbor
3	1	0	C Memory Bank contains Nearest Neighbor
4	1	1	D Memory Bank contains Nearest Neighbor

*from Figure 14 above

Addressing for each memory bank (A, B, C, D) is done using the uppermost address bits (XA_μ) of the TMC2302s. The LSB of each TMC2302 is used to determine both the upper leftmost pixel and the address modification required. In the following paragraphs, the lower case subscripts (i,j) denote the address of a pixel within a given memory bank (A, B, C, or D), and XA, YA are used to denote physical address outputs of the TMC2302 pairs.

Pixel address modification use to access the correct four pixel group is determined as follows:

Case A:
$A_{i,j}$ is nearest upperleft neighbor,
(No address modifications)
($XA_0 = YA_0 = 0$)

$A_{i,j}$ $B_{i,j}$
*
$C_{i,j}$ $D_{i,j}$

Figure 15. Pixel Memory Mapping for A = Upper Leftmost

Memory Addressing Becomes:
A address = XA_μ, YA_μ
B address = XA_μ, YA_μ
C address = XA_μ, YA_μ
D address = XA_μ, YA_μ
i.e., no modification is required.

Case B:
$B_{i,j}$ is upperleft neighbor,
(Modify X component of A & C memory addresses)
($XA_0 = 1$, $YA_0 = 0$)

$B_{i,j}$ $A_{i+1,j}$
*
$D_{i,j}$ $C_{i+1,j}$

Figure 16. Pixel Memory Pattern for B = Upper Leftmost

Memory Addressing Becomes:
A address = ($XA_\mu + 1$, YA_μ)
B address = (XA_μ, YA_μ)
C address = ($XA_\mu + 1$, Ya_μ)
D address = (XA_μ YA_μ)

Case C:
Ci,j is upperleft neighbor,
(Modify Y component of A & B memory addresses)
($XA_0 = 0$, $YA_0 = 1$)

$C_{i,J}$ $D_{i,j}$
*
$A_{i,j+1}$ $B_{i,j+1}$

Figure 17. Pixel Pattern for C = Upper Leftmost

Memory Addressing Becomes:
A address = XA_μ $YA_\mu + 1$
B address = XA_μ, $Ya_\mu + 1$
C address = XA_μ, YA_μ
D address = XA_μ, YA_μ

Case D:
Di,j is the nearest neighbor
(Modify A, B & C addresses, X and Y components)
($XA_0 = 1$, $YA_0 = 1$)

$D_{i,j}$ $C_{i+1,j}$
*
$B_{i,j+1}$ $A_{i+1,j+1}$

Figure 18. Pixel Pattern for D = Upper Leftmost

Memory Addressing Becomes:
A address = $XA_\mu + 1$, $YA_\mu + 1$
B address = XA_μ, $Ya_\mu + 1$
C address = $XA_\mu + 1$, YA_μ
D address = XA_μ, YA_μ

Taking a close look at the address modifications required for each case above, a simple pattern can be seen. This pattern leads to a set of address modification "rules" based on the values of the least-signficant address bits from the TMC2301s (XA_0 and YA_0). These rules are:

When $YA_0 = 0$. (Case A & B)
No modificaton to the Y address component (YA_μ) is necessary.

When $YA_0 = 1$, (Case C & D)
The Y component (YA_μ) of addresses to the A & B memory banks must be incremented by 1.

When $XA_0 = 0$. (Case A & C)
No modification to the X address component (XA_μ) is necessary.

When $XA_0 = 1$, (Case B & D)
The X component (XA_μ,) of addresses to the A & C memory banks must be incremented by 1.

A system can easily be designed to modify the pixel memory addresses according to the above criteria, to select the correct four pixels to be interpolated. Rather than actually performing a "conditional" address increment as discussed above. It requires less logic simply to add the LSB address bit to the memory bank addresses (XA_μ, YA_μ). Figure 12 shows the logic to perform the required address modifications. The addition (XA_μ, + XA_0, YA_μ, +YA_0) can be done using half-adders with the XA_0 (YA_0) address output of the TMC2302 connected to the carry-in of each adder. It can also be done using high-speed programmable logic.

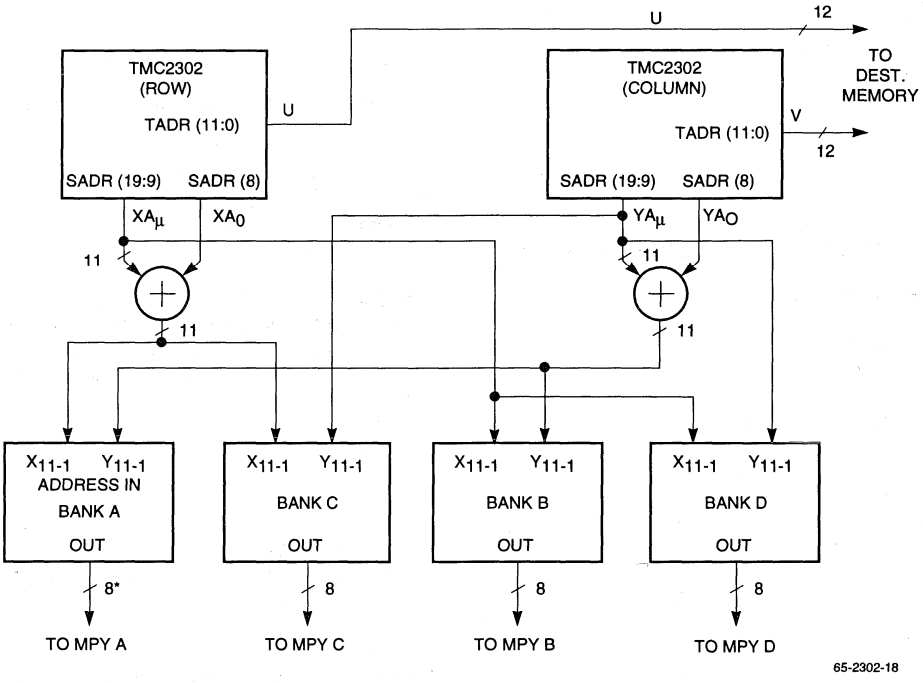
Note: Only modifications to the source image memory are necessary. The destination image memory may be arranged in a linear or other type array as required by the refresh circuitry.

Coefficient Memory

Typically, the 4 highest fractional source address bits from each TMC2302 (SADR (7:4) in the example) are used to reflect the offset from the nearest XA (YA) pixel location.

With spatial resolution of 4 bits in both the X and Y directions, there can be as many as 256 unique coefficient values. This requires a coefficient memory of at least 256 bytes. However, as shown below, each of the four different cases requires its own set of 256 coefficients.

One-cycle bilinear interpolation requires four independent coeffficient memories, so that a parallel multiplication can be performed with the four pixel values.



*Number of bits of intensity per pixel, per column component, typically 8 to 12.

Figure 19. Memory Address Modification

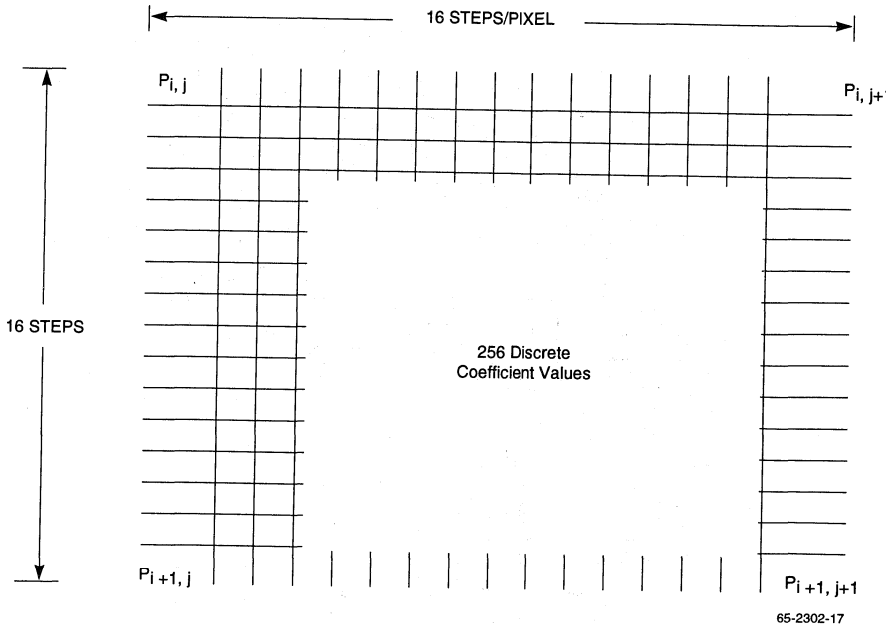


Figure 20. Intrapixel Resolution

Similar to determining the correct four pixel group, the coefficients must take into account the memory bank (A, B, C, or D) that contains the upper leftmost pixel, and adjust the coefficients accordingly. These adjustments are necessary since the fractional address outputs ($SADR_X$ 7:4), $SADR_Y$ (7,4) from the TMC2302s reflect the spatial distance only from the upper leftmost pixel within the pixel group. Assuming that the fractional addresses $SADR_X$ (7:4) and $SADR_Y$ (7:4) plus the integer LSBs $SADR_X$ (8) and $SADR_Y$ (8) are to be used directly to address the 1024-byte coefficient memory, the loading of the coefficients is shown below with $F_X = SADR_X$ (7:4) and $F_Y = SADR_Y$ (7:4) Case A through D are the same as discussed previously for the pixel address modifications.

Case A:
A is nearest neighbor ($XA_0 = 0$, $YA_0 = 0$)

Coeff A = $(1 - f_X) * (1 - f_Y)$
Coeff B = $(f_X) *(1 - f_Y)$
Coeff C = $(1 - f_X) * (f_Y)$
Coeff D = $f_X * f_Y$

Case B:
B is nearest neighbor ($XA_0 = 0$, $YA_0 = 1$)

Coeff A = $f_X * (1-f_Y)$
Coeff B = $(1-f_X) * (1-f_Y)$
Coeff C = $f_X * f_Y$
Coeff D = $(1-f_X)f_Y$

Case C:
C is nearest neighbor ($XA_0 = 1$, $YA_0 = 0$)

Coeff A = $(1- f_X) f_Y$
Coeff B = $f_X f_Y$
Coeff C = $(1 - f_X) (1 - f_Y)$Coeff D = $f_X * (1 - f_Y)$

Case D:
D is nearest neighbor ($XA_0 = 1$, $YA_0 = 1$)

Coeff A = $f_X f_Y$
Coeff B = $(1 - f_X)f_Y$
Coeff C = $f_X * (1 - f_Y)$
Coeff D = $(1 - f_X) (1 - f_Y)$

Incorporating the concepts outlined in this discussion, the final system for one-cycle blinear interpolation is shown in Figure 21. This figure shows a small increase in logic over the basic 2-D system shown in Figure 10. The additional logic required includes: TMC2246 (rather than a single multiply/accumulate), and three additional coefficient memories. Some additional decoding logic is required to load the four pixel memory banks as well as some data and address pipelining (registering) to meet timing requirements. The solution, however, provides an increased pixel bandwidth, by a factor of four, and only a small increase in part count.

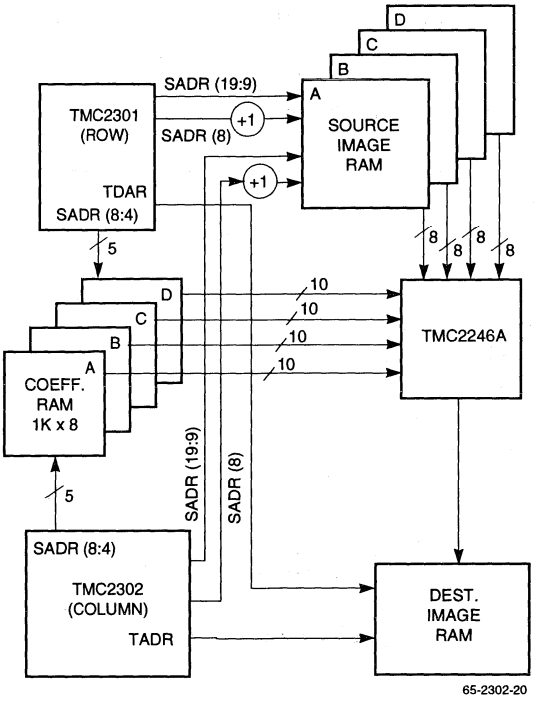


Figure 14. One-Cycle Bilinear Interpolation System

Related Products

- TMC2301 Image Resampling Sequencer
- TMC2246A Image Filter
- TMC2249A Digital Mixer
- TMC2242B Half-Band Filterll

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2302H5C	0°C to 70°C	30MHz	Commercial	120 Pin Plastic Pin Grid Array	2302H5C
TMC2302H5C1	0°C to 70°C	40 MHz	Commercial	120 Pin Plastic Pin Grid Array	2302H5C1
TMC2302KEC	0°C to 70°C	30MHz	Commercial	120 Lead Metric Quad FlatPack	2302KEC
TMC2302KEC1	0°C to 70°C	40MHz	Commercial	120 Lead Metric Quad FlatPack	2302KEC1

TMC2330A

Coordinate Transformer

16 x 16 Bit, 50 MOPS

Features

- Rectangular-to-Polar or Polar-to-Rectangular conversion at guaranteed 50 MOPS pipelined throughput rate
- Polar data: 16-bit magnitude, 32-bit input/16-bit output phase
- 16-bit user selectable two's complement or sign-and-magnitude rectangular data formats
- Input register clock enables and asynchronous output enables simplify interfacing
- User-configurable phase accumulator for waveform synthesis and amplitude, frequency, or phase modulation
- Magnitude output data overflow flag (in Polar-to-Rectangular mode)
- Low power consumption CMOS process
- Single +5V power supply
- Available in a 120-pin plastic pin grid array package (PPGA) and 120-pin metric quad flatpack (MQFP)

Applications

- Scan conversion (phased array to raster)
- Vector magnitude estimation
- Range and bearing derivation
- Spectral analysis
- Digital waveform synthesis, including quadrature functions
- Digital modulation and demodulation

Description

The TMC2330A VLSI circuit converts bidirectionally between Cartesian (real and imaginary) and Polar (magnitude and phase) coordinates at up to 50 Mops (Million Operations Per Second).

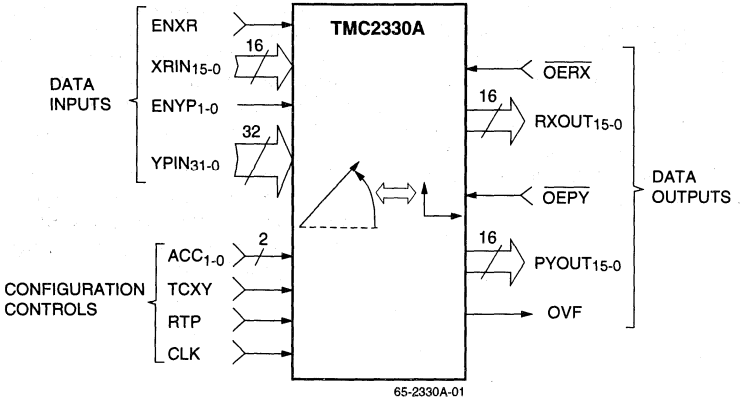
In its Rectangular-to-Polar mode, the TMC2330A can extract phase and magnitude information or backward "map" from a rectangular raster display to a radial (e.g., range-and-azimuth) data set.

The Polar-to-Rectangular mode executes direct digital waveform synthesis and modulation. The TMC2330A greatly simplifies real-time image-space conversion between the radially-generated image scan data found in radar, sonar, and medical imaging systems, and raster display formats.

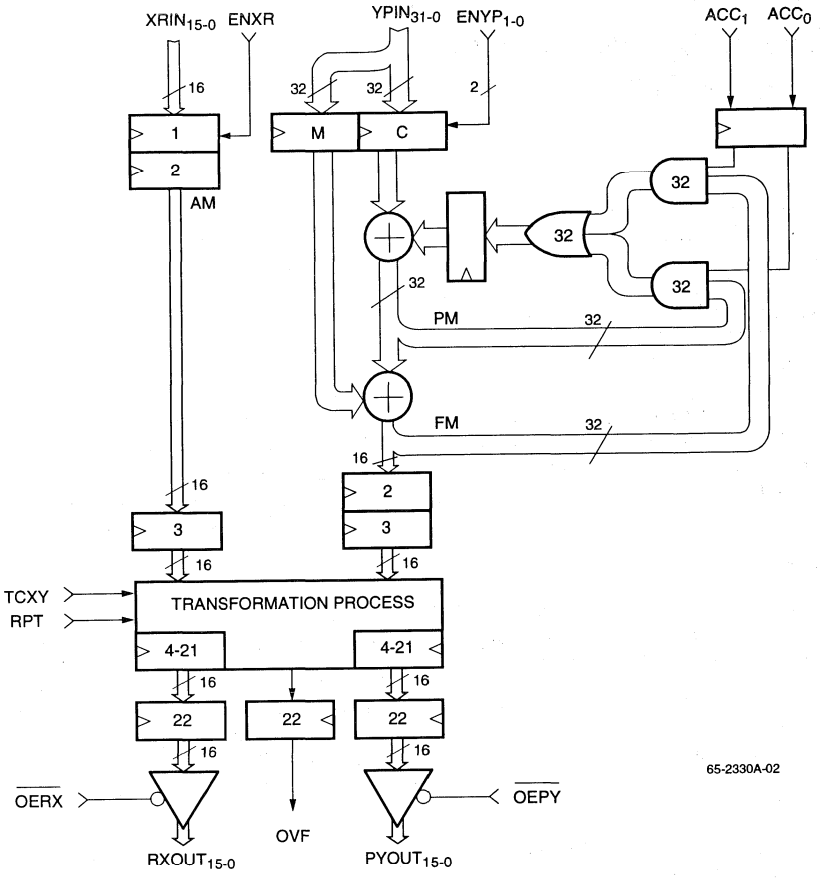
All input and output data ports are registered, and a new transformed data word pair is available at the output every clock cycle. The user-configurable phase accumulator structure, input clock enables, and asynchronous three-state output bus enables simplify interfacing. All signals are TTL compatible.

Fabricated in a submicron CMOS process, the TMC2330A operates at up to the 50 MHz maximum clock rate over the full commercial (0 to 70°C) temperature and supply voltage ranges, and is available in low-cost 120-pin plastic pin grid array and metric quad flatpack packages.

Logic Symbol



Block Diagram



Functional Description

The TMC2330A converts between Rectangular (Cartesian) and Polar (Phase and Magnitude) coordinate data word pairs. The user selects the numeric format and transformation to be performed (Rectangular-To-Polar or Polar-To-Rectangular), and the operation is performed on the data presented to the inputs on the next clock. The transformed result is then available at the outputs 22 clock cycles later, with new output data available every 20ns with a 50MHz clock. All input and output data ports are registered, with input clock enables and asynchronous high-impedance output enables to simplify connections to system buses.

When executing a Rectangular-To-Polar conversion, the input ports accept 16-bit Rectangular coordinate words, and the output ports generate 16-bit magnitude and 16-bit phase data. The user selects either two's complement or sign-and-magnitude Cartesian data format. Polar magnitude data are always in magnitude format only. Since the phase angle word is modulo 2π, it may be regarded as either unsigned or two's complement format (Tables 1 and 2).

In Polar-To-Rectangular mode, the input ports accept 16-bit Polar magnitude and 32-bit phase data, and the output ports produce 16-bit Rectangular data words. Again, the user selects between two's complement or sign-and-magnitude Cartesian data format.

Table 1. Data Input/Output Formats—Integer Format

Port	RTP	TCXY	Bit # 31	30	29	...	16	15	14	...	0	Format	
XRIN	0	X						2^{15}	2^{14}	...	2^{0}		U
XRIN	1	0						NS	2^{14}	...	2^{0}		S
XRIN	1	1						-2^{15}	2^{14}	...	2^{0}		T
YPIN	0	X	$\pm2^{0}$	2^{-1}	2^{-2}	...	2^{-15}	2^{-16}	2^{-17}	...	2^{-31}	(xπ)T/U	
YPIN	1	0	NS	2^{14}	2^{13}	...	2^{0}						S
YPIN	1	1	-2^{15}	2^{14}	2^{13}		2^{0}						T
RXOUT	0	0						NS	2^{14}		2^{0}		S
RXOUT	0	1						-2^{15}	2^{14}		2^{0}		T
RXOUT	1	X						2^{15}	2^{14}		2^{0}		U
PYOUT	0	0						NS	2^{14}		2^{0}		S
PYOUT	0	1						-2^{15}	2^{14}		2^{0}		T
PYOUT	1	X						$\pm2^{0}$	2^{-1}		2^{-15}	(xπ)T/U	

Table 2. Data Input/Output Formats—Fractional Format

Port	RTP	TCXY	Bit # 31	30	29	...	16	15	14	...	0	Format	
XRIN	0	X						2^{0}	2^{-1}	...	2^{-15}		U
XRIN	1	0						NS	2^{-1}	...	2^{-15}		S
XRIN	1	1						-2^{0}	2^{-1}	...	2^{-15}		T
YPIN	0	X	$\pm2^{0}$	2^{-1}	2^{-2}	...	2^{-15}	2^{-16}	2^{-17}	...	2^{-31}	(xπ)T/U	
YPIN	1	0	NS	2^{-1}	2^{-2}	...	2^{-15}						S
YPIN	1	1	-2^{0}	2^{-1}	2^{-2}	...	2^{-15}						T
RXOUT	0	0						NS	2^{-1}	...	2^{-15}		S
RXOUT	0	1						-2^{0}	2^{-1}	...	2^{-15}		T
RXOUT	1	X						2^{0}	2^{-1}	...	2^{-15}		U
PYOUT	0	0						NS	2^{-1}	...	2^{-15}		S
PYOUT	0	1						-2^{0}	2^{-1}	...	2^{-15}		T
PYOUT	1	X						$\pm2^{0}$	2^{-1}	...	2^{-15}	(xπ)T/U	

Notes:

1. -2^{15} denotes two's complement sign bit.
2. NS denotes negative sign, i.e., '1' negates the number.
3. $\pm2^{0}$ denotes two's complement sign or highest magnitude bit – since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as $+\pi$ or $-\pi$.
4. All phase angles are in terms of π radians, hence notation "xπ."
5. If ACC = 00, YPIN(15-0) are "don't cares."
6. Formats:
   T = Two's Complement
   S = Signed Magnitude
   U = Unsigned

HEX	U	T	S
FFFF	65535	–1	-32767
...	...	...	...
8001	32769	-32767	-1
8000	32768	-32768	0
7FFF	32767	32767	32767
...	...	...	...
0001	1	1	1
0000	0	0	0

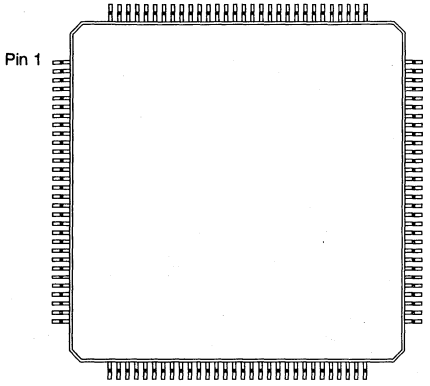
BROADCAST VIDEO

Static Control Inputs

The controls RTP and TCXY determine the transformation mode and the assumed numeric format of the Rectangular data. The user must exercise caution when changing either of these controls, as the new transformed results will not be seen at the outputs until the entire internal pipe (22 clocks) has been flushed. Thus, these controls are considered static.

Pin Assignments

120-Pin MQFP

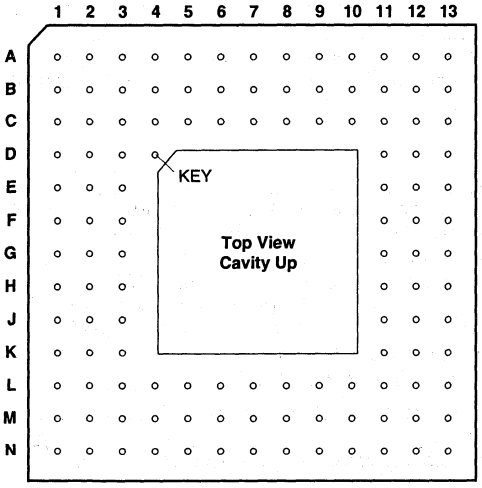


65-2330A-03

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VDD	31	GND	61	VDD	91	VDD
2	PYOUT4	32	YPIN9	62	XRIN1	92	RXOUT9
3	PYOUT3	33	YPIN10	63	XRIN2	93	RXOUT8
4	GND	34	VDD	64	GND	94	GND
5	PYOUT2	35	YPIN11	65	XRIN3	95	RXOUT7
6	PYOUT1	36	YPIN12	66	XRIN4	96	RXOUT6
7	PYOUT0	37	YPIN13	67	XRIN5	97	RXOUT5
8	VDD	38	YPIN14	68	GND	98	GND
9	$\overline{\text{OEPY}}$	39	YPIN15	69	XRIN6	99	RXOUT4
10	GND	40	YPIN16	70	XRIN7	100	RXOUT3
11	RTP	41	YPIN17	71	XRIN8	101	RXOUT2
12	CLK	42	VDD	72	XRIN9	102	VDD
13	GND	43	YPIN18	73	XRIN10	103	RXOUT1
14	TCXY	44	YPIN19	74	XRIN11	104	RXOUT0
15	ENPY	45	YPIN20	75	XRIN12	105	OVF
16	GND	46	GND	76	GND	106	GND
17	ENPY1	47	YPIN21	77	XRIN13	107	PYOUT15
18	ACC0	48	YPIN22	78	XRIN14	108	PYOUT14
19	ACC1	49	YPIN23	79	XRIN15	109	PYOUT13
20	VDD	50	VDD	80	VDD	110	VDD
21	YPIN0	51	YPIN24	81	$\overline{\text{OERX}}$	111	PYOUT12
22	YPIN1	52	YPIN25	82	GND	112	PYOUT11
23	YPIN2	53	YPIN26	83	RXOUT15	113	PYOUT10
24	YPIN3	54	YPIN27	84	VDD	114	VDD
25	YPIN4	55	YPIN28	85	RXOUT14	115	PYOUT9
26	YPIN5	56	YPIN29	86	RXOUT13	116	PYOUT8
27	YPIN6	57	YPIN30	87	RXOUT12	117	PYOUT7
28	GND	58	YPIN31	88	GND	118	GND
29	YPIN7	59	ENXR	89	RXOUT11	119	PYOUT6
30	YPIN8	60	XRIN0	90	RXOUT10	120	PYOUT5

Pin Assignments (continued)

121-Pin PPGA



65-2330A-04

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	PYOUT5	C5	GND	G11	GND	L10	YPIN31
A2	PYOUT7	C6	VDD	G12	XRIN12	L11	VDD
A3	PYOUT8	C7	GND	G13	RXIN13	L12	XRIN3
A4	PYOUT10	C8	VDD	H1	ACCO	L13	XRIN4
A5	PYOUT12	C9	GND	H2	ACC1	M1	YPIN6
A6	PYOUT14	C10	GND	H3	VDD	M2	YPIN9
A7	PYOUT15	C11	VDD	H11	XRIN9	M3	YPIN11
A8	RXOUT0	C12	RXOUT11	H12	XRIN10	M4	YPIN13
A9	RXOUT2	C13	RXOUT13	H13	XRIN11	M5	YPIN16
A10	RXOUT4	D1	$\overline{OEPY}$	J1	YPIN0	M6	YPIN18
A11	RXOUT6	D2	PYOUT0	J2	YPIN1	M7	YPIN20
A12	RXOUT8	D3	GND	J3	YPIN3	M8	YPIN23
A13	RXOUT10	D11	GND	J11	GND	M9	YPIN25
B1	PYOUT3	D12	RXOUT14	J12	XRIN7	M10	YPIN28
B2	PYOUT4	D13	RXOUT15	J13	XRIN8	M11	ENXR
B3	PYOUT6	E1	RTP	K1	YPIN2	M12	XRIN1
B4	PYOUT9	E2	GND	K2	YPIN4	M13	XRIN2
B5	PYOUT11	E3	GND	K3	GND	N1	YPIN8
B6	PYOUT13	E11	VDD	K11	GND	N2	YPIN10
B7	OVF	E12	GND	K12	XRIN5	N3	YPIN12
B8	RXOUT1	E13	$\overline{OERX}$	K13	XRIN6	N4	YPIN15
B9	RXOUT3	F1	TCKY	L1	YPIN5	N5	YPIN17
B10	RXOUT5	F2	GND	L2	YPIN7	N6	YPIN19
B11	RXOUT7	F3	CLK	L3	GND	N7	YPIN21
B12	RXOUT9	F11	VDD	L4	VDD	N8	YPIN22
B13	RXOUT12	F12	RXIN15	L5	YPIN14	N9	YPIN24
C1	PYOUT1	F13	RXIN14	L6	VDD	N10	YPIN26
C2	PYOUT2	G1	ENPY1	L7	GND	N11	YPIN29
C3	VDD	G2	ENPY0	L8	VDD	N12	YPIN30
C4	GND	G3	GND	L9	YPIN27	N13	XRIN0

Pin Descriptions

Pin Name	Pin Number MQFP	Pin Number PPGA	Description
Power, Ground and Clock			
VDD	C3, E3, H3, L4, L6, L8, L11, F11, E11, C11, C8, C6	1, 8, 20, 34, 42, 50, 61, 80, 84, 91, 102, 110	The TMC2330A operates from a single +5V supply. All power and ground pins must be connected.
GND	D3, E2, F2, G3, K3, L3, L7, K11, J11, G11, E12, D11, C10, C9, C7, C5, C4	4, 10, 13, 16, 28, 31, 46, 64, 68, 76, 82, 88, 94, 98, 106, 114, 118	Ground
CLK	F3	12	The TMC2330A operates from a single clock. All enabled registers are strobed on the rising edge of CLK, which is the reference for all timing specifications.

Pin Descriptions (continued)

Pin Name	Pin Number MQFP	Pin Number PPGA	Description
Inputs/Outputs			
$XRIN_{15-0}$	F12, F13, G13, G12, H13, H12, H11, J13, J12, K13, K12, L13, L12, M13, M12, N13	79, 78, 77, 75, 74, 73, 72, 71, 70, 69, 67, 66, 65, 63, 62, 60	$XRIN_{15-0}$ is the registered Cartesian X-coordinate or Polar Magnitude (Radius) 16-bit input data port. $XRIN_{15}$ is the MSB.
$YPIN_{31-0}$	L10, N12, N11, M10, L9, N10, M9, N9, M8, N8, N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, N2, M2, N1, L2, M1, L1, K2, J3, K1, J2, J1	58, 57, 56, 55, 54, 53, 52, 51, 49, 48, 47, 45, 44, 43, 41, 40, 39, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26, 25, 24, 23, 22, 21	$YPIN_{31-0}$ is the registered Cartesian Y-coordinate or Polar Phase angle 32-bit input data port. The input phase accumulators are fed through this port in conjunction with the input enable select $ENYP_{1,0}$. When RTP is HIGH (Rectangular-To-Polar), the input accumulators are normally not used. The 16 MSBs of YPIN are the input port, and the lower 16 bits become "don't cares" if ACC = 00. $YPIN_{31}$ is the MSB.
$RXOUT_{15-0}$	D13, D12, C13, B13, C12, A13, B12, A12, B11, A11, B10, A10, B9, A9, B8, A8	83, 85, 86, 87, 89, 90, 92, 93, 95, 96, 97, 99, 100, 101, 103, 104	$RXOUT_{15-0}$ is the registered Polar Magnitude (Radius) or X-coordinate 16-bit output data port. This output is forced into the high-impedance state when $\overline{OERX}$=HIGH. $RXOUT_{15}$ is the MSB.
$PYOUT_{15-0}$	A7, A6, B6, A5, B5, A4, B4, A3, A2, B3, A1, B2, B1, C2, C1, D2	107, 108, 109, 111, 112, 113, 115, 116, 117, 119, 120, 2, 3, 5, 6, 7	$PYOUT_{15-0}$ is the registered Polar Phase angle or Cartesian Y-coordinate 16-bit output data port. This output is forced to the high-impedance state when $\overline{OEPY}$=HIGH. $PYOUT_{15}$ is the MSB.
Controls			
ENXR	M11	59	The value presented to the input port XRIN is latched into the input registers on the current clock when ENXR is HIGH. When ENXR is LOW, the value stored in the register remains unchanged.
$ENYP_{1,0}$	G1, G2	17, 15	The value presented to the YPIN input port is latched into the phase accumulator input registers on the current clock, as determined by the control inputs $ENYP_{1,0}$, as shown below: **Register Operation** $ENYP_{1,0}$ M C 00 hold hold 01 load hold 10 hold load 11 clear load where C is the Carrier register and M is the Modulation register, and 0=LOW, 1=HIGH. See the Functional Block Diagram.
RTP	E1	11	This registered input selects the current transformation mode of the device. When RTP is HIGH, the TMC2330A executes a Rectangular-To-Polar conversion. When RTP is LOW, a Polar-To-Rectangular conversion will be performed. The input and output ports are then configured to handle data in the appropriate coordinate system. This is a static input. See the Timing Diagram.

Pin Descriptions (continued)

Pin Name	Pin Number		Description
	MQFP	PPGA	
$ACC_{1,0}$	H2, H1	19, 18	In applications utilizing the TMC2330A to perform waveform synthesis and modulation in the Polar-To-Rectangular mode (RTP=LOW), the user determines the internal phase Accumulator structure implemented on the next clock by setting the accumulator control word $ACC_{1,0}$, as shown below: **$ACC_{1,0}$ Configuration** 00 No accumulation performed (normal operation) 01 PM accumulator path enabled 10 FM accumulator path enabled 11 (Nonsensical) logical OR of PM and FM where 0 = LOW, 1 = HIGH. See the Functional Block Diagram. The accumulator will roll over correctly when full-scale is exceeded, allowing the user to perform continuous phase accumulation through 2π radians or 360 degrees. Note that the accumulators will also function when RTP=HIGH (Rectangular-To-Polar), which is useful when performing backward mapping from Cartesian to polar coordinates. However, most applications will require that $ACC_{1,0}$ be set to 00 to avoid accumulating the Cartesian Y input data.
TCXY	F1	14	The format select control sets the numeric format of the Rectangular data, whether input (RTP=HIGH) or output (RTP=LOW). This control indicates two's complement format when TCXY=HIGH and sign-and-magnitude when LOW. This is a static input. See the Timing Diagram.
OVF	B7	105	When RTP=LOW (Polar-To-Rectangular), the Overflow Flag will go HIGH on the clock that the magnitude of either of the current Cartesian coordinate outputs exceeds the maximum range. It will return LOW on the clock that the Cartesian out-put value(s) return to full-scale or less. See the Applications Discussion section. Overflow is not possible in Rectangular-To-Polar mode (RTP = HIGH).
$\overline{OERX}$, $\overline{OEPY}$	E13, D1	81, 9	Data in the output registers are available at the outputs of the device when the respective asynchronous Output Enables are LOW. When $\overline{OERX}$ or $\overline{OEPY}$ is HIGH, the respective output port(s) is in the high impedance state.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		-0.5		7.0	V
Input Voltage		-0.5		V_{DD} + 0.5	V
Output Applied Voltage[2]		-0.5		V_{DD} + 0.5	V
Externally Forced Current[3,4]		-3.0		6.0	V
Short-Circuit Duration	Single output in HIGH state to ground			1	sec
Operating Temperature		-20		110	°C
Ambient Temperature		-20		110	°C
Storage Temperature		-65		150	°C
Junction Temperature			140		°C
Lead Soldering	10 seconds			300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2330A			20	MHz
		TMC2330A-1			40	MHz
		TMC2330A-2			50	MHz
t_{PWH}	Clock Pulse Width, HIGH		7			ns
t_{PWL}	Clock Pulse Width, LOW		6			ns
t_S	Input Data Setup Time		6			ns
t_H	Input Data Hold Time		1			ns
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Nom	Max	Units
I_{DD}	Power Supply Current	V_{DD} = Max, C_{LOAD} = 25pF, f_{CLK} = Max				
		TMC2330A			140	mA
		TMC2330A-1			240	mA
		TMC2330A-2			290	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OERX}$, $\overline{OEPY}$ = HIGH, f_{CLK} = Max				
		TMC2330A			95	mA
		TMC2330A-1			175	mA
		TMC2330A-2			215	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	S_{15-0}, I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	S_{15-0}, I_{OL} = Max			0.4	V

Switching Characteristics

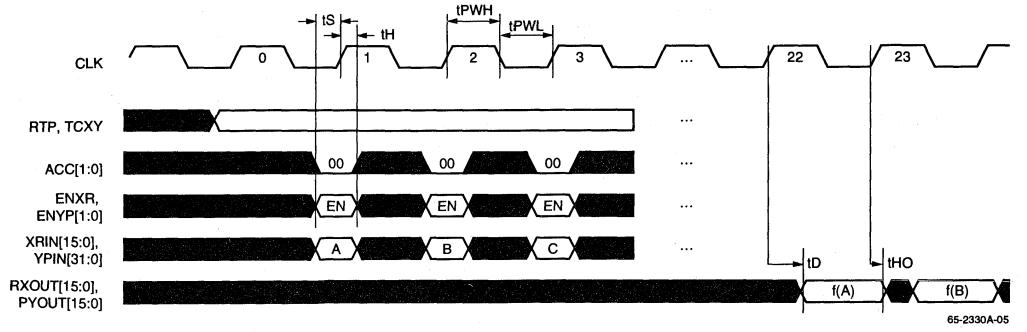
Parameter		Conditions[1]	Min	Nom	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			16	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	3			ns
t_{ENA}	Three-State Output Enable Delay	C_{LOAD} = 0 pF			13	ns
t_{DIS}	Three-State Output Disable Delay	C_{LOAD} = 0 pF			13	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS}.

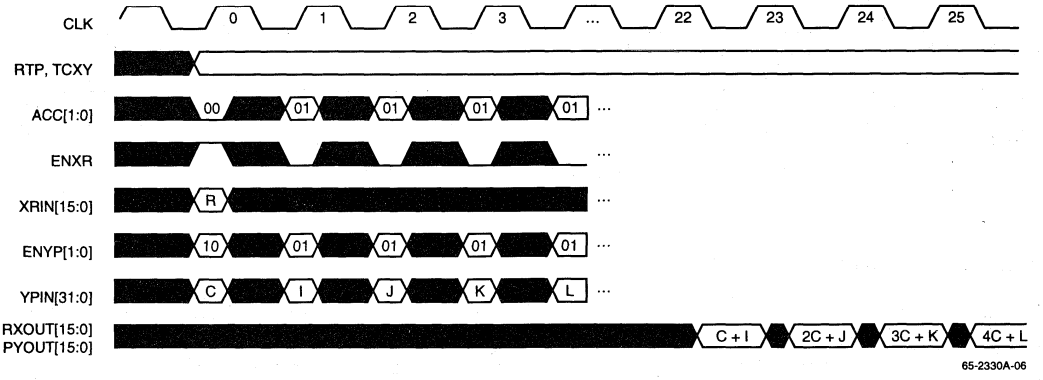
Timing Diagrams

No Accumulation



Note: $\overline{OERX}$ = $\overline{OEPY}$ = LOW

Phase Modulation



Notes:
1. $\overline{OERX}$ = $\overline{OEPY}$ = LOW
2. Carrier C and amplitude R loaded on CLK0.
3. Modulation Values I, J, K, L... Loaded on CLK1, CLK2, etc.
4. Output corresponding to modulation loaded at CLKi emerged tDO after CLKi + 21.
5. To modulate amplitude, vary XRIN with ENXR = 1.

Applications Discussion

Numeric Overflow

Because the TMC2330A accommodates 16-bit unsigned radii and 16-bit signed Cartesian coordinates, Polar-To-Rectangular conversions can overflow for incoming radii greater than 32767= 7FFFh and will overflow for all incoming radii greater than 46341=B505h. (In signed magnitude mode, a radius of 46340 = B504h will also overflow at all angles.) The regions of overflow and of correct conversion are illustrated in Figure 1.

In signed magnitude mode, overflows are circularly symmetrical—if a given radius overflows at an angle P, it will also overflow at the angles π-P, π+P, and -P. This is because -X will overflow if and only if X overflows, and -Y will overflow if and only if Y overflows.

In two's complement mode, the number system's asymmetry complicates the overflow conditions slightly. An input vector with an X component of -32768=8000h will not overflow, whereas one with an X component of +32768 will. Table 3 summarizes several simple cases of overflow and near-overflow.

Table 3a. X-Dimensional Marginal Overflows

TC	YPIN	OV	RXOUT	CORRECT X
0	0000 = 0	1	0000 = +0	+32768
0	8000 = π	1	8000 = -0	-32768
1	0000 = 0	1	8000 = -32768	+32768
1	8000 = π	0	8000 = -32768	-32768

In all cases, RTP=0 (Polar-To-Rectangular mode) and XRIN=8000 (incoming radius=32768).

Table 3b. Maximal Overflow (Radius In=65535)

TC	YPIN	OV	RXOUT	CORRECT X
0	0000 = 0	1	7FFF = +32767	+65535
0	8000 = π	1	FFFF = -32767	-65535
1	0000 = 0	1	FFFF = -1	+65535
1	8000 = π	1	0001 = +1	-65535

In all cases, RTP=0 (Polar-To-Rectangular mode) and XRIN=7FFF (incoming radius=65535, which will always overflow).

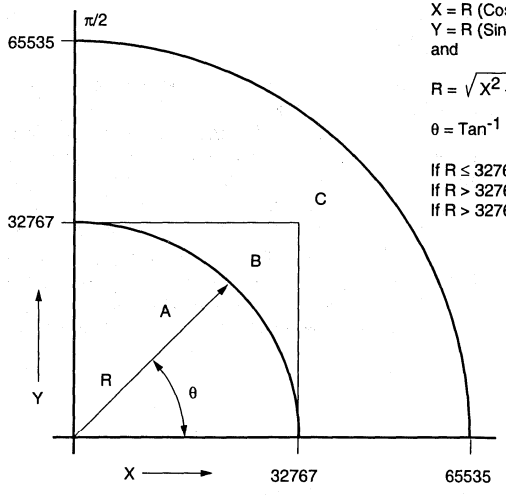
Numeric Underflow

In RTP=1 (Rectangular-To-Polar) mode, if XRIN=YPIN=0, the angle is undefined. Under these conditions, the TMC2330A will output the expected radius of 0 (RXOUT= 0000) and an angle of 1.744 radians (PYOUT=4707). This angle is an artifact of the CORDIC algorithm and is not flagged as an error, since the angle of any 0 length vector is arbitrary.

Performing Scan Conversion with the TMC2330A

Medical Imaging Systems such as Ultrasound, MRI, and PET, and phased array Radar and Sonar systems generate radial-format coordinates (range or distance, and bearing) which must be converted into raster-scan format for further processing and display. Utilizing the TMC2302 Image Resampling Sequencer, a minimum chipcount Scan Converter can be implemented which utilizes the trigonometric translation performed by the TMC2330A to backwards-map from a Cartesian coordinate set into the Polar source image buffer address space.

As shown in Figure 2, the TMC2330A transforms the Cartesian source image addresses from the TMC2302 directly to vector distance and angle coordinates, while the TMC2302 writes the resulting resampled pixel values into the target memory in raster fashion. Note that the ability to perform this spatial transformation in either direction gives the user the freedom to process images in either coordinate space, with little restriction. Image manipulation such as zooms or tilts can easily be included in the transformation by programming the desired image manipulation into the TMC2302's transformation parameter registers.



$X = R (\cos \theta)$
$Y = R (\sin \theta)$
and

$R = \sqrt{X^2 + Y^2}$

$\theta = \text{Tan}^{-1} (Y/X)$

If $R \leq 32767$, overflow will not occur (Region A).
If $R > 32767$, overflow will not occur (Region B) if $|X| \leq 32767$ and $|Y| \leq 32767$.
If $R > 32767$, overflow will occur (Region C) if $|X| \geq 32768$ or $|Y| \geq 32768$.

65-2330A-07

Figure 1. First Quadrant Coordinate Relationships

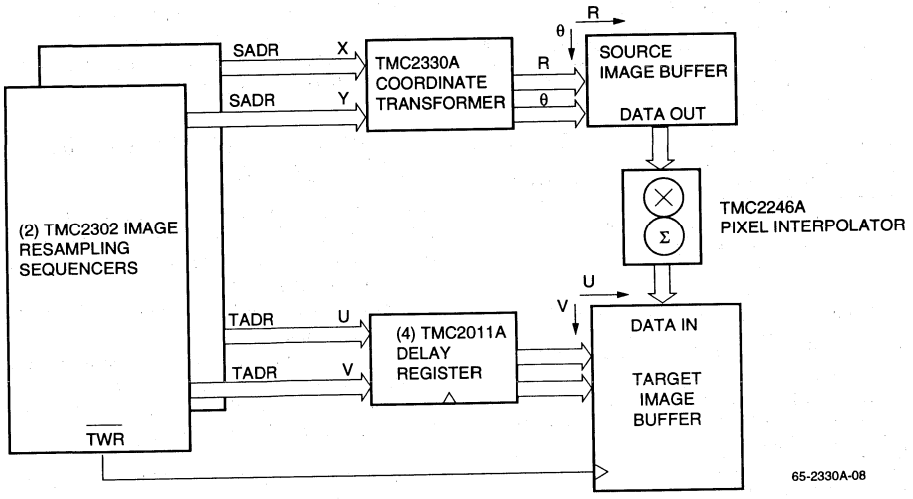


Figure 2. Block Diagram of Scan Converter Circuit Utilizing TMC2330A and TMC2302 Image Resampling Sequencer

Arithmetic Error for Two's Complement Rectangular to Polar Conversion

A random set of 5000 input vector coordinate pairs (X,Y), uniformly spread over a circle of radius 32767 was converted to polar coordinates.

Radius Error Range	–0.609 to 0.746 LSB
Mean Radius Error	0.019 LSB
Mean Absolute Radius Error	0.252 LSB
Phase Error Range	–1.373 to 1.469 LSB
Mean Phase Error	0.058 LSB
Mean Absolute Phase Error	0.428 LSB

Statistical Evaluation of Double Conversion

In this empirical test, 10,000 random Cartesian vectors were converted to and from polar format by the TMC2330A. The resulting Cartesian pairs were then compared against the original ones. The un-restricted database represents uniform sampling over a square bounded by -32769<x<32768 and -32769<y<32768.

The results of the 10,000-vector study were as follows:

Mean Error (X)	+0.0052 LSB
Mean Error (Y)	0.0031 LSB
Mean Absolute Error (X)	0.662 LSB
Mean Absolute Error (Y)	0.664 LSB
Root Mean Square Error (X)	1.025 LSB
Root Mean Square Error (Y)	1.020 LSB
Max Error (X)	+4/ -5 LSB
Max Error (Y)	+5 -4 LSB

Since this is a double conversion (rectangular to polar and back) which includes a wide variety of "good case" and "bad case" vectors, the chip should perform even better in many real systems. Repeating the experiment and restricting the original data set to an annulus defined by 8196<R<32768 reduced the mean square error to 0.89 LSB and the peak error to ±4 LSB (x or y). These latter results are more germane to synthesizer, demodulator, and other applications in which the amplitude can be restricted to lie between quarter and full scale. The largest errors tend to occur in the angle component of small radius cartesian-to-polar conversion.

Equivalent Circuits

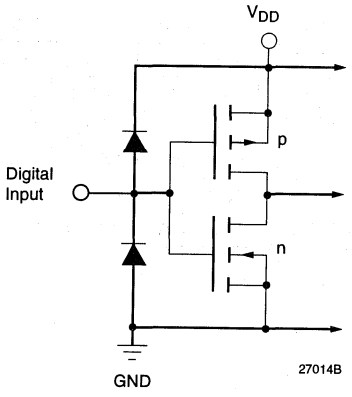


Figure 3. Equivalent Input Circuit

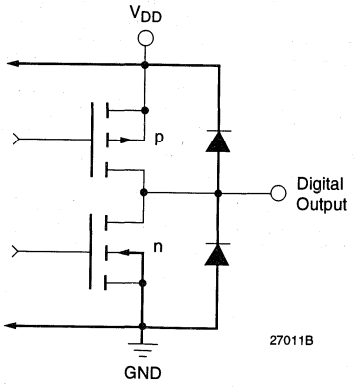


Figure 4. Equivalent Output Circuit

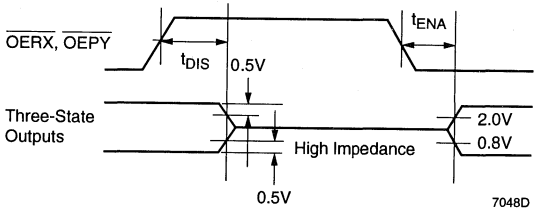


Figure 5. Transition Levels for Three-State Measurements

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2330AH5C	0° to 70°C	20 MHz	Commercial	120-Pin Plastic Pin Grid Array	2330AH5C
TMC2330AH5C1	0° to 70°C	40 MHz	Commercial	120-Pin Plastic Pin Grid Array	2330AH5C1
TMC2330AH5C2	0° to 70°C	50 MHz	Commercial	120-Pin Plastic Pin Grid Array	2330AH5C2
TMC2330AKEC	0° to 70°C	20 MHz	Commercial	120-Pin Metric Quad FlatPack	2330AKEC
TMC2330AKEC1	0° to 70°C	40 MHz	Commercial	120-Pin Metric Quad FlatPack	2330AKEC1
TMC2330AKEC2	0° to 70°C	50 MHz	Commercial	120-Pin Metric Quad FlatPack	2330AKEC2

TMC2340A

Digital Synthesizer

Dual 16 Bit, 50 Msps

Features

- User-configurable phase accumulator for waveform synthesis, frequency modulation or phase modulation
- Amplitude input for amplitude modulation and gain adjustment
- Guaranteed 50 Msps pipelined data throughput rate
- 15-bit magnitude, 32-bit phase data input precision
- 16-bit offset binary or 15-bit unsigned magnitude output data format
- Input register clock enables simplify interfacing
- Low power consumption CMOS process
- Single +5V power supply
- Available in a 120-pin plastic pin grid array package (PPGA) and 120-pin metric quad flat pack (MQFP)

Applications

- Digital waveform synthesis, including quadrature functions
- Digital modulation and demodulation

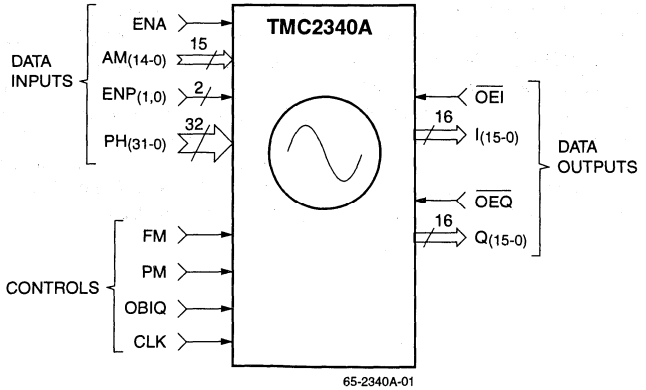
Description

The TMC2340A performs waveform synthesis, modulation, and demodulation. When presented with a TTL clock signal and user-selected 15-bit amplitude and 32-bit phase increment values, the TMC2340A automatically generates quadrature matched pairs of 16-bit sine and cosine waves in DAC-compatible 16-bit offset binary format. If desired, these waveforms are easily phase or frequency-modulated on-chip, and the amplitude input facilitates gain adjustment or amplitude modulation. Digital output frequencies are restricted only by the Nyquist limit of clock rate/2, with frequency resolution of 0.012 Hz at the guaranteed maximum 50 MHz clock rate.

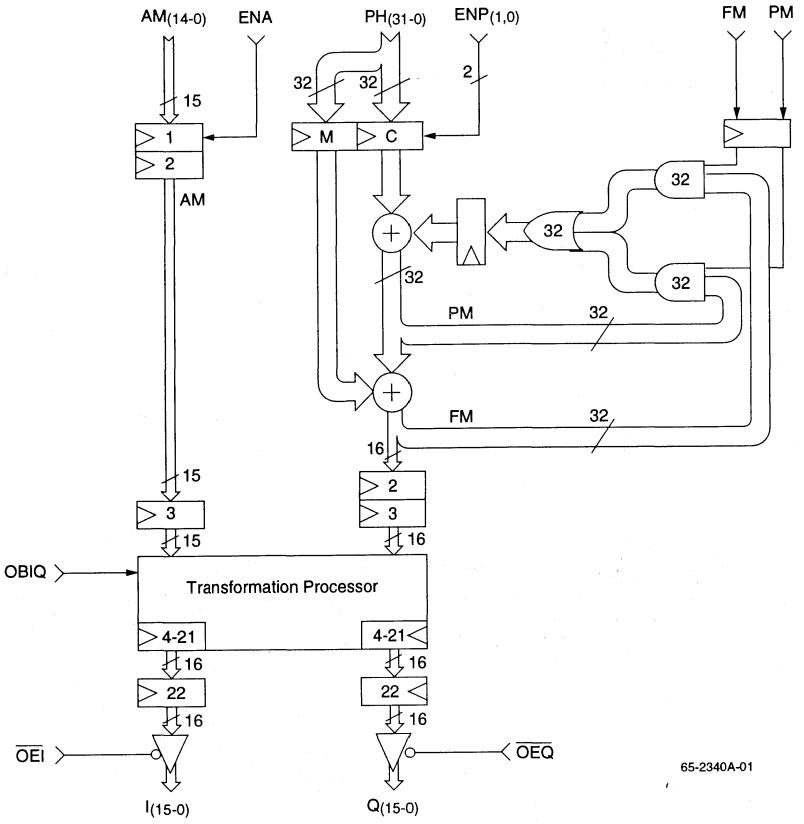
A new data word pair is available at the output every clock cycle. All input and output data ports are registered, with a user-configurable phase accumulator structure and input register clock enables to simplify interfacing. The phase data range over a full 2π radians. All signals are TTL compatible.

Fabricated in a submicron CMOS process, the TMC2340A operates at the 50 MHz maximum clock rate over the full commercial temperature (0 to 70°C) and supply (4.75 to 5.25V) voltage ranges, and is available in low-cost 120 pin plastic pin grid array (PPGA) and a 120-lead metric quad flat pack (MQFP) package.

Logic Symbol



Block Diagram



Functional Description

General Information

The TMC2340A converts Polar (Phase and Magnitude) data into Rectangular (Cartesian) format. The first transformed result is available at the outputs 22 clock cycles after startup, with new output data available every clock cycle. All input and output data ports are registered, with input clock enables to simplify system bus connections.

The input ports accept 15-bit amplitude and 32-bit phase data, and the output ports produce 16-bit Rectangular data words in either 16-bit offset binary or 15-bit unsigned magnitude format. The 32-bit phase accumulator handles high-accuracy (0.012Hz at the maximum clock rate) phase increment values with minimal accumulation error. The flexible input phase accumulator structure supports frequency or phase modulation, as determined by the input register clock enable $ENYP_{1,0}$ and accumulator controls FM and PM. The 16 MSBs (Most Significant Bits) of phase data are used in the transformation itself.

Table 1. Data Input/Output Formats – Integer Format

Port	OBIQ	BIT# 31	30	29	. . .	16	15	14	. . .	0	Format
AM	X							2^{14}	. . .	2^{0}.	U
PH	X	$\pm2^{0}$	2^{-1}	2^{-2}		2^{-15}	2^{-16}	2^{-17}	. . .	2^{-31}	(xπ) T/U
I	0							2^{14}	. . .	2^{0}.	U
I	1						2^{15}	2^{14}	. . .	2^{0}.	B
Q	0							2^{14}	. . .	2^{0}.	U
Q	1						2^{15}	2^{14}	. . .	2^{0}.	B

Notes:

1. $\pm2^{0}$ denotes two's complement sign or highest magnitude bit — since phase angles are modulo 2π and phase accumulator is modulo 2^{32} this bit may be regarded as ±π.
2. All phase angles are in terms of π radians, hence notation "xπ."
3. A sign-and-magnitude "Q" output is obtained by appending the input bit PH_{31} as a sign bit to the corresponding (i.e., delayed 22 cycles) $Q_{14\text{-}0}$.
4. A sign-and-magnitude "I" output is obtained by appending the exclusive OR of PH_{31} and PH_{30} as a sign bit to the corresponding $I_{14\text{-}0}$.
5. When OBIQ=0, outputs I_{15} and Q_{15} become "do not connects" and will stay at logic HIGH. (They may be wired to V_{DD}, left open, or connected to any logic input without damage to the part or excessive power consumption.)
6. Formats:
   T/U = Two's Complement/Unsigned Magnitude 32 Bits
   U = Unsigned Magnitude 15 Bits
   B = Offset Binary 16 Bits

AM, I, Q			PH	
HEX	U	B	T	U
FFFF		32767	$-\pi \cdot 2^{-15}$	$\pi(2-2^{-15})$
--	--	--		
8001		1	$-\pi(1-2^{-15})$	$\pi(1+2^{-15})$
8000		0	$-\pi$	π
7FFF	32767	-1	$\pi(1-2^{-15})$	$\pi(1-2^{-15})$
--	--	--		
0001	1	-32767	$\pi \cdot 2^{-15}$	$\pi \cdot 2^{-15}$
0000	0	-32768	0	0

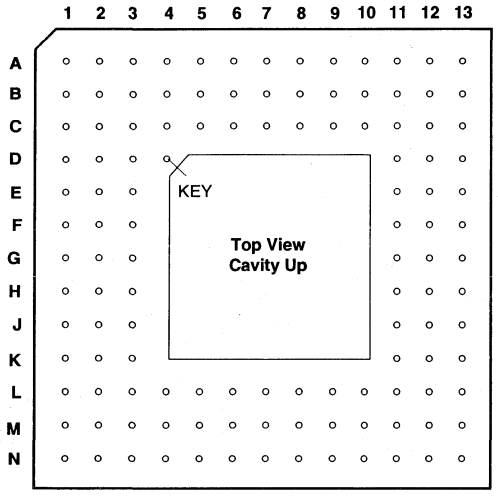
"Hex" column contains the 16 MSBs of the 32-bit phase input (16 LSBs are 0), the 15 bits of the amplitude input or the 16 bits of the offset binary output

Static Control Input

OBIQ determines the numeric format of the output data: offset binary if HIGH and unsigned magnitude if LOW. This control acts with 2-cycle latency on the chip's 22-cycle data path and is normally hardwired to a system-specific state.

Pin Assignments

120-Pin Plastic Pin Grid Array (PPGA)

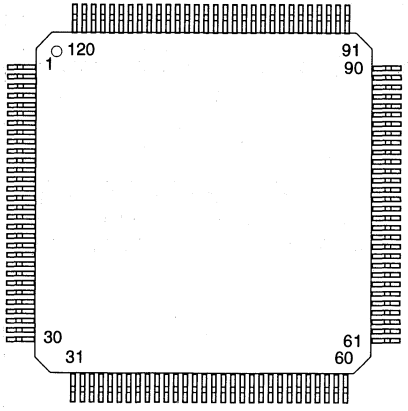


65-2340A-03

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	Q_5	C5	GND	G11	GND	L10	PH_{31}
A2	Q_7	C6	V_{DD}	G12	AM_{12}	L11	V_{DD}
A3	Q8	C7	GND	G13	AM_{13}	L12	AM_3
A4	Q_{10}	C8	V_{DD}	H1	PM	L13	AM_4
A5	Q_{12}	C9	GND	H2	FM	M1	PH_6
A6	Q_{14}	C10	GND	H3	V_{DD}	M2	PH_9
A7	Q_{15}	C11	V_{DD}	H11	AM_9	M3	PH_{11}
A8	I_0	C12	I_{11}	H12	AM_{10}	M4	PH_{13}
A9	I_2	C13	I_{13}	H13	AM_{11}	M5	PH_{16}
A10	I_4	D1	$\overline{OEQ}$	J1	PH_0	M6	PH_{18}
A11	I_6	D2	Q_0	J2	PH_1	M7	PH_{20}
A12	I_8	D3	GND	J3	PH_3	M8	PH_{23}
A13	I_{10}	D11	GND	J11	GND	M9	PH_{25}
B1	Q_3	D12	I_{14}	J12	AM_7	M10	PH_{28}
B2	Q_4	D13	I_{15}	J13	AM_8	M11	ENA
B3	Q_6	E1	GND	K1	PH_2	M12	AM_1
B4	Q_9	E2	GND	K2	PH_4	M13	AM_2
B5	Q_{11}	E3	V_{DD}	K3	GND	N1	PH_8
B6	Q_{13}	E11	V_{DD}	K11	GND	N2	PH_{10}
B7	GND	E12	GND	K12	AM_5	N3	PH_{12}
B8	I_1	E13	$\overline{OEI}$	K13	AM_6	N4	PH_{15}
B9	I_3	F1	OBIQ	L1	PH_5	N5	PH_{17}
B10	I_5	F2	GND	L2	PH_7	N6	PH_{19}
B11	I_7	F3	CLK	L3	GND	N7	PH_{21}
B12	I_9	F11	V_{DD}	L4	V_{DD}	N8	PH_{22}
B13	I_{12}	F12	GND	L5	PH_{14}	N9	PH_{24}
C1	Q_1	F13	AM_{14}	L6	V_{DD}	N10	PH_{26}
C2	Q_2	G1	ENP_1	L7	GND	N11	PH_{29}
C3	V_{DD}	G2	ENP_0	L8	V_{DD}	N12	PH_{30}
C4	GND	G3	GND	L9	PH_{27}	N13	AM_0

Pin Assignments (continued)

120-Lead Metric Quad Flat Pack (MQFP)



65-2340A-04

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	31	GND	61	V_{DD}	91	V_{DD}
2	Q_4	32	PH_9	62	AM_1	92	I_9
3	Q_3	33	PH_{10}	63	AM_2	93	I_8
4	GND	34	V_{DD}	64	GND	94	GND
5	Q_2	35	PH_{11}	65	AM_3	95	I_7
6	Q_1	36	PH_{12}	66	AM_4	96	I_6
7	Q_0	37	PH_{13}	67	AM_5	97	I_5
8	V_{DD}	38	PH_{14}	68	GND	98	GND
9	$\overline{OEQ}$	39	PH_{15}	69	AM_6	99	I_4
10	GND	40	PH_{16}	70	AM_7	100	I_3
11	GND	41	PH_{17}	71	AM_8	101	I_2
12	CLK	42	V_{DD}	72	AM_9	102	V_{DD}
13	GND	43	PH_{18}	73	AM_{10}	103	I_1
14	OBIQ	44	PH_{19}	74	AM_{11}	104	I_0
15	ENP_0	45	PH_{20}	75	AM_{12}	105	GND
16	GND	46	GND	76	GND	106	GND
17	ENP_1	47	PH_{21}	77	AM_{13}	107	Q_{15}
18	PM	48	PH_{22}	78	AM_{14}	108	Q_{14}
19	FM	49	PH_{23}	79	GND	109	Q_{13}
20	V_{DD}	50	V_{DD}	80	V_{DD}	110	V_{DD}
21	PH_0	51	PH_{24}	81	$\overline{OEI}$	111	Q_{12}
22	PH_1	52	PH_{25}	82	GND	112	Q_{11}
23	PH_2	53	PH_{26}	83	I_{15}	113	Q_{10}
24	PH_3	54	PH_{27}	84	V_{DD}	114	GND
25	PH_4	55	PH_{28}	85	I_{14}	115	Q_9
26	PH_5	56	PH_{29}	86	I_{13}	116	Q_8
27	PH_6	57	PH_{30}	87	I_{12}	117	Q_7
28	GND	58	PH_{31}	88	GND	118	GND
29	PH_7	59	ENR	89	I_{11}	119	Q_6
30	PH_8	60	AM_0	90	I_{10}	120	Q_5

Pin Descriptions

Pin Name	Pin Number		Pin Function Description
	PPGA	MQFP	
Power, Ground and Clock			
V_{DD}	C3, E3, H3, L4, L6, L8, L11, F11, E11, C11, C8, C6	1, 8, 20, 34, 42, 50, 61, 80, 84, 91, 102, 110	The TMC2340A operates from a single +5V supply. All power and ground pins must be connected.
GND	D3, E2, E1, F2, G3, K3, L3, L7, K11, J11, G11, F12, E12, D11, C10, C9, B7, C7, C5, C4	4, 10, 11, 13, 16, 28, 31, 46, 64, 68, 76, 79, 82, 88, 94, 98, 105, 106, 114, 118	Ground
CLK	F3	12	The TMC2340A operates from a single clock. All enabled registers are strobed on the rising edge of CLK, which is the reference for all timing specifications.

Pin Descriptions (continued)

Pin Name	Pin Number PPGA	Pin Number MQFP	Pin Function Description
Inputs/Outputs			
AM_{14-0}	F13, G13, G12, H13, H12, H11, J13, J12, K13, K12, L13, L12, M13, M12, N13	78, 77, 75-69, 67-65, 63, 62, 60	AM_{14-0} is the registered peak amplitude 15-bit input data port. AM_{14} is the MSB.
PH_{31-0}	L10, N12, N11, M10, L9, N10, M9, N9, M8, N8, N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, N2, M2, N1, L2, M1, L1, K2, J3, K1, J2, J1	58-51, 49-47, 45-43, 41-35, 33, 32, 30, 29, 27-21	PH_{31-0} is the registered Phase angle increment 32-bit input data port. The input phase accumulators are fed through this port in conjunction with the input enable select $ENP_{1,0}$. PH_{31} is the MSB.
I_{15-0}	D13, D12, C13, B13, C12, A13, B12, A12, B11, A11, B10, A10, B9, A9, B8, A8	83, 85, 86, 87, 89, 90, 92, 93, 95-97, 99-101, 103, 104	I_{15-0} is the registered X-coordinate 16-bit output data port. This output is forced into the high-impedance state when $\overline{OEI}$=HIGH. I_0 is the LSB. I_{15} will be "stuck at" logic HIGH if OBIQ=O.
Q_{15-0}	A7, A6, B6, A5, B5, A4, B4, A3, A2, B3, A1, B2, B1, C2, C1, D2	107-109, 111-113, 115-117, 119, 120, 122, 123, 125-127	Q_{15-0} is the registered Cartesian Y-coordinate 16-bit output data port. This output is forced to the high- impedance state when $\overline{OEQ}$=HIGH. Q_0 is the LSB. Q_{15} will remain at logic HIGH if OBIQ=0.
Controls			
ENA	M11	59	Data presented to the input port AM are latched into the input registers on the current clock when ENA is HIGH. When ENA is LOW, the data stored in the register remains unchanged.
$ENP_{1,0}$	G1, G2	17, 15	The value presented to the PH input port is latched into the phase accumulator input registers on the current clock, as determined by the control inputs $ENP_{1,0}$, as shown below: $ENP_{1,0}$ / Instruction 00 — No registers enabled, current data held 01 — M register input enabled, C data held 10 — C register input enabled, M data held 11 — M register set to 0, C register input enabled where C is the Carrier register and M is the Modulation register, and 0=LOW, 1= HIGH. See the Block Diagram.

Pin Descriptions (continued)

Pin Name	Pin Number PPGA	Pin Number MQFP	Pin Function Description
FM, PM	H2, H1	19, 18	The user determines the internal phase Accumulator structure implemented on the next clock by setting the accumulator control word FM, PM, as shown below: FM, PM: 00 — No accumulation performed; 01 — PM accumulator path enabled; 10 — FM accumulator path enabled; 11 — (Nonsensical) logical OR of PM and FM where 0=LOW, 1=HIGH. See the Block Diagram. The accumulator will roll over correctly when full-scale is exceeded, allowing the user to perform continuous phase accumulation through 2π radians, or 360 degrees.
OBIQ	F1	14	The format select control sets the numeric format of the Rectangular data: offset binary format when HIGH, and unsigned when LOW. This is a static input. See the Timing Diagram.
$\overline{OEI}$, $\overline{OEQ}$	E13, D1	81, 9	Data in the output registers are available at the outputs of the device when the respective asynchronous Output Enables are LOW. When $\overline{OEI}$ or $\overline{OEQ}$ is HIGH, the respective output port is in the high-impedance state.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Max	Units
Power Supply Voltage (V_{CC})	-0.5	7	V
Input Voltage	-0.5 to (V_{DD}+0.5)V		
Applied Voltage[2] Output	-0.5	V_{DD}+0.5	
Externally Forced Current Output			
Short-circuit Duration Output (single output in HIGH state to ground)		1 second	
Operating Temperature	-20	110	°C
Storage Temperature	-65	150	°C
Junction Temperature		140	°C
Lead Soldering Temperature (10 sec)		300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Condition	Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2340A			20	MHz
		TMC2340A-1			40	MHz
		TMC2340A-2			50	MHz
t_{PWH}	Clock Pulse Width, HIGH		7			ns
t_{PWL}	Clock Pulse Width, LOW		6			ns
t_S	Input Data Setup Time		6			ns
t_H	Input Data Hold Time		1			ns
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

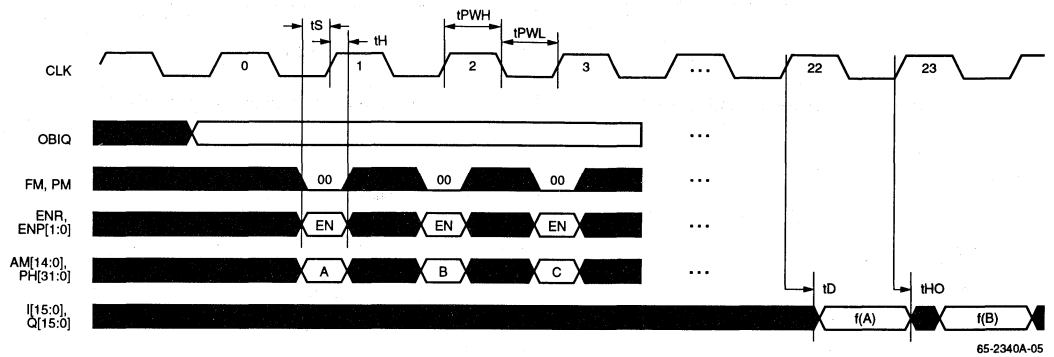
Parameter		Conditions	Min	Nom	Max	Units
I_{DD}	Power Supply Current	V_{DD} = Max, C_{LOAD} = 25pF, f_{CLK} = Max				
		TMC2340A			140	mA
		TMC2340A-1			240	mA
		TMC2340A-2			290	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OEI}$, $\overline{OEQ}$ = HIGH, f_{CLK} = Max				
		TMC2340A			95	mA
		TMC2340A-1			175	mA
		TMC2340A-2			215	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max,CLK = LOW			5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		–20		–80	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max			0.4	V

Switching Characteristics

Parameter		Conditions[1]	Min	Nom	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			16	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	3			ns
t_{ENA}	Three-State Output Enable Delay	C_{LOAD} = 0 pF			13	ns
t_{DIS}	Three-State Output Disable Delay	C_{LOAD} = 0 pF			13	ns

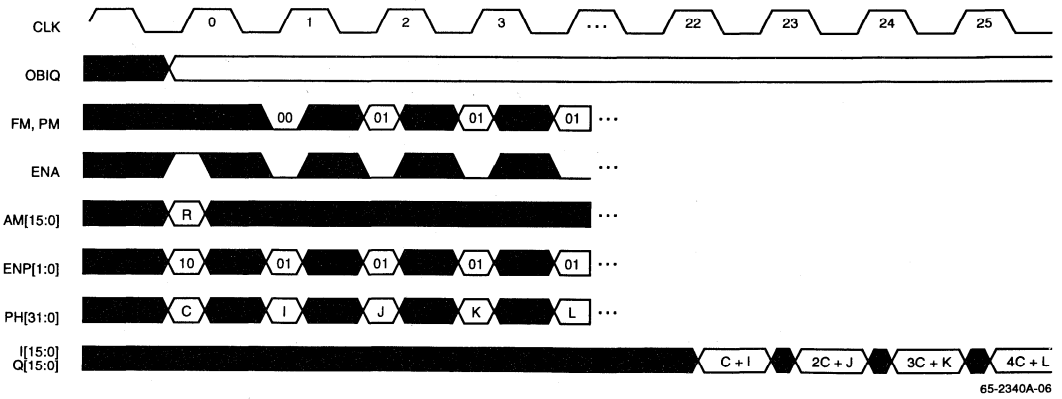
Note:
1. All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS}.

Timing Diagram – No Accumulation



Note: $\overline{OEI}$, $\overline{OEQ}$ = LOW.

Timing Diagram – Phase Modulation



Notes:
1. $\overline{OEI}$, $\overline{OEQ}$ = LOW.
2. Carrier C and peak amplitude A loaded on CLK 0.
3. Modulation values I, J, K, L, ... loaded on CLK 1, CLK 2, etc.
4. Output corresponding to modulation loaded at CLK i emerged t_{DO} after CLK i +21.
5. To modulate amplitude, vary AM with ENA = 1.

Equivalent Circuits and Transition Levels

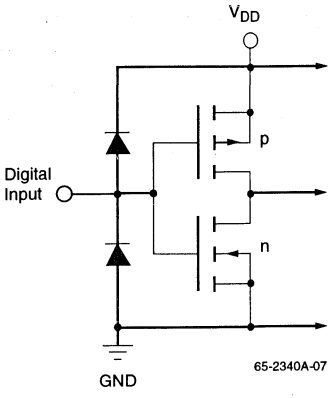


Figure 1. Equivalent Input Circuit

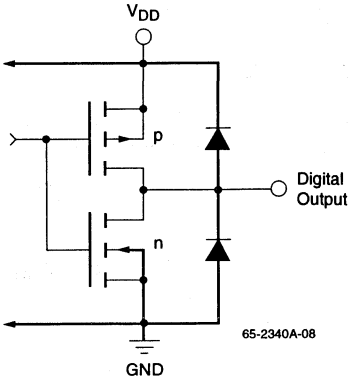


Figure 2. Equivalent Output Circuit

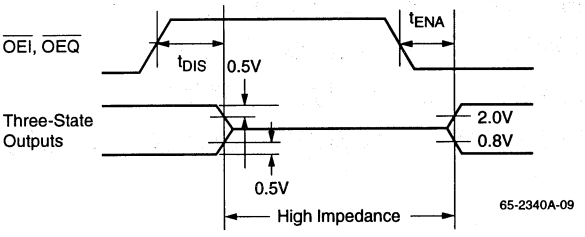


Figure 3. Transition Levels for Three-State Measurements

Digital Waveform Synthesis

Generating Unmodulated Sine and Cosine Waves

The TMC2340 can generate simultaneous quadrature-matched sine and cosine waves with optional amplitude, frequency, or phase modulation. To obtain an unmodulated waveform, the user loads the desired phase step value, computed as:

$$f_C = \frac{2^{32} \times \text{desired\_output\_frequency}}{\text{digital\_clock\_frequency}}$$

into the 32-bit-wide carrier register via the PH input port, and applies the desired sinusoid amplitude (half of the desired peak-to-peak value) to the 15-bit-wide AM input port. As the chip's internal phase accumulator increments linearly in steps of f_C, the chip will output a series of complex number pairs representing the horizontal and vertical projections of a vector rotating about the origin, i.e., cosine and sine waves.

A procedure that will yield continuous unmodulated sinusoids is shown in Table 2.

Table 2. Generating unmodulated sinusoids

FM	PM	ENA	AM	ENP	PH	
0	0	1	a	11	f_C	loads freq & amplitude
0	1	0	x	00	x	starts synthesizer @ phase = f_C
0	1	0	x	00	x	continues @ phase = $2f_C$

Because the chip's internal pipeline is 22 registers deep, the effects of any given set of data inputs or instructions won't be seen for 22 clock cycles. After the (22+n)th rising edge of the system clock, the outputs will be (Figure 4):

$$I(22+n) = a\cos(2\pi n f_C/2^{32}) \text{ and}$$

$$Q(22+n) = a\sin(2\pi n f_C/2^{32}),$$

where a is the (constant) amplitude and f_C is the (constant) carrier phase step or frequency ratio. For example, if we arbitrarily set a=4000h and f_C=2000 0000h, the chip will generate quadrature-matched sines and cosines at 1/8 of the clock frequency and 1/2 of full-scale amplitude. Here, the internal phase accumulation sequence will be:

Phase Accumulator	Phase
2000 0000h	45 degrees
4000 0000h	90
6000 0000h	135
8000 0000h	180
a000 0000h	225
c000 0000h	270
e000 0000h	315
0000 0000h	0
2000 0000h	45
•••	•••

On any given clock cycle, the phase angle into the chip's polar-to-rectangular converter core is that of the phase accumulator:

$$\text{phase}(n) = nf_C$$

[The maximum possible output frequency is just less than half of the clock rate, per the Nyquist limit. For f>8000 0000, one obtains "negative" frequencies, because the phase increment now aliases backward. Thus, a=4000h and f=e000 0000h will generate a cosine wave and a negated sine wave at 1/8 of the clock frequency and 1/2 of full-scale amplitude.]

Amplitude Modulation

By holding amplitude enable pin ENA high, the user can vary the incoming amplitude sample by sample, thereby amplitude-modulating the output signals. The output equations become:

$$I(22+n) = a(n) \times \cos(2\pi n f_C/2^{32}) \text{ and}$$

$$Q(22+n) = a(n) \times \sin(2\pi n f_C/2^{32}),$$

Most amplitude modulation applications employ an external adder to combine a fixed (unsigned magnitude) carrier amplitude with a sample-by-sample two's complement modulation term, such that the chip sees:

$$a(n) = \text{carrier\_amplitude} + \text{amplitude\_modulation}(n)$$

[Since the chip accepts only nonnegative amplitudes, this simple implementation is limited to 100% modulation, wherein the instantaneous incoming amplitude can drop to 0, but not below.]

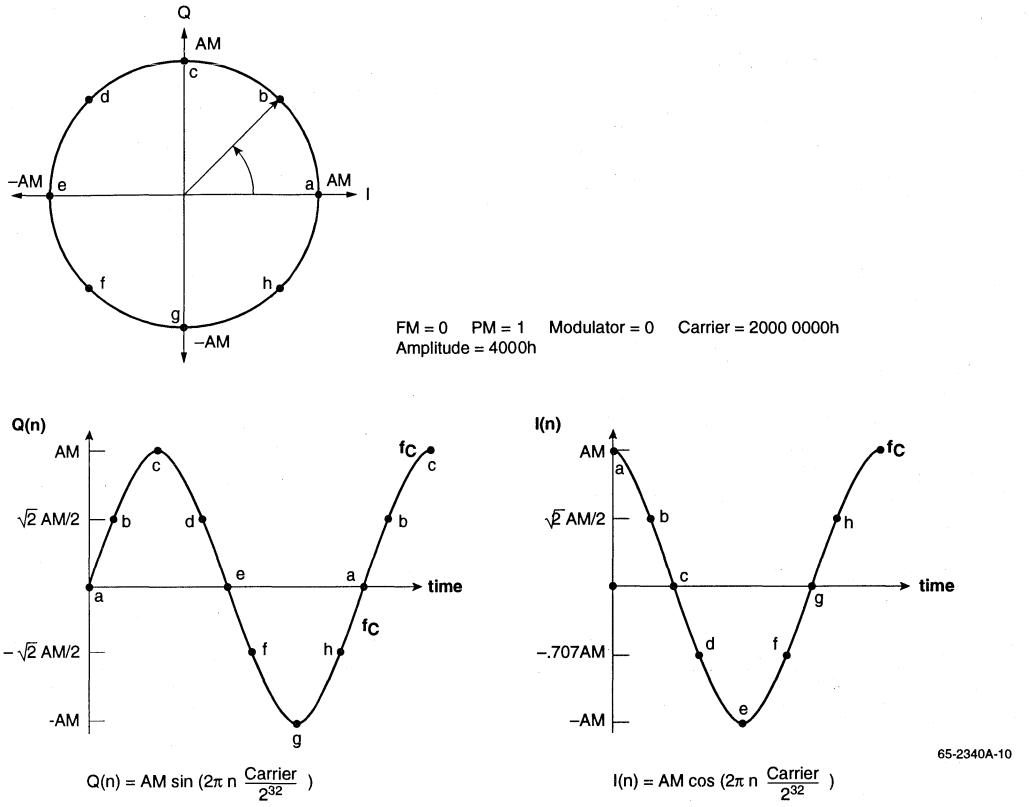


Figure 4. Unmodulated Sinusoid Generation

Again, on any given clock cycle, the phase angle into the chip's polar-to-rectangular converter core is that of the phase accumulator:

$$phase(n) = nf_C$$

Phase Modulation

By setting ENP to 10 instead of 00 (while keeping FM = 0 and PM = 1), the user can load a new modulating phase shift into the PH port on each clock cycle. If we label this modulating term p(n), the output equations become:

$$I(n+22) = a(n) \times \cos(2\pi(p(n)+nf_C)/2^{32}$$

$$Q(n+22) = a(n) \times \sin(2\pi(p(n)+nf_C)/2^{32}$$

Figure 5 depicts the internal subsarrier architecture in this mode. If we again load carrier = 2000 0000h, but now alternately apply phase modulation (p) terms 0 and 1000 000h, the internal phase sequence will be:

Phase Modulation	Phase
2000 0000h	normal unmodulated start
5000 0000h	phase advanced by an additional 1000 0000h
6000 0000h	phase back to normal progression
9000 0000h	phase advanced by an additional 1000 0000h
a000 0000h	phase back to normal progression
d000 0000h	phase advanced by an additional 1000 0000h
e000 0000h	phase back to normal progression

Here, on any given clock cycle, the phase angle into the chip's polar-to-rectangular converter core is that of the phase accumulator, plus the current value of the modulator:

$$phase(n) = nf_C + p(n)$$

Frequency Modulation

By setting ENP = 10, FM = 1 , and PM = 0, the user can load a new frequency modulation sample into the PH port on each clock cycle. In phase modulation, the angular modulation term was outside of the phase accumulator/integration loop. Therefore, each modulation sample affected only a single complex output sample. In frequency modulation, since the angular modulation occurs within the phase accumulator, each modulation sample affects all future outputs. Figure 5 depicts the phase accumulator architecture in this mode.

Consider the following phase advance sequence, using the same 2000 0000h carrier and alternate 0 and 1000 000h modulation, this time in frequency modulation instead of phase modulation mode:

Phase Accumulator	Phase
2000 0000h	unmodulated
5000 0000h	phase advanced by 10000000+20000000
7000 0000h	unmodulated—phase advanced by 20000000
a000 0000h	phase again advanced by 30000000
c000 0000h	advance by 20000000
f000 0000h	advance by 30000000

Here, on any given clock cycle, the phase angle into the chip's polar-to-rectangular converter core is that of the previous cycle, plus carrier + modulator:

$$phase(n+1) = phase(n) + f_C + p(n)$$

and is the same as the present value in phase accumulator. In frequency modulation mode, introducing a single nonzero modulation term will shift the phases of all outputs which follow. In contrast, in phase modulation, introducing a single nonzero modulation term will shift the phase of only one output.

Digital Synthesizer with the TDC1012 D/A Converter

The TDC1012 is an ideal D/A converter for digital synthesis, exhibiting a Spurious-Free Dynamic Range of greater than 70dB. Connection between the TMC2340A and TDC1012 is straightforward, as illustrated in Figure 5.

Either the I or the Q output of the TMC2340 may be connected to the D/A; two converters are used for quadrature synthesis. The trans-former-coupled output circuit shown is recommended for minimum distortion. See the TDC1012 datasheet for details.

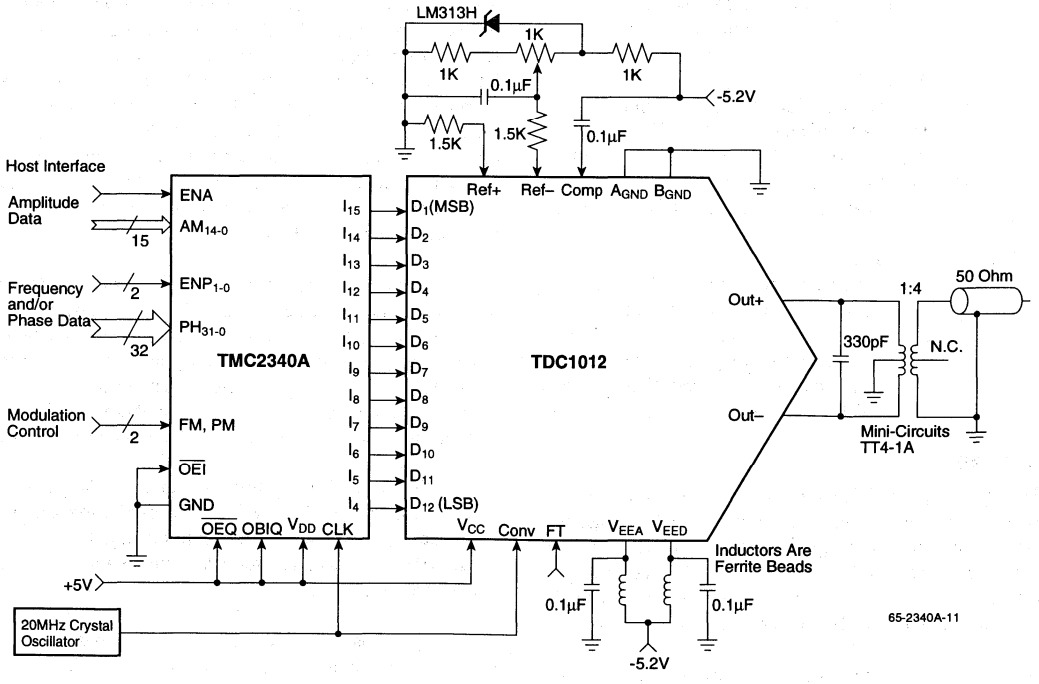


Figure 5. Frequency Synthesizer

Control of the TMC2340A

The TMC2340A needs to be initialized to tell it what frequency and amplitude sinusoid to generate. To initialize amplitude, apply the desired full-scale amplitude to the AM input port of the TMC2340A (AM_{14} through AM_0) and pull ENA HIGH for one clock cycle. This will load the amplitude. If ENA is held HIGH, then the amplitude will follow the inputs on the AM port. If the user assumes an implied binary point before the MSB of the AM port, the input range will be 0 to just under 1, and the outputs will fall between 0 and 2, with binary points after I_{15} and Q_{15}.

To set the frequency, the C register must be loaded with a value which is the phase increment per clock cycle. If the binary point is considered to be just left of the MSB (input range is 0 to almost 1) then the output frequency is the TMC2340A clock frequency multiplied by the number loaded into C. Since C is 32 bits wide, with a 20MHz clock, one LSB represents a frequency increment of 0.005Hz.

To load the C register, set $ENYP_1$=1 and $ENYP_0$=0; the data presented at the PH port will be loaded on the next clock rising edge.

At this point the TMC2340A has been initialized and can be put into one of three modes depending upon the states of FM and PM:

Mode 0 FM = 0, PM = 0
In this mode the chip is in standby. The unchanging output corresponds to AM cos(PM) on the I outputs with PM being the phase increment.

Mode 1 FM=1, PM=0
Frequency Modulation Mode. The chip generates an output signal of peak amplitude AM and frequency determined by accumulating the sum of the phase increment values in the C and M registers (more about the M register in a later section).

Mode 2 FM=0, PM=1
Phase Modulation Mode. The TMC2340A generates a sinusoid of the frequency represen-ted in the C register and the peak amplitude in the AM register. On each clock cycle, the phase of the signal is offset by the value in the M register. Use this mode with ENP=00 for unmodulated sinewave synthesis.

Modulation

The output of the TMC2340A can be phase (Mode 2) or frequency (Mode 1) modulated. An unmodulated sinusoid results if the contents of registers C and M are held constant. Its frequency is set by C (Mode 2) or C+ M (Mode 1). Since the state of the M register is not defined at power up, the M register should be loaded or cleared to begin operation.

If the signal is to be frequency modulated then the modulation signal is loaded into the M register. The format for the frequency is the same as that for the C register. If $ENYP_{1,0}$ = 0, 1 then the data value present at the PH port is automatically loaded on each clock rising edge.

For phase modulation, the phase deviation is loaded into the M register (same manner as for frequency modulation). The units of the phase offset are cycles and full-scale is just under one output cycle per TMC2340A clock cycle. The MSB represents a phase of 180°, and the LSB a phase of about $8x10^{-8}$ degrees (eight one-hundred millionths of a degree) or $\pi/2^{31}$ radians.

To synchronize two TMC2340As, first load them with their respective data in mode 0, then switch them simultaneously to either Mode 1 or Mode 2.

Calculating Frequency, Amplitude, and Phase Input Values for the TMC2340A

This Application Brief discusses equations which simplify the calculation of register values which control the TMC2340A. These values allow the generation of output carrier frequency, frequency or phase modulation, and output amplitude.

The results of the equations are converted to binary register values and should be rounded to the resolution of the applicable register (32 or 15-bits). For negative values of phase or frequency modulation, use these equations for positive values and see Table 1 to convert them to negative values.

The TMC2340A operates by continuously incrementing a register (phase accumulator) that rolls over when it becomes full. For example, if the next increment to the phase accumulator causes it to overflow by 47 LSBs, the phase accumulator retains the value 47. The value present in the carrier register (C) is the amount by which the phase accumulator is incremented each system clock cycle. As the value of the carrier register is increased, the value with which the phase accumulator is incremented each clock cycle is increased, resulting in an increased carrier frequency.

The magnitude of the carrier is determined or modulated by the value loaded In the AM register. Phase modulation is accomplished by adding the value of the phase accumulator to the value of the modulation (M) register. This adds an offset to the phase of the carrier. This does not affect the increment value of the phase accumulator and therefore affects only the phase of the carrier, leaving the frequency constant.

Adding the value of the modulation register to the phase accumulator along with the value of the carrier register on each clock cycle results in a shift in frequency. This is because the phase accumulator is incremented by a different amount each clock cycle.

Frequency or phase modulation is selected with the FM and PM input pins which configure the TMC2340A. The equations presented herein are useful for setting carrier frequency

and phase, output amplitude, and frequency and phase modulation. To modulate the carrier with an external signal, the signal must be digitized and those values loaded into the modulation inputs of the TMC2340A.

The carrier and modulation registers are loaded through the PH_{31-0} inputs. The $ENP_{1,0}$ inputs select the desired register. The amplitude register is loaded through the AM_{14-0} inputs.

CARRIER FREQUENCY:

$$\text{Carrier Register (C) Value} = \frac{\text{Desired Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

AMPLITUDE AND AMPLITUDE MODULATION:

$$\text{AM Register Value} = \frac{\text{Desired Output Amplitude}}{\text{Full-Scale Output Amplitude}} \times (2^{15} - 1)$$

FREQUENCY MODULATION:

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

PHASE-MODULATION:

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Phase in Radians (Degrees)}}{2\pi(360^\circ)} \times 2^{32}$$

EXAMPLE 1: Set carrier frequency to 3.579545 MHz with a system clock of 20MHz.

$$\text{Carrier Register (C) Value} = \frac{\text{Desired Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32} = \frac{3.579545 \times 10^6}{20 \times 10^6} \times 2^{32}$$

C = 0.17897725 X 4,294,967,296 = 768,701,436 = 2DD1 73FCh
= 0010 1101 1101 0001 0111 0011 1111 1011 = PH_{31-0}

EXAMPLE 2: Set output amplitude to be 12.2% of full-scale.

$$\text{AM Register Value} = \frac{\text{Desired Output Amplitude}}{\text{Full-Scale Output Amplitude}} \times (2^{15} - 1) = \frac{12.2}{100.0} \times 32767$$

AM = 3,998 = 0F9Eh = 0001 1111 0011 1100 = AM_{14-0}

EXAMPLE 3: Change carrier frequency by 10kHz with a system clock of 3 MHz.

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

$$M = \frac{10 \times 10^3}{3 \times 10^6} \times 2^{32} = 14,316,558 = 00DA\ 740Eh$$

$$M = 0000\ 0000\ 1101\ 1010\ 0111\ 0100\ 0000\ 1110 = PH_{31-0}$$

EXAMPLE 4: Advance the phase of any carrier frequency by 12°.

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Phase}}{360^\circ} \times 2^{32} = \frac{12}{360} \times 2^{32}$$

M = 0.033333 X 2^{32} = 143,165,577 = 0888 8889h
= 0000 1000 1000 1000 1000 1000 1000 1001 = PH_{31-0}

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2340AH5C	0° to 70°C	20 MHz	Commercial	121-Pin Plastic Pin Grid Array	2340AH5C
TMC2340AH5C1	0° to 70°C	40 MHz	Commercial	121-Pin Plastic Pin Grid Array	2340AH5C1
TMC2340AH5C2	0° to 70°C	50 MHz	Commercial	121-Pin Plastic Pin Grid Array	2340AH5C2
TMC2340AKEC	0° to 70°C	20 MHz	Commercial	120-Pin Metric Quad FlatPack	2340AKEC
TMC2340AKEC1	0° to 70°C	40 MHz	Commercial	120-Pin Metric Quad FlatPack	2340AKEC1
TMC2340AKEC2	0° to 70°C	50 MHz	Commercial	120-Pin Metric Quad FlatPack	2340AKEC2

TMC1103

Triple Video A/D Converter with Clamps

8-Bit, 50Msps

Features

- 8-bit resolution
- 50 Msps conversion rate
- Low power: 100mW per channel @ 20 Msps
- Integral track/hold
- Independent Input Clamps
- Independent clock inputs
- Integral and differential linearity error 0.5 LSB
- Differential phase 0.7 degree
- Differential gain 1.8%
- Single +5V power supply
- Three-state TTL/CMOS-compatible outputs
- Low cost

Applications

- Video digitizing (composite and Y-C)
- VGA and CCD digitizing
- LCD projection panels
- Image scanners
- Personal computer video boards
- Multimedia systems
- Low cost, high speed data conversion

Description

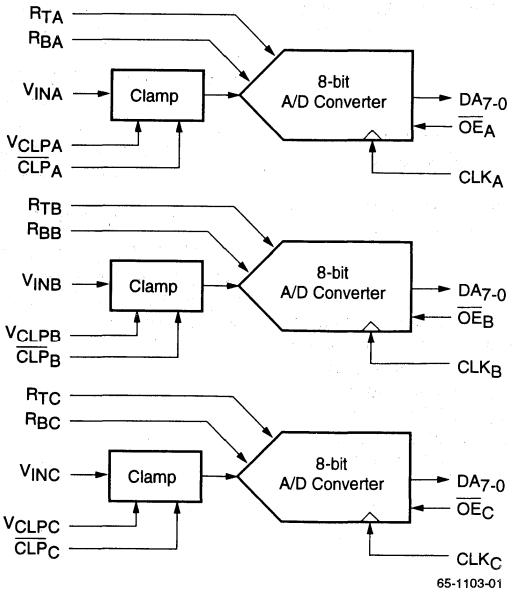
Incorporated into the TMC1103 are three analog-to-digital (A/D) converters, each with an independent clock, reference voltage and input clamp. Analog signals are converted to Triple 8-bit digital words at sample rates up to 50 Msps (Megasamples per second) per channel.

Integral Track/Hold circuits deliver excellent performance on signals with full-scale spectral components up to 12 MHz. Innovative two-step conversion architecture and submicron CMOS technology reduce typical power dissipation to 100 mW per converter.

Power is derived from a single +5 Volt power supply. Outputs are three-state outputs and TTL/CMOS-compatible.

TMC1103 package is a 80-lead Metric Quad Flat Pack (MQFP). Performance specifications are guaranteed from 0°C to 70°C.

Block Diagram



65-1103-01

Rev. 1.1.0

Circuit Function

Within the TMC1103 are three 8-bit A/D converters, each employing two-step architecture to convert an analog input to a digital output at rates up to 50 Msps. Input signals are held in integral track/hold stages during the conversion process. Operation is pipelined, with one input sample taken and one output word provided for each CLK_X cycle.

Each of the three converters function identically. In the following descriptions 'X' refers to a generic input/output or clock where 'X' is equivalent to A, B or C.

The first step in the conversion process is a coarse 4-bit quantization. This determines the range of the subsequent fine 4-bit quantization step. To eliminate spurious codes, the fine 4-bit A/D quantizer output is gray-coded and converted to binary before it is combined with the coarse result to form a complete 8-bit result.

Analog Input and Voltage References

Each A/D accepts analog signals in the range R_{BX} to R_{TX} into digital data. Input signals outside this range produce "saturated" 00h or FFh output codes. The device will not be damaged by signals within the range A_{GND} to V_{DDA}.

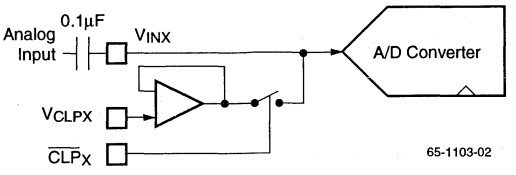
Input range is very flexible and extends from the +5 Volt power supply to ground. Nominal input range is 2 Volts, extending from 0.6V to 2.6V. Characterization and performance is specified over this range. However, the part will function with a full-scale range from 1.0V to 5.0V. A smaller input range may simplify analog signal conditioning circuitry, at the expense of additional noise sensitivity and some reduced differential linearity performance.

External voltage reference sources are connected to the R_{TX} and R_{BX} pins. R_{BX} can be grounded. Within each A/D converter is a reference resistor ladder comprising 255 resistors that are accessed by the TMC1103 comparators. R_{TX} is connected to the top of the ladder, R_{BX} to the bottom. Gain and offset errors are directly related to the accuracy and stability of the applied reference voltages.

Input Clamps

A clamp circuit is connected to the input pin V_{INX} of each of the three A/D converters. With $\overline{CLP_X}$ LOW, the input pin is clamped to the voltage at V_{CLPX}. If $\overline{CLP_X}$ is HIGH, the input pin is high impedance. Clamping adds an offset voltage to an AC coupled signal to adjust this signal's amplitude to the A/D converter input voltage range.

The analog input is corrected through a 0.1µF capacitor to V_{INX}. The source impedance of the analog source should be less than 50 Ohms. Current pulses through the capacitor over several clamp cycles until the voltage across the capacitor equals the difference between V_{CLPX} and the voltage at the analog source during the clamping period. When the switch is open, the voltage on the coupling capacitor is added to the analog input, producing a a DC offset input signal.



Input Clamp Circuit

Digital Inputs and Outputs

Sampling of the applied input signal occurs on the falling edge of the CLK_X signal (Figure 1). Output data is delayed by 2 1/2 CLK_X cycles and is valid following the rising edge of CLK_X. Previous output data remains valid for t_{HO} (Output Hold Time). New data becomes valid t_D (Output Delay Time) after this rising edge of CLK_X.

Whenever the analog input signal is sampled and found to be at a level beyond the A/D conversion range, the output limits at 00h or FFh, as appropriate.

Table 1. A/D Output Coding

Input Voltage	Output
R_{TX} + 1 LSB	FF
R_{TX}	FF
R_{TX} - 1 LSB	FE
• • •	• • •
R_{BX} + 128 LSB	80
R_{BX} + 127 LSB	7F
• • •	• • •
R_{BX} + 1 LSB	01
R_{BX}	00
R_{BX} - 1 LSB	00

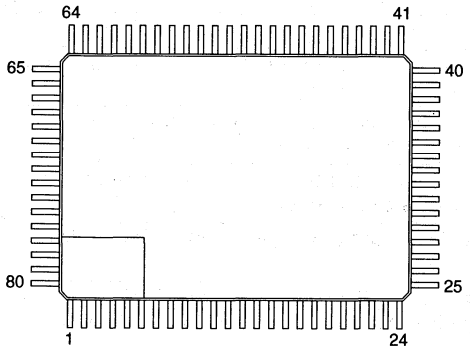
Note: 1 LSB = (R_{TX} – R_{BX}) / 255

The outputs of the TMC1103 are CMOS- and TTL-compatible, and are capable of driving four low-power Schottky TTL loads. An Output Enable control, $\overline{OE_X}$, places the A/D outputs in a high-impedance state when HIGH. The outputs are enabled when $\overline{OE_X}$ is LOW.

Power and Ground

The TMC1103 operates from a single +5 Volt power supply. For optimum performance, an analog ground plane should be placed under the TMC1103 the A_{GND} and D_{GND} pins should be connected to the system analog ground plane.

Pin Assignments



65-1103-03

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	21	DGND	41	DC_7	61	V_{DD}
2	DA_5	22	DGND	42	$\overline{OE}_C$	62	$\overline{OE}_B$
3	DA_6	23	NC	43	V_{DD}	63	DB_7
4	DA_7	24	NC	44	V_{DD}	64	DB_6
5	$\overline{OE}_A$	25	DGND	45	CLK_C	65	DB_5
6	V_{DD}	26	DGND	46	NC	66	DB_4
7	V_{DD}	27	V_{DD}	47	V_{DDA}	67	DB_3
8	NC	28	$\overline{CLP}_A$	48	V_{INC}	68	DB_2
9	CLK_A	29	$\overline{CLP}_B$	49	AGND	69	DB_1
10	NC	30	$\overline{CLP}_C$	50	R_{TC}	70	DB_0
11	V_{DDA}	31	NC	51	R_{BC}	71	DGND
12	V_{INA}	32	DGND	52	R_{BB}	72	DGND
13	AGND	33	DGND	53	R_{TB}	73	NC
14	R_{TA}	34	DC_0	54	AGND	74	DGND
15	R_{BA}	35	DC_1	55	V_{INB}	75	DGND
16	V_{CLPA}	36	DC_2	56	V_{DDA}	76	DA_0
17	V_{CLPB}	37	DC_3	57	NC	77	DA_1
18	V_{CLPC}	38	DC_4	58	CLK_B	78	DA_2
19	DGND	39	DC_5	59	NC	79	DA_3
20	DGND	40	DC_6	60	V_{DD}	80	DA_4

Pin Descriptions

Pin Name	Pin Number	Value	Pin Function Description
A/D Converters			
V_{INA}, V_{INB}, V_{INC}	12, 55, 48	R_{TX} to R_{BX}	**Analog Inputs.** The input voltage conversion range lies between the voltage applied to the R_{TX} and R_{BX} pins.
R_{TA}, R_{TB}, R_{TC}	14, 53, 50	2.6V	**Reference Voltage, Top Inputs.** DC voltages applied to R_{TA}, R_{TB} and R_{TC} define highest value of V_{INX}.
R_{BA}, R_{BB}, R_{BC}	15, 52, 51	0.6V	**Reference Voltage, Bottom Inputs.** DC voltages applied to R_{BA}, R_{BB} and R_{BC} define lowest value of V_{INX}.
CLK_A, CLK_B, CLK_C	9, 58, 45	CMOS	**Clock Inputs.** CMOS-compatible. V_{INX} is sampled on the falling edge of CLK_X.
DA_{7-0}	4, 3, 2, 80, 79, 78, 77, 76	CMOS/ TTL	**Data outputs, Converter A (D_7 = MSB).** Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLK_X.
DB_{7-0}	63, 64, 65, 66, 67, 68, 69, 70	CMOS/ TTL	**Data outputs, Converter B (D_7 = MSB).** Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLK_X.
DC_{7-0}	41, 40, 39, 38, 37, 36, 35, 34	CMOS/ TTL	**Data outputs, Converter C (D_7 = MSB).** Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLK_X.
$\overline{OE}_A$, $\overline{OE}_B$, $\overline{OE}_C$	5, 62, 42	CMOS	**Output Enable Inputs.** CMOS-compatible. When LOW, the A/D output is enabled. When HIGH, the output is in a high-impedance state.
Clamps			
V_{CLPA}, V_{CLPB}, V_{CLPB}	16, 17, 18	R_{TX} to R_{BX}	**Clamp Reference Voltage.** One reference for each clamp. A V_{INX} input is clamped to V_{CLPX} when $\overline{CLP}_X$ is low.
$\overline{CLP}_A$, $\overline{CLP}_B$, $\overline{CLP}_C$	28, 29, 30	CMOS	**Clamp Pulse Inputs.** One input for each A/D clamp. When $\overline{CLP}_X$ is low, the V_{INX} input is clamped to the V_{CLPX} clamp voltage.
Power			
V_{DDA}	11, 47, 56	+5V	**Analog Supply Voltage.** +5 Volt power inputs. These should come from the same power source and be decoupled to A_{GND}.
V_{DD}	6, 7, 27, 28, 29, 30, 43, 44, 60, 61	+5V	**Digital Supply Voltage.** +5 Volt power inputs. These should come from the same power source and be decoupled to A_{GND}.
A_{GND}	13, 49, 54	0.0V	**Analog Ground.** Ground connections. These pins should be connected to the system analog ground plane.
D_{GND}	16, 17, 18, 19, 20, 21, 22, 25, 26, 32, 33, 71, 72, 74, 75	0.0V	**Digital Ground.** Ground connections. These pins should be connected to the system analog ground plane.
No Connect			
N/C	1, 8, 10, 23, 24, 31, 46, 57, 59, 73	open	**Not Connected.**

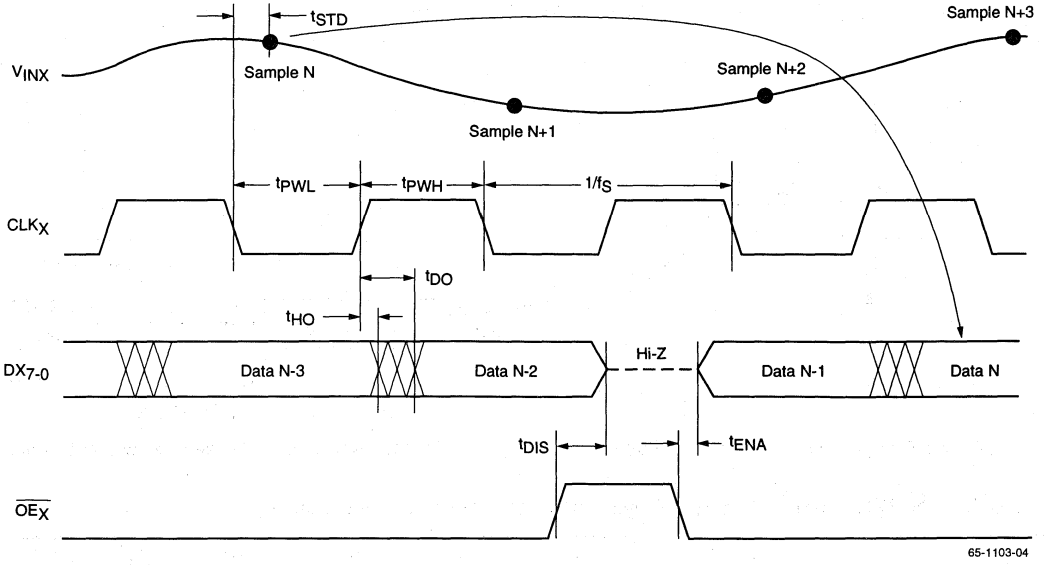


Figure 1. Timing

Equivalent Circuits and Threshold Levels

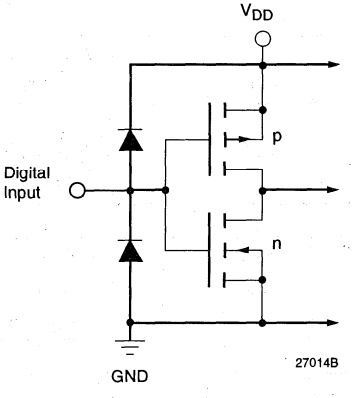


Figure 2. Equivalent Digital Input Circuit

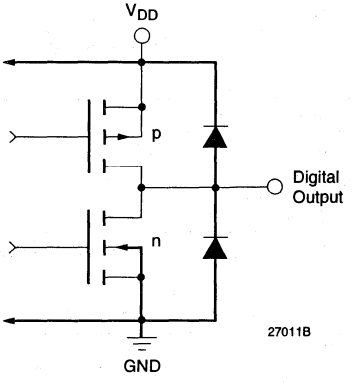


Figure 3. Equivalent Digital Output Circuit

Equivalent Circuits and Threshold Levels (continued)

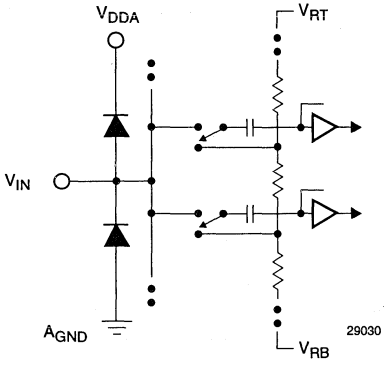


Figure 4. Equivalent Analog Input Circuit

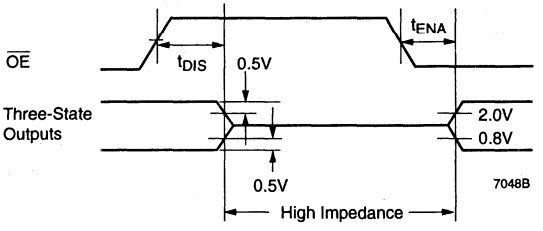


Figure 5. Threshold Levels for Three-State Measurements

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Condition	Min	Typ	Max	Unit
Power Supply Voltages					
VDDA	Measured to AGND	-0.5		+7.0	V
VDD	Measured to DGND	-0.5		+7.0	V
VDDA	Measured to VDD	-0.5		+0.5	V
AGND	Measured to DGND	-0.5		+0.5	V
Digital Inputs					
Applied Voltage	Measured to DGND	-0.5		VDD + 0.5	V
Forced current		-10.0		+10.0	mA
Analog Inputs					
Applied Voltage	Measured to AGND	-0.5		VDDA+0.5	V
Forced current		-10.0		+10.0	mA
Digital Outputs					
Applied voltage	Measured to DGND	-0.5		VDD + 0.5	V
Forced current		-6.0		+6.0	mA
Short circuit duration	Single output in HIGH state to ground)			1 second	
Temperature					
Operating, ambient		-20		110	°C
Junction				+150	°C
Lead, soldering	10 seconds			+300	°C
Vapor Phase soldering	1 minute			+220	°C
Storage		-65		+150	°C
Electrostatic Discharge	EIAJ test method			±150	V

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Min.	Nom	Max.	Units
V_{DD}, V_{DDA}	Power Supply Voltage	4.75	5.0	5.25	V
AGND	Analog Ground (Measured to D_{GND})	-0.1	0	0.1	V
V_{RTX}	Reference Voltage, Top		2.6	V_{DDA}	V
V_{RBX}	Reference Voltage, Bottom	0	0.6		V
V_{RTX}-V_{RBX}	Reference Voltage Differential	1.0	2.0	5.0	V
V_{INX}	Analog Input Range	V_{RB}		V_{RT}	V
V_{CLPX}	Clamp Reference Voltage, 50Ω max source	0			V
V_{IH}	Input Voltage, Logic HIGH	0.7 V_{DD}		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW	GND		0.3 V_{DD}	V
I_{OH}	Output Current, Logic HIGH			-4.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Min.	Typ[1]	Max.	Units
I_{DD}	Power Supply Current[1]	C_{LOAD} = 35pF, f_{CK} = f_S (3 A/Ds)				
		f_S = 20 Msps		60	90	mA
		f_S = 40 Msps		85	120	mA
		f_S = 50 Msps		98	135	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = V_{DDA} = Max.				
		CLK_X = LOW		24	45	mA
		CLK_X = HIGH		36	55	mA
PD	Total Power Dissipation[1]	C_{LOAD} = 35pF, f_{CK} = f_S (3 A/Ds)				
		f_S = 20 Msps		300	470	mW
		f_S = 40 Msps		425	630	mW
		f_S = 50 Msps		490	710	mW
C_{AI}	Input Capacitance, Analog	CLK_X = LOW		4		pF
		CLK_X = HIGH		12		pF
R_{IN}	Input Resistance		500			kΩ
R_{REF}	Reference Resistance		200	270	340	Ω
I_{CB}	Input Current, Analog				±5	µA
I_{IH}	Input Current, HIGH	V_{DD} = Max., V_{IN} = V_{DD}			±5	µA
I_{IL}	Input Current, LOW	V_{DD} = Max., V_{IN} = 0V			±5	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max., V_{IN} = V_{DD}			±5	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max., V_{IN} = V_{DD}			±5	µA
I_{OS}	Short-Circuit Current				35	mA

Electrical Characteristics (continued)

Parameter		Conditions	Min.	Typ[1]	Max.	Units
V_{OH}	Output Voltage, HIGH	I_{OH} = -2.5mA	3.5			V
		I_{OH} = Max.	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max.			0.4	V
C_{DI}	Digital Input Capacitance			4	10	pF
C_{DO}	Digital Output Capacitance			10		pF

Note:
1. Typical values with V_{DD} = V_{DDA} = Nom and T_A = Nom, Maximum values with V_{DD} = V_{DDA} = Max. and T_A = Min.

Switching Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
f_S	Conversion Rate					
	TMC1103-20				20	Msps
	TMC1103-40				40	Msps
	TMC1103-50				50	Msps
t_{PWH}	CLKX Pulsewidth, HIGH					
	TMC1103-20		14			ns
	TMC1103-40		14			ns
	TMC1103-50		13			ns
t_{PWL}	CLKX Pulsewidth, LOW					
	TMC1103-20		8			ns
	TMC1103-40		8			ns
	TMC1103-50		7			ns
E_{AP}	Aperture Error			30		ps
t_{STO}	Sampling Time Offset		1	2	5	ns
t_{STS}	Sampling Time Skew			150	400	ps
t_{CPW}	Clamp Pulse Width[1]	+20 < T_A < +70°C	2			µS
t_{CDLY}	Clamp Delay Time		100		300	ns
t_{HO}	Output Hold Time	CLOAD = 15pF	9			ns
t_{DO}	Output Delay Time				14	ns
t_{ENA}	Output Enable Time				27	ns
t_{DIS}	Output Disable Time				42	ns

System Performance Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
E_{LI}	Integral Linearity Error, Independent	V_{RT} = 2.6V		±0.5		LSB
E_{LD}	Differential Linearity Error	V_{RB} = 0.6V		±0.5		LSB
BW	Bandwidth[1]	TMC1203-20			10	MHz
		TMC1203-40			12	MHz
		TMC1203-50			12	MHz
E_{OT}	Offset Voltage, Top (R_T – V_{IN} for most positive code transition)	V_{RT} = 2.6V, V_{RB} = 0.6V	-40		80	mV
E_{OB}	Offset Voltage, Bottom (R_B – V_{IN} for most negative code transition)	V_{RT} = 2.6V, V_{RB} = 0.6V	-95		-30	mV
OFF_{CL}	Offset Voltage, Clamp				±20	mV
dg	Differential Gain	f_S = 14.3Msps NTSC 40 IRE Mod Ramp V_{DDA} = +5.0V, T_A=25°C V_{RT} = 2.6V, V_{RB} = 0.6V		1.8		%
dp	Differential Phase	f_S = 14.3Msps NTSC 40 IRE Mod Ramp V_{DDA} = +5.0V, T_A=25°C V_{RT} = 2.6V, V_{RB} = 0.6V		0.7		deg
XTALK	Channel Crosstalk	f_N = 5.0 MHz		45		dB
SNR	Signal-to-Noise Ratio	f_S = 20Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_N = 1.24MHz		46		dB
		f_N = 2.48MHz		46		dB
		f_N = 6.98MHz		45		dB
		f_N = 10.0MHz		45		dB
		f_S = 40Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_N = 1.24MHz		42		dB
		f_N = 6.98MHz		41		dB
		f_N = 12.0MHz		40		dB
		f_S = 50Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_N = 1.24MHz		40		dB
		f_N = 6.98MHz		40		dB
		f_N = 12.0MHz		40		dB

System Performance Characteristics (continued)

Parameter		Conditions	Min.	Typ.	Max.	Units
SFDR	Spurious-Free Dynamic Range	f_S = 20Msps, V_{IN} = 2V p-p				
		f_N = 1.24MHz		53		dB
		f_N = 2.48MHz		48		dB
		f_N = 6.98MHz		44		dB
		f_N = 10.0MHz		40		dB
		f_S = 40Msps, V_{IN} = 2V p-p				
		f_N = 1.24MHz		49		dB
		f_N = 6.98MHz		44		dB
		f_N = 12.0MHz		38		dB
		f_S = 50Msps, V_{IN} = 2V p-p				
		f_N = 1.24MHz		46		dB
		f_N = 6.98MHz		40		dB
		f_N = 12.0MHz		37		dB

Notes:

1. Bandwidth is the frequency up to which a full-scale sinewave can be digitized without spurious codes.
2. Values shown in Typ. column are typical for V_{DD} = V_{DDA} = +5V and T_A = 25°C.
3. SNR values do not include the harmonics of the fundamental frequency.
4. SFDR is the ratio in dB of fundamental amplitude to the harmonic with the highest amplitude.
5. Characteristics specified for V_{RT} = 2.6V, V_{RB} = 0.6V.

Typical Performance Characteristics

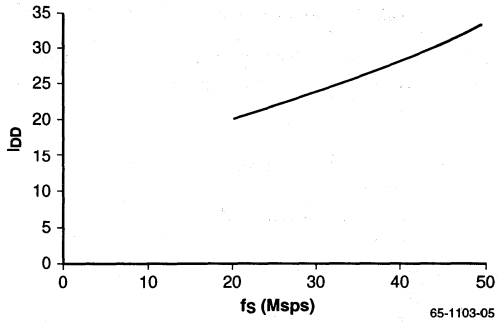


Figure 6. Typical I_{DD} vs f_S (Single A/D)

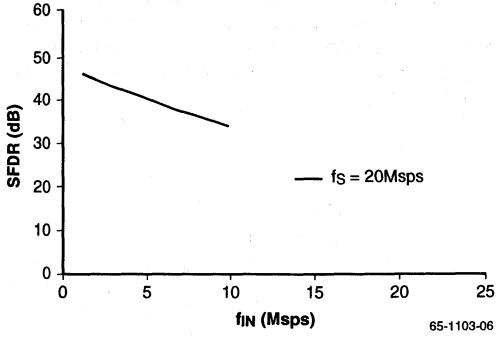


Figure 7. Typical SFDR vs f_{IN}

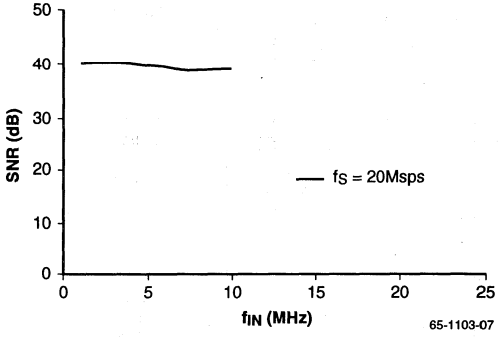


Figure 8. Typical SNR vs f_{IN}

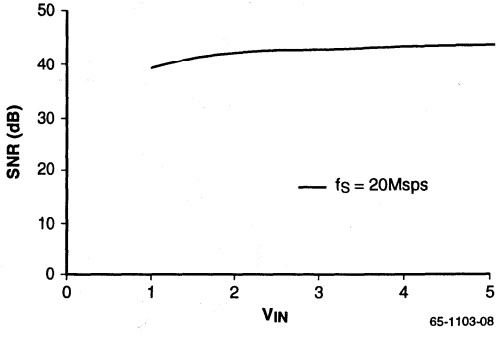


Figure 9. Typical SNR vs Full Scale Input Range

Application Notes

The circuit in Figure 10 employs a band-gap reference to generate a variable R_{TX} reference voltages for the TMC1103 as well as a bias voltage to offset the wideband input amplifiers to mid-range. The operational amplifier in the reference circuitry is a standard 741-type.

The voltage reference at R_{TX} can be adjusted from 0.0 to 2.4 volts while R_{BX} is grounded. Schottky diodes can be used at V_{INX} to restrict the wideband amplifier output to between -0.3V and V_{DD} +0.3V. Diode protection is good practice to limit the analog input voltage at V_{INX} to the safe operating range.

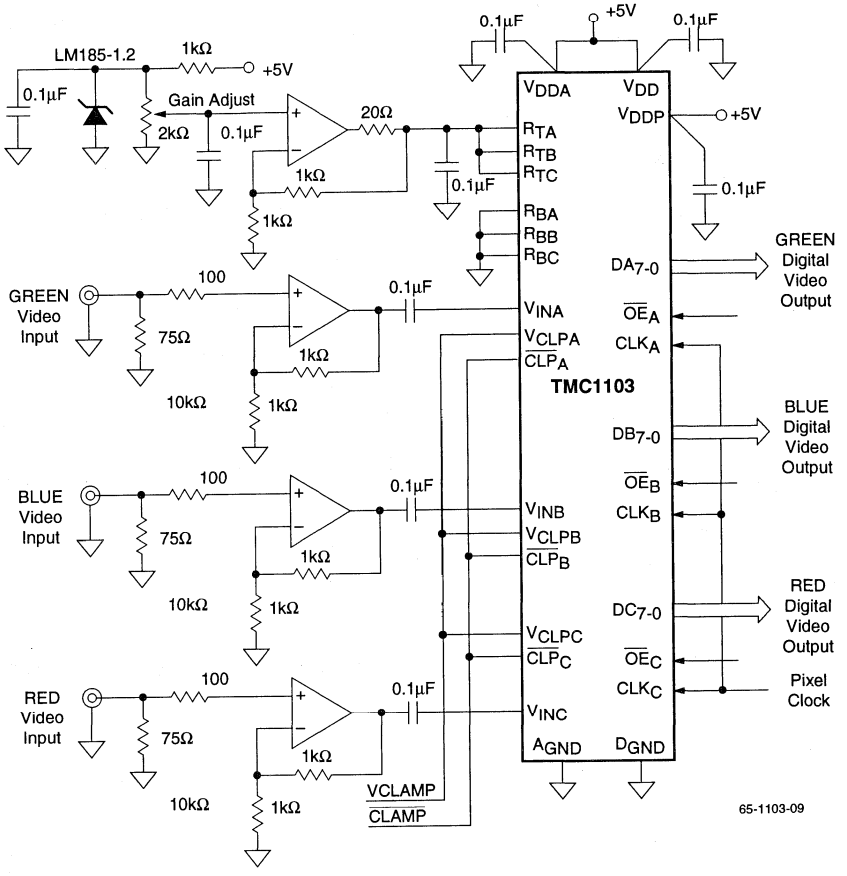


Figure 10. Typical Interface Circuit – High Performance

Grounding

The TMC1103 has separate analog and digital circuits. To keep digital system noise from the A/D converter, it is recommended that power supply voltages (V_{DD} and V_{DDA}) come from the same source, and that ground connections (D_{GND} and A_{GND}) be made to the analog ground plane, and as close as possible to the device pins. Power supply pins should be individually decoupled at the pin. The digital circuitry that gets its input from the TMC1103 should be referred to the system digital ground plane.

Printed Circuit Board Layout

Designing with high performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_N, R_{TX}, R_{BX}) as short as possible and as far as possible from all digital signals. The TMC1103 should be located close to the analog input connectors.

2. The power plane for the TMC1103 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC1103 is the same as that of the system's digital circuitry, power to the TMC1103 should be decoupled with ferrite beads and 0.1µF capacitors to reduce noise.

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They supply different circuits on the integrated circuit, each of which generate varying amounts and types of noise. For best results, use 0.1µF ceramic capacitors. Lead lengths should be minimized.

5. CLK$_X$ should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line, if needed, to eliminate overshoot and ringing.

Related Products

- TMC1175A, TMC1275 8-Bit Video A/D Converters
- TMC1173A, TMC1273 3V, Low-Power 8-Bit Video A/D Converters
- TMC1203 Triple 8-bit A/D Converter
- TMC3003/TMC3503 Triple Video D/A Converters
- TMC2242B/TMC2243/TMC2246A Digital Filters

Ordering Information

Product Number	Conversion Rate (Msps)	Temperature Range	Screening	Package	Package Marking
TMC1103KLC20	20 Msps	T_A = 0°C to 70°C	Commercial	80-Lead MQFP	1203KLC20
TMC1103KLC40	40 Msps	T_A = 0°C to 70°C	Commercial	80-Lead MQFP	1203KLC40
TMC1103KLC50	50 Msps	T_A = 0°C to 70°C	Commercial	80-Lead MQFP	1203KLC50

TMC1173A/TMC1273

Video A/D Converter

8 bit, 20 Msps, 3V

Features

- 8-bit resolution
- 20 Msps conversion rate
- Low power: 15mW @ 5 Msps
- Integral track/hold
- Integral and differential linearity error 0.5 LSB
- Single +3V power supply
- Three-state TTL/CMOS-compatible outputs
- Low cost

Applications

- Video digitizing
- VGA and CCD digitizing
- LCD projection panels
- Image scanners
- Personal computer video boards
- Multimedia systems
- Low cost, high speed data conversion

Description

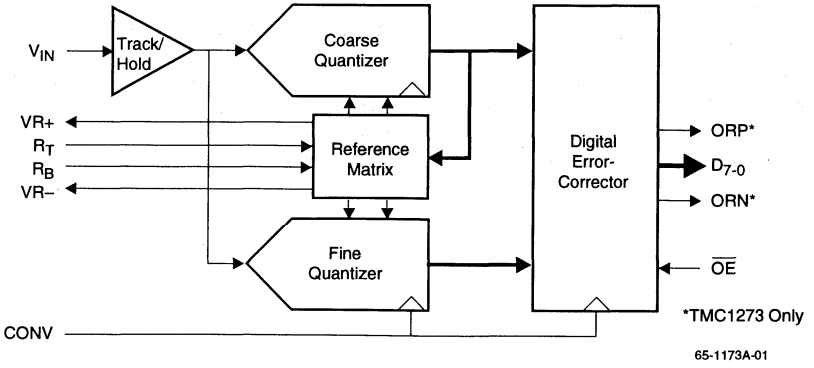
The TMC1173A/1273 analog-to-digital (A/D) converter employs a two-step architecture to convert analog signals into 8-bit digital words at sample rates of up to 20 Msps (Megasamples per second). An integral Track/Hold circuit delivers excellent performance on signals with full-scale frequency components up to 5 MHz. The innovative architecture and submicron CMOS technology limit typical power dissipation to 15 mW.

The TMC1173A/1273 operates from a single +2.7 to +3.6 Volt power supply and has internal voltage reference resistors for self-bias operation. Input capacitance is very low, simplifying or eliminating input driving amplifiers. All digital three-state outputs are 3V TTL- and CMOS-compatible.

The TMC1173A and TMC1273 share their core architectures; the TMC1273 adds two overrange outputs that indicate when the analog input signal is beyond the conversion range.

The TMC1173A/1273 is available in 24-pin plastic DIP, 24-lead plastic SOIC, and 28-lead J-lead PLCC packages. Performance specifications are guaranteed from -20°C to 75°C.

Block Diagram



Functional Description

The TMC1173A/1273 8-bit A/D converter uses a two-step architecture to perform analog-to-digital conversion at rates up to 20 Msps. The input signal is held in an integral track/hold stage during the conversion process. Operation is pipelined, with one input sample taken and one output word provided for each CONVert cycle.

The first step in the conversion process is a coarse 4-bit quantization. This determines the range of the subsequent fine 4-bit quantization step. To eliminate spurious codes, the fine 4-bit A/D quantizer output is gray-coded and converted to binary before it is combined with the coarse result to form a complete 8-bit result.

The TMC1173A/1273 is characterized and specified for use in "3 Volt" applications where the power supply voltage can be as low as 2.7V.

Analog Input and Voltage References

The TMC1173A/1273 converts analog signals in the range R_B to R_T into digital data. Input signals outside that range produce "saturated" 00h or FFh output codes. The device will not be damaged by signals within the range A_{GND} to V_{DDA}.

The A/D converter input range is very flexible and extends from the +3.3 Volt power supply to ground. The nominal input range is 1.56 Volts, from 0.36V to 1.92V. The circuit is characterized and performance is specified over that range. However, the part will work well with a full-scale range from 1.0V to 3.0V. A reduced input range may simplify analog signal conditioning circuitry, at the expense of additional noise sensitivity and some reduced differential linearity performance. Similarly, increasing the range can improve differential linearity, but puts a greater burden on the input signal conditioning circuitry.

In many applications, external voltage reference sources are connected to the R_T and R_B pins. R_B can be grounded. Gain and offset errors are directly related to the accuracy and stability of the applied reference voltages.

Two reference pull-up and pull-down resistors connected to VR+ and VR-, are provided internally for operation without external voltage reference circuitry (Figure 1). The reference voltages applied to R_T and R_B may be generated by connecting VR+ to R_T and VR- to R_B. The power supply voltage is divided by the on-chip resistors to bias the R_T and R_B points. This sets-up the converter for operation in its nominal range from 0.4V to 1.6V.

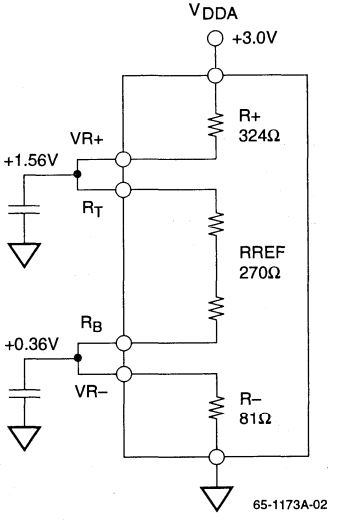


Figure 1. Reference Resistors

With V_{DDA} at 3.0V, connecting VR+ to R_T and grounding R_B will provide an input range from 0.0V to 1.36V, while connecting R_T to V_{DDA} and R_B to VR- produces a full scale range of 2.31V referenced to V_{DDA}. External resistors may also be employed to provide arbitrary reference voltages, but they will not match the temperature coefficient of the on-chip resistors as well as R+ and R-, and will cause the converter transfer function to vary with temperature.

With this implementation, errors in the power supply voltage end up on the conversion data output.

Because a two-step conversion process is employed, it is important that the references remain stable during the ENTIRE conversion process (two clock cycles). The reference voltage can then be changed, but any conversion in progress during a reference change is invalid.

Table 1. Output Coding

Input Voltage	ORP[2]	ORN[2]	Output
R_T + 1 LSB	1	0	FF
R_T	0	0	FF
R_T – 1 LSB	0	0	FE
• • •	• • •	• • •	• • •
R_B + 128 LSB	0	0	80
R_B + 127 LSB	0	0	7F
• • •	• • •	• • •	• • •
R_B + 1 LSB	0	0	01
R_B	0	0	00
R_B – 1 LSB	0	1	00

Notes:
1. LSB = (R_T – R_B) / 255
2. TMC1273 Only

Digital Inputs and Outputs

Sampling of the applied input signal takes place on the falling edge of the CONV signal (Figure 2). The output word is delayed by 2 1/2 CONV cycles. It is then available after the rising edge of CONV. The previous data on the output remain valid for t_{HO} (Output Hold Time), satisfying any hold time requirement of the receiving circuit. The new data become valid t_{DO} (Output Delay Time) after this rising edge of CONV.

Whenever the analog input signal is sampled and found to be at a level beyond the A/D conversion range, an Overrange output of the TMC1273 will go HIGH. If the input is more positive (by at least one LSB) than the positive end of the range, ORP will go HIGH and D_{7-0} will be FFh. If the input is more negative (by at least one LSB) than the negative end of the range, ORN will go HIGH and D_{7-0} will be 00h.

The outputs of the TMC1173A/1273 are CMOS- and 3V TTL-compatible, and are capable of driving four low-power Schottky TTL (54/74LS) loads. An Output Enable control, $\overline{OE}$, places the outputs in a high-impedance state when HIGH. The outputs are enabled when $\overline{OE}$ is LOW.

Power and Ground

The TMC1173A/1273 operates from a single +2.7 to +3.6 Volt power supply. For optimum performance, it is recommended that A_{GND} and D_{GND} pins of the TMC1173A/1273 be connected to the system analog ground plane.

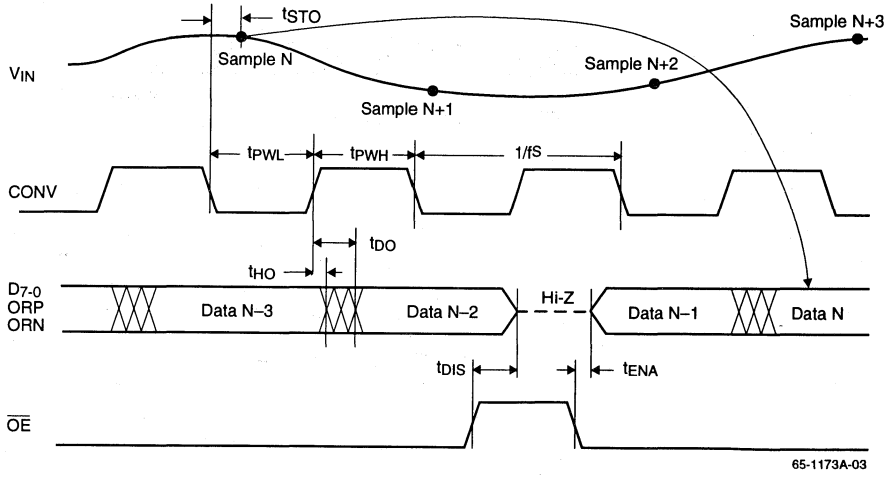


Figure 2. Conversion Timing

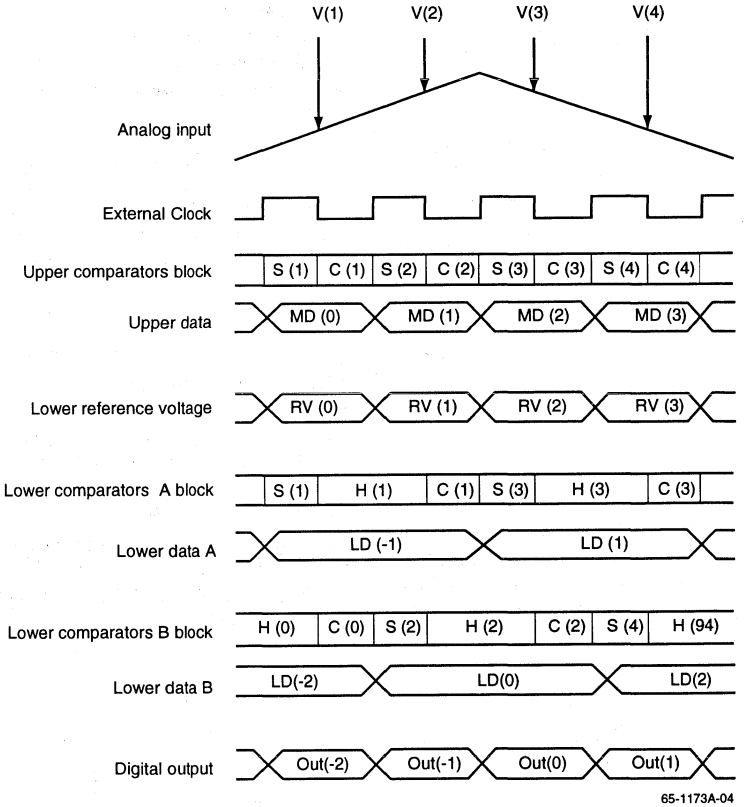
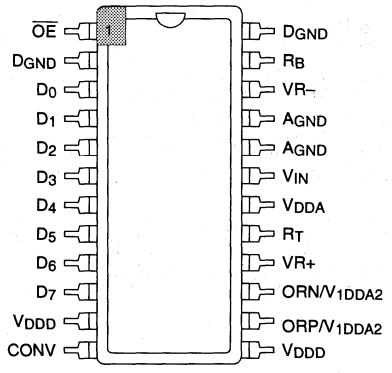
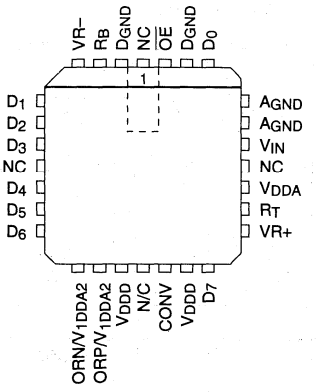


Figure 3. Internal Timing

Pin Assignments



N2 Package
M7 Package



R3 Package

65-1173A-05

Pin Description

Pin Name	Pin Number N2, M7	Pin Number R3	Pin Type	Pin Function Description
Inputs				
V_{IN}	19	23	$R_T - R_B$	**Analog Input.** The input voltage conversion range lies between the voltages applied to the RT and RB pins.
R_T	17	20	1.6V	**Reference Voltage Top Input.** R_T is the top input to the reference resistor ladder. A DC voltage applied to R_T defines the positive end of the V_{IN} conversion range.
R_B	23	27	0.4V	**Reference Voltage Bottom Input.** R_B is the bottom input to the reference resistor ladder. A DC voltage applied to R_B defines the negative end of the V_{IN} conversion range.
VR+	16	19		**Reference Voltage Top Source.** VR+ is the internal pull-up reference resistor for self-bias operations.
VR–	22	26		**Reference Voltage Bottom Source.** VR- is the internal pull-down reference resistor for self-bias operations.
$\overline{OE}$	1	2	CMOS	**Output Enable.** (CMOS-compatible) When LOW, D_{7-0} are enabled. When HIGH, D_{7-0} are in a high-impedance state.
CONV	12	14	CMOS	**Convert (Clock) Input.** (CMOS-compatible) V_{IN} is sampled on the falling edge of CONV.
Outputs				
D_{7-0}	10–3	12–9, 7–4	CMOS/ 3V TTL	**Data Outputs (D7 = MSB).** Eight-bit CMOS- and 3V TTL-compatible digital outputs. Data is output following the rising edge of CONV.
ORP[1]	14[1]	17[1]	CMOS/ 3V TTL	**OverRange Positive Output.** When HIGH, ORP indicates that the analog input voltage is at least one LSB higher than the voltage that produces output code FFh. ORP is synchronous with D_{7-0}.
ORN[1]	15[1]	18[1]	CMOS/ 3V TTL	**OverRange Negative Output.** When HIGH, ORN indicates that the analog input voltage is at least one LSB lower than the voltage that produces output code 00h. ORN is synchronous with D_{7-0}.

Pin Description (continued)

Pin Name	Pin Number N2, M7	Pin Number R3	Pin Type	Pin Function Description
Power				
VDDA	14[2], 15[2], 18	17[2], 18[2], 21	+3.3V	**Analog Supply Voltage.** These should originate from a common +3.3V source and be decoupled to AGND.
VDDD	11, 13	13, 16	+3.3V	**Digital Supply Voltage.** +3.3 Volt power inputs. These should originate from a common +3.3V power source and be decoupled to AGND.
AGND	20, 21	24, 25	0.0V	**Analog Ground.** Connect to the system analog ground plane.
DGND	2, 24	3, 28	0.0V	**Digital Ground.** Connect to the system analog ground plane.
No Connect				
N/C		1, 8, 15, 22	open	Not Connected.

Notes:
1. TMC1273 Only.
2. TMC1173A Only.

Preliminary Information

Specification Notes

Bandwidth

The specification for bandwidth of an A/D converter is somewhat different from the normal frequency-response specification used in amplifiers and filters. An understanding of the differences will help in selecting converters properly for particular applications.

A/D conversion comprises two distinct processes: sampling and quantizing. Sampling is "grabbing" a snapshot of the input signal and holding it steady for quantizing. The quantizing process is approximating the analog input, which may be any value within the conversion range, with its nearest numerical value. While sampling is a high-frequency process, quantizing operates on a dc signal, held steady by the track/hold circuit. Therefore, the sampling process is what relates to the dynamic characteristics of the converter.

Sampling involves an aperture time, the time during which the track/hold is trying to capture the input signal and settle on a dc value to hold. It is analogous to the shutter speed of a camera: the shorter the aperture (or faster the shutter) the less the signal will be blurred, and the less uncertainty there will be in the quantized value.

For example, a 10 MHz sinewave with a 1V peak amplitude (2Vp-p) has a maximum slew rate of $2\pi fA$ at zero crossing, or 62.8V/µs. With an 8-bit A/D converter, q (the quantization step size) = 2V/255 = 7.8mV. The input signal will slew one LSB in 124ps. To limit the error (and noise) contribution due to aperture effects to 1/2LSB, the aperture must be shorter than 62ps.

This is the primary reason that the signal to noise ratio drops off as full scale frequency increases. Note, also, that the slew rate is directly proportional to signal amplitude, A. A/Ds will handle lower-amplitude signals of higher bandwidth.

All this is of particular interest in applications such as digitizing analog VGA RGB signals, or the output of a CCD imaging chip. These data are effectively pre-sampled: there is a period of rapid slewing from one pixel value to another, followed by a relatively stable dc level before the signal slews to the next pixel value. The goal is, of course, to sample on these pixel values, not on the slewing between pixels. During the aperture time, the A/D sees essentially a dc signal, and classic bandwidth considerations are not important. As long as the input circuit can slew and settle to the new value in the prescribed period, an accurate conversion will be made.

The TMC1173A/1273 is capable of slewing a full 2V and settling between samples taken as little as 25ns apart, making it ideal for digitizing analog VGA and CCD outputs.

Equivalent Circuits and Threshold Level

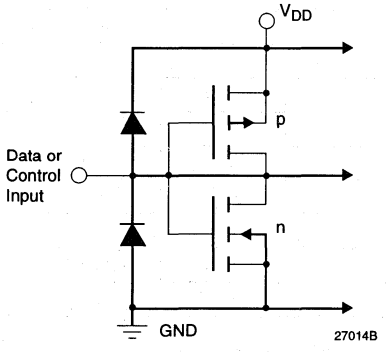


Figure 4. Equivalent Digital Input Circuit

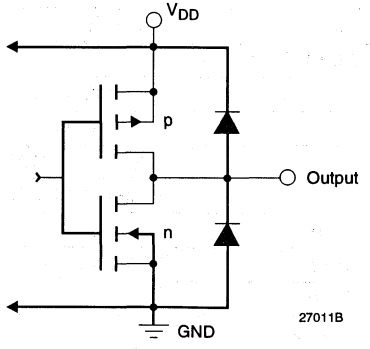


Figure 5. Equivalent Digital Output Circuit

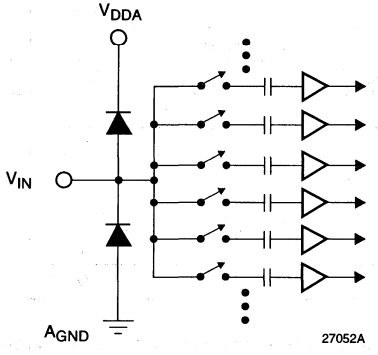


Figure 6. Equivalent Analog Input Circuit

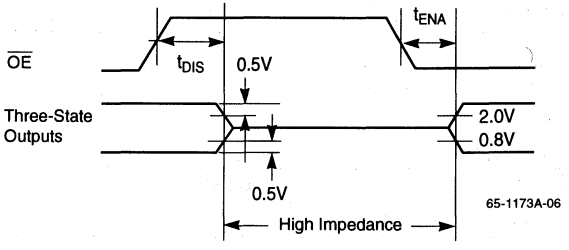


Figure 7. Threshold Levels for Three-State Measurements

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Conditions	Min	Max	Unit
Power Supply Voltages				
V_{DDA}	Measured to A_{GND}	-0.5	7.0	V
V_{DDD}	Measured to D_{GND}	-0.5	7.0	V
V_{DDA}	Measured to V_{DDD}	-0.5	0.5	V
A_{GND}	Measured to D_{GND}	-0.5	0.5	V
Digital Inputs				
Applied Voltage[2]	Measured to D_{GND}	-0.5	V_{DDD} + 0.5	V
Forced Current[3,4]		-10.0	10.0	mA
Analog Inputs				
Applied Voltage[2]	Measured to A_{GND}	-0.5	V_{DDA} + 0.5	V
Forced Current[3,4]		-10.0	10.0	mA
Outputs				
Applied Voltage[2]	Measured to D_{GND}	-0.5	V_{DDD} + 0.5	V
Forced Current[3,4]		-6.0	6.0	mA
Short Circuit Duration	Single output in HIGH state to ground		1	sec
Temperature				
Operating, ambient		-20	110	°C
Junction			150	°C
Storage		-65	150	°C
Lead Soldering	10 seconds		300	°C
Vapor Phase Soldering	1 minute		220	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DDD}	Digital Power Supply Voltage		2.7	3.0	3.6	V
V_{DDA}	Analog Power Supply Voltage		2.7	3.0	3.6	V
A_{GND}	Analog Ground (Measured to D_{GND})		-0.1	0	0.1	V
f_S	Conversion Rate	TMC1173A/1273-5			5	Msps
		TMC1173A/1273-10			10	
		TMC1173A/1273-20			20	
t_{PWH}	CONV Pulsewidth, HIGH		20			ns
t_{PWL}	CONV Pulsewidth, LOW		17			ns
V_{RT}	Reference Voltage, Top		1.5	1.56	V_{DDA}	V
V_{RB}	Reference Voltage, Bottom		0	0.36	1.5	V
V_{RT}-V_{RB}	Reference Voltage Differential		1.0		3.0	V

Operating Conditions (continued)

Parameter			Min	Nom	Max	Units
V_{IN}	Analog Input Range		V_{RB}		V_{RT}	V
V_{IH}	Input Voltage, Logic HIGH		0.85 x V_{DDD}		V_{DDD}	V
V_{IL}	Input Voltage, Logic LOW		GND		0.2 x V_{DDD}	V
I_{OH}	Output Current, Logic HIGH				-1.0	mA
I_{OL}	Output Current, Logic LOW				2.0	mA
T_A	Ambient Temperature, Still Air		-20		75	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Units
I_{DD}	Power Supply Current[1]	V_{DDD} = V_{DDA} = Max, C_{LOAD} = 35pF				mA
		f_S = 5Msps		5	12	
		f_S = 10Msps		8	15	
		f_S = 20Msps		14	24	
I_{DDQ}	Power Supply Current, Quiescent	V_{DDD} = V_{DDA} = Max				
		CONV = LOW		2	9	mA
		CONV = HIGH		3	11	mA
P_D	Total Power Dissipation	V_{DDD} = V_{DDA} = Max, C_{LOAD} = 35pF				mW
		f_S = 5Msps		15	45	
		f_S = 10Msps		24	55	
		f_S = 20Msps		42	86	
C_{AI}	Input Capacitance, Analog	CONV = LOW		4		pF
		CONV = HIGH		12		pF
R_{IN}	Input Resistance		500	1000		kΩ
I_{CB}	Input Current, Analog				±1	µA
R_{REF}	Reference Resistance		200	270	340	Ω
I_{IH}	Input Current, HIGH	V_{DDD} = Max, V_{IN} = V_{DDD}			±5	µA
I_{IL}	Input Current, LOW	V_{DDD} = Max, V_{IN} = 0V			±5	µA
I_{OZH}	Hi-Z Output Leakage	V_{DDD} = Max, V_{IN} = V_{DDD}			±5	µA
I_{OZL}	Hi-Z Output Leakage	V_{DDD} = Max, V_{IN} = 0V			±5	µA
I_{OS}	Short-Circuit Current				-30	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = -100µA	V_{DDD}-0.3			V
		I_{OH} = -0.5mA	2.5			V
		I_{OH} = Max	2.1			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max			0.3	V
C_{DI}	Digital Input Capacitance			4	10	pF
C_{DO}	Digital Output Capacitance			10		pF

Note:

1. Typical values with V_{DDD} = V_{DDA} = Nom and T_A = Nom, Minimum/Maximum values with V_{DDD} = V_{DDA} = Max and T_A = Min.

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{STO}	Sampling Time Offset		3	5	8	ns
t_{HO}	Output Hold Time	C_{LOAD} = 15pF	5			ns
t_{DO}	Output Delay Time	C_{LOAD} = 15pF			32	ns
t_{ENA}	Output Enable Time				40	ns
t_{DIS}	Output Disable Time				45	ns

System Performance Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Units
E_{LI}	Integral Linearity Error, Independent	V_{RT} - V_{RB} ≥ 1.2V		±0.5	±0.75	LSB
E_{LD}	Differential Linearity Error	V_{RT} - V_{RB} ≥ 1.2V		±0.5	±0.75	LSB
BW	Bandwidth[2]	TMC1173A/1273-5			5	MHz
		TMC1173A/1273-10			5	
		TMC1173A/1273-20			10	
E_{AP}	Aperture Error			50		ps
E_{OT}	Offset Voltage, Top	R_T – V_{IN} for most positive code transition	-25	-2	25	mV
E_{OB}	Offset Voltage, Bottom	R_B – V_{IN} for most negative code transition	15	20	45	mV

Notes:

1. Values shown in Typ column are typical for V_{DDD} = V_{DDA} = +3.0V and T_A = 25°C.
2. Bandwidth is the frequency up to which a full-scale sinewave can be digitized without spurious codes.

System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Units
SNR	Signal-to-Noise Ratio	f_S = 5Msps, V_{IN} = 1.2V p-p				
		f_{IN} = 1.24MHz	42	47		dB
		f_{IN} = 2.48MHz	41	46		
		f_S = 10Msps, V_{IN} = 1.2V p-p				
		f_{IN} = 1.24MHz	42	47		dB
		f_{IN} = 2.48MHz	40	45		
		f_{IN} = 4.96MHz	34	39		
		f_S = 20Msps, V_{IN} = 1.2V p-p				
		f_{IN} = 1.24MHz	38	44		dB
		f_{IN} = 2.48MHz	37	42		
		f_{IN} = 6.98MHz	26	32		
		f_{IN} = 10MHz	25	30		

System Performance Characteristics (continued)

Parameter		Conditions	Min	Typ	Max	Units
SFDR	Spurious-Free Dynamic Range	f_S = 5Msps, V_{IN} = 1.2V p-p				
		f_{IN} = 1.24MHz	37	43		dB
		f_{IN} = 2.48MHz	32	37		
		f_S = 10Msps, V_{IN} = 1.2V p-p				
		f_{IN} = 1.24MHz	37	43		dB
		f_{IN} = 2.48MHz	32	37		
		f_{IN} = 4.96MHz	26	32		
		f_S = 20Msps, V_{IN} = 1.2V p-p				
		f_{IN} = 1.24MHz	34	40		dB
		f_{IN} = 2.48MHz	31	37		
		f_{IN} = 6.98MHz	25	31		
		f_{IN} = 10MHz	22	28		

Notes:
1. SNR values do not include the harmonics of the fundamental frequency.
2. SFDR is the ratio in dB of fundamental amplitude to the harmonic with the highest amplitude.
3. Values shown in Typ column are typical for V_{DDD} = V_{DDA} = +3.3V and T_A = 25°C.

Typical Performance Characteristics

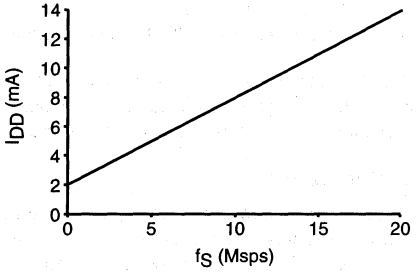


Figure 8. Typical I_{DD} vs f_S

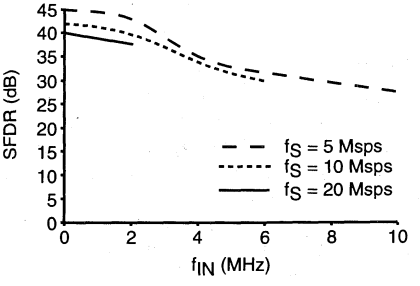


Figure 9. Typical SFDR vs f_{IN} and f_S

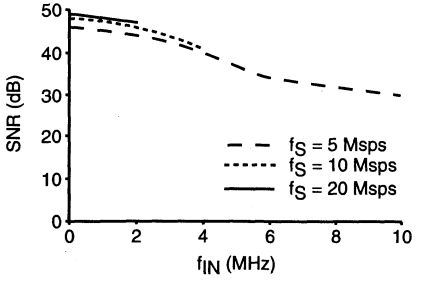


Figure 10. Typical SNR vs f_{IN} and f_S

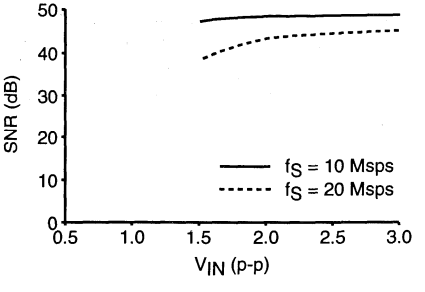


Figure 11. Typical SNR vs Full Scale Input Range

Applications Discussion

The circuit in Figure 12 employs a band-gap reference to generate a variable RT reference voltages for the TMC1173A/1273 as well as a bias voltage to offset the inverting wideband input amplifier to mid-range. An "offset adjust" is also shown for varying the mid-range voltage level. The operational amplifier in the reference circuitry is a standard 741-type.

The voltage reference at R_T can be adjusted from 0.0 to 2.4 volts while R_B is grounded. Diodes are used to restrict the wideband amplifier output to between -0.7V and V_{DD} +0.7V. Diode protection is good practice to limit the analog input voltage at V_{IN} to the safe operating range.

The circuit in Figure 13 shows self-bias of R_T and R_B by connection to VR+ and VR-. This sets up a 0.4 to 1.7 Volt input range for V_{IN}. The input range is susceptible to power supply variation since the voltages on R_T and R_B are directly derived from V_{DDA}. The video input is AC-coupled and biased at a adjustable midpoint of the A/D input range. This circuit offers the advantage of minimum support circuitry for the most cost-sensitive applications.

In Figure 14, an external band-gap reference sets R_T to +1.2 Volts while R_B is grounded. The internal pull-up resistor, R+, provides the bias current for the band-gap reference. The A/D converter input is biased to the mid-point of the input range.

Grounding

The TMC1173A/1273 has separate analog and digital circuits. To keep digital system noise from the A/D converter, it is recommended that power supply voltages (V_{DDD} and V_{DDA}) come from the same source, and that ground connections (D_{GND} and A_{GND}) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin. The digital circuitry that gets its input from the TMC1173A/1273 should be referred to the system digital ground plane.

Printed Circuit Board Layout

Designing with high performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is likely to degrade performance. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{IN}, R_T, R_B, VR+, VR-) as short as possible and as far as possible from all digital signals. The TMC1173A/1273 should be located near the board edge, close to the analog input connectors.

2. The power plane for the TMC1173A/1273 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC1173A/1273 is the same as that of the system's digital circuitry, power to the TMC1173A/1273 should be decoupled with ferrite beads and 0.1µF capacitors to reduce noise.

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They supply different circuits on the integrated circuit, each of which generate varying amounts and types of noise. For best results, use 0.1µF ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not be placed under the TMC1173A/1273, the voltage reference, or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC1173A/1273 and its related analog circuitry can have an adverse effect on performance.

6. CONV should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Evaluation Board

An evaluation board is available that implements good interface practices and provide a convenient testbed for developing system applications and circuit variations. An on-board D/A converter is provided to reconstruct the digitized signal and to evaluate converter performance.

Contact your sales representative for information.

Typical Interface Circuits

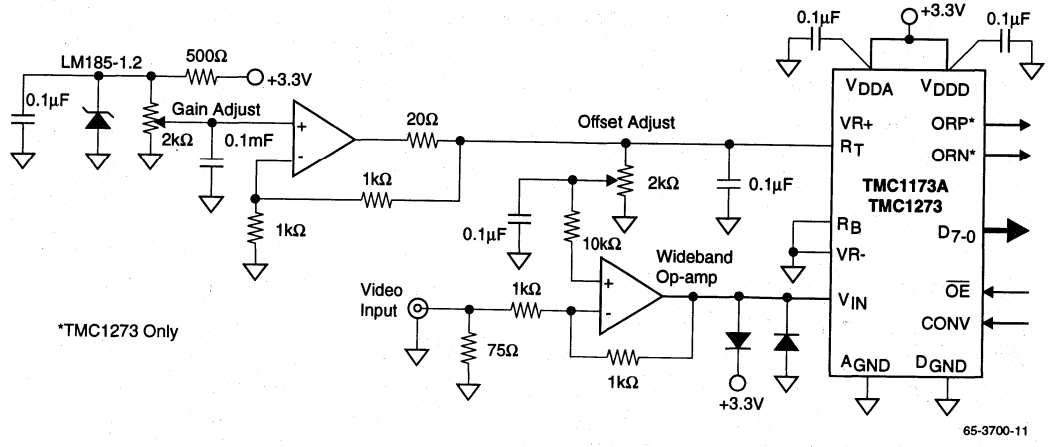


Figure 12. High Performance Circuit

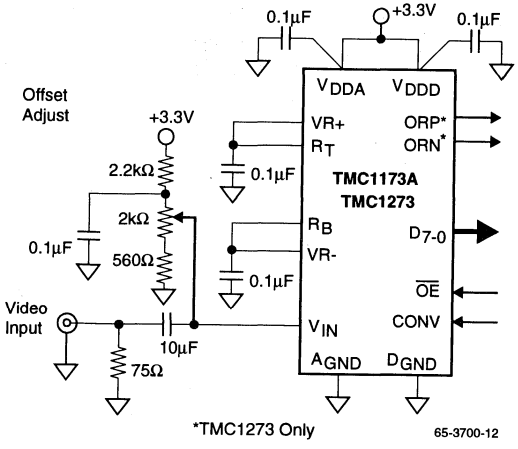


Figure 13. Low Cost Circuit

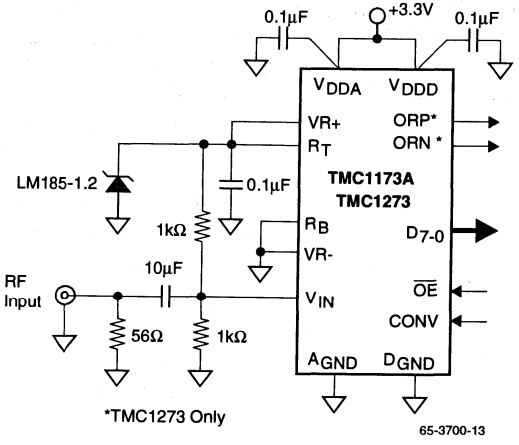


Figure 14. Stabilized Reference Circuit

Ordering Information

Product Number	Conversion Rate	Temperature Range	Screening	Package	Package Marking
TMC1173AM7C5	5 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1173AM7C5
TMC1173AM7C10	10 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1173AM7C10
TMC1173AM7C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1173AM7C20
TMC1173AN2C5	5 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1173AN2C5
TMC1173AN2C10	10 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1173AN2C10
TMC1173AN2C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1173AN2C20
TMC1173AR3C5	5 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1173AR3C5
TMC1173AR3C10	10 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1173AR3C10
TMC1173AR3C20	20 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1173AR3C20
TMC1273M7C5	5 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1273M7C5
TMC1273M7C10	10 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1273M7C10
TMC1273M7C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1273M7C20
TMC1273N2C5	5 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1273N2C5
TMC1273N2C10	10 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1273N2C10
TMC1273N2C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1273N2C20
TMC1273R3C5	5 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1273R3C5
TMC1273R3C10	10 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1273R3C10
TMC1273R3C20	20 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1273R3C20

TMC1175A/TMC1275

Video A/D Converter

8 bit, 40 Msps

Features

- 8-mit resolution
- 40 Msps conversion rate
- Low power: 100mW @ 20 Msps
- Integral track/hold
- Integral and differential linearity error 0.5 LSB
- Single +5V power supply
- Differential phase 0.5 degree
- Differential gain 1.5%
- Three-state TTL/CMOS-compatible outputs
- Low cost

Applications

- Video digitizing
- VGA and CCD digitizing
- LCD projection panels
- Image scanners
- Personal computer video boards
- Multimedia systems
- Low cost, high speed data conversion

Description

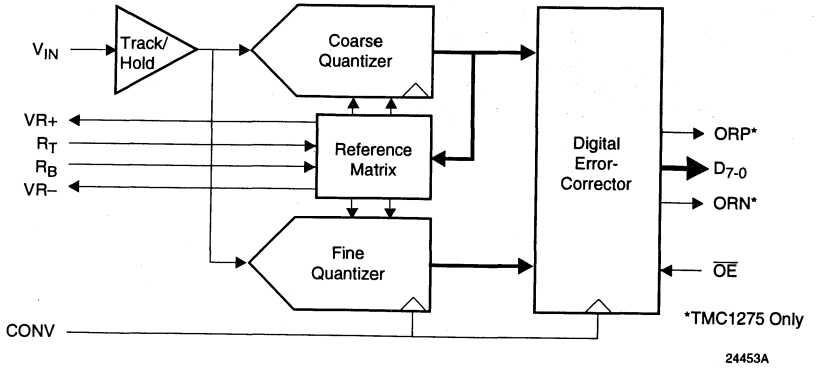
The TMC1175A/1275 analog-to-digital (A/D) converter employs a two-step architecture to convert analog signals into 8-bit digital words at sample rates of up to 40 Msps (Megasamples per second). An integral Track/Hold circuit delivers excellent performance on signals with full-scale frequency components up to 12 MHz. The innovative architecture and submicron CMOS technology limit typical power dissipation to 100 mW.

The TMC1175A/1275 operates from a single +5 Volt power supply and has internal voltage reference resistors for self-bias operation. Input capacitance is very low, simplifying or eliminating input driving amplifiers. All digital three-state outputs are TTL- and CMOS-compatible.

The TMC1175A and TMC1275 share their core architectures; the TMC1275 adds two overrange outputs that indicate when the analog input signal is beyond the conversion range.

The TMC1175A/1275 is available in 24-pin plastic DIP, 24-lead plastic SOIC, and 28-lead J-lead PLCC packages. Performance specifications are guaranteed from -20°C to 75°C.

Block Diagram



Functional Description

The TMC1175A/1275 8-bit A/D converter uses a two-step architecture to perform analog-to-digital conversion at rates up to 40 Msps. The input signal is held in an integral track/hold stage during the conversion process. Operation is pipelined, with one input sample taken and one output word provided for each CONVert cycle.

The first step in the conversion process is a coarse 4-bit quantization. This determines the range of the subsequent fine 4-bit quantization step. To eliminate spurious codes, the fine 4-bit A/D quantizer output is gray-coded and converted to binary before it is combined with the coarse result to form a complete 8-bit result.

Analog Input and Voltage References

The TMC1175A/1275 converts analog signals in the range R_B to R_T into digital data. Input signals outside that range produce "saturated" 00h or FFh output codes. The device will not be damaged by signals within the range AGND to V_{DDA}.

The A/D converter input range is very flexible and extends from the +5 Volt power supply to ground. The nominal input range is 2 Volts, from 0.6V to 2.6V. The circuit is characterized and performance is specified over that range. However, the part will work well with a full-scale range from 1.0V to 5.0V. A reduced input range may simplify analog signal conditioning circuitry, at the expense of additional noise sensitivity and some reduced differential linearity performance. Similarly, increasing the range can improve differential linearity, but puts a greater burden on the input signal conditioning circuitry.

In many applications, external voltage reference sources are connected to the R_T and R_B pins. R_B can be grounded. Gain and offset errors are directly related to the accuracy and stability of the applied reference voltages.

Two reference pull-up and pull-down resistors connected to VR+ and VR-, are provided internally for operation without external voltage reference circuitry (Figure 1). The reference voltages applied to R_T and R_B may be generated by connecting VR+ to R_T and VR- to R_B. The power supply voltage is divided by the on-chip resistors to bias the R_T and R_B points. This sets-up the converter for operation in its nominal range from 0.6V to 2.6V.

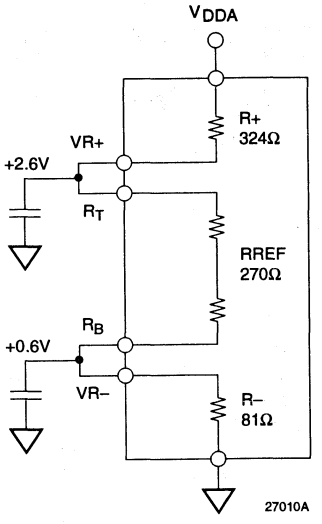


Figure 1. Reference Resistors

With V_{DDA} at 5.0V, connecting VR+ to R_T and grounding R_B will provide an input range from 0.0V to 2.27V, while connecting R_T to V_{DDA} and R_B to VR- produces a full scale range of 3.85V referenced to V_{DDA}. External resistors may also be employed to provide arbitrary reference voltages, but they will not match the temperature coefficient of the on-chip resistors as well as R+ and R-, and will cause the converter transfer function to vary with temperature.

With this implementation, errors in the power supply voltage end up on the conversion data output.

Because a two-step conversion process is employed, it is important that the references remain stable during the ENTIRE conversion process (two clock cycles). The reference voltage can then be changed, but any conversion in progress during a reference change is invalid.

Table 1. Output Coding

Input Voltage	ORP[2]	ORN[2]	Output
R_T + 1 LSB	1	0	FF
R_T	0	0	FF
R_T – 1 LSB	0	0	FE
• • •	• • •	• • •	• • •
R_B + 128 LSB	0	0	80
R_B + 127 LSB	0	0	7F
• • •	• • •	• • •	• • •
R_B + 1 LSB	0	0	01
R_B	0	0	00
R_B – 1 LSB	0	1	00

Notes:
1. LSB = (R_T – R_B) / 255
2. TMC1275 Only

Digital Inputs and Outputs

Sampling of the applied input signal takes place on the **falling** edge of the CONV signal (Figure 2). The output word is delayed by 2 1/2 CONV cycles. It is then available after the **rising** edge of CONV. The previous data on the output remain valid for t_{HO} (Output Hold Time), satisfying any hold time requirement of the receiving circuit. The new data become valid t_{DO} (Output Delay Time) after this rising edge of CONV.

Whenever the analog input signal is sampled and found to be at a level beyond the A/D conversion range, an Overrange output of the TMC1275 will go HIGH. If the input is more positive (by at least one LSB) than the positive end of the range, ORP will go HIGH and D_{7-0} will be FFh. If the input is more negative (by at least one LSB) than the negative end of the range, ORN will go HIGH and D_{7-0} will be 00h.

The outputs of the TMC1175A/1275 are CMOS- and TTL-compatible, and are capable of driving four low-power Schottky TTL (54/74LS) loads. An Output Enable control, $\overline{OE}$, places the outputs in a high-impedance state when HIGH. The outputs are enabled when $\overline{OE}$ is LOW.

Power and Ground

The TMC1175A/1275 operates from a single +5 Volt power supply. For optimum performance, it is recommended that A_{GND} and D_{GND} pins of the TMC1175A/1275 be connected to the system analog ground plane.

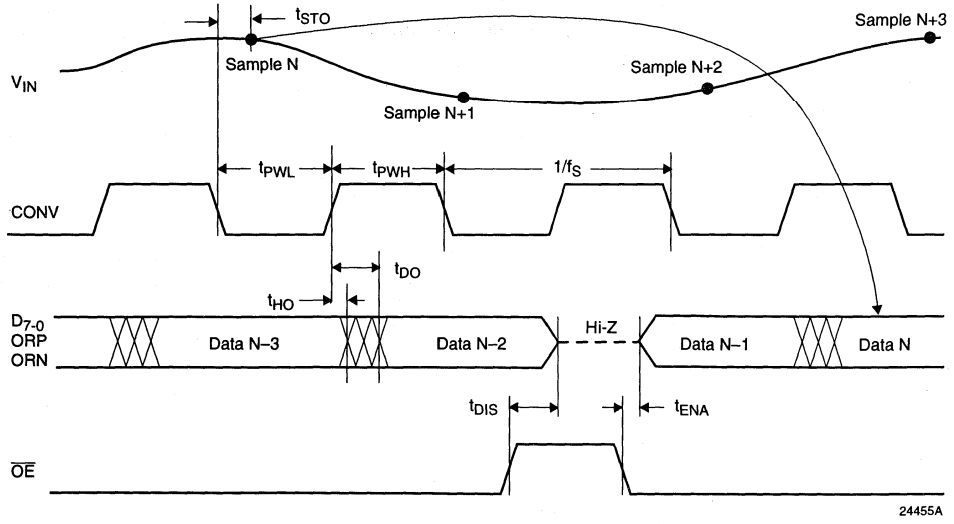


Figure 2. Conversion Timing

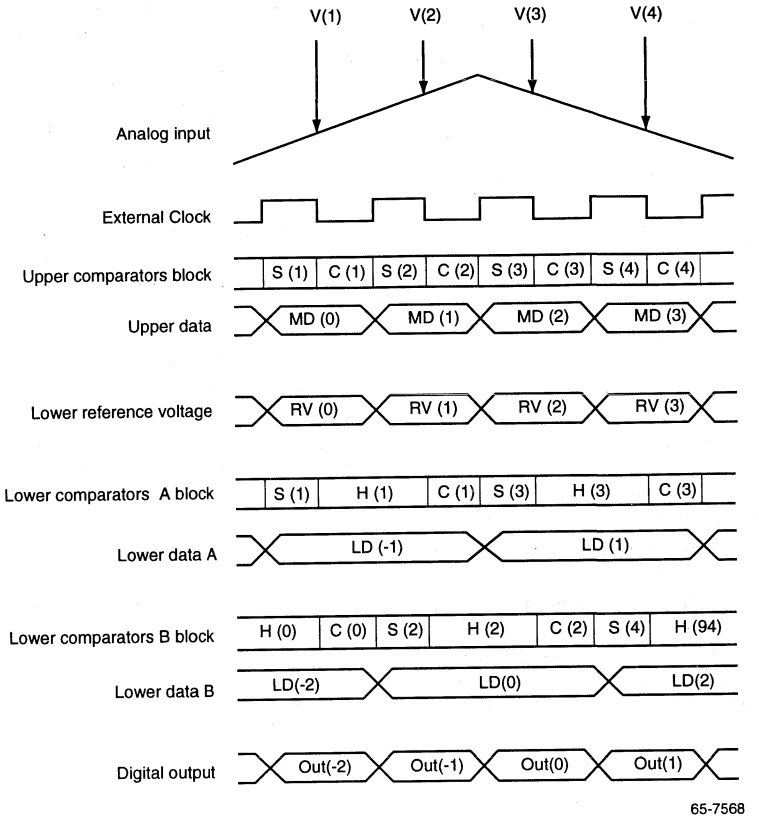
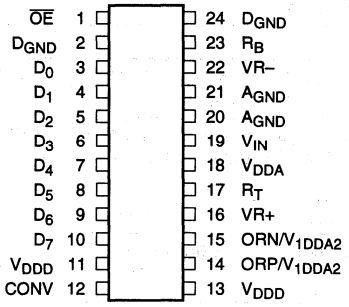
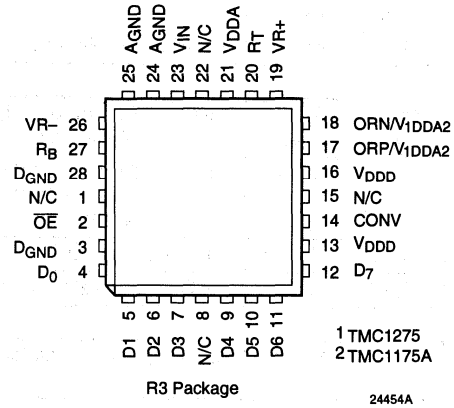


Figure 3. Internal Timing

Pin Assignments



N2 Package
M7 Package



R3 Package

1 TMC1275
2 TMC1175A

24454A

BROADCAST VIDEO

Pin Descriptions

Pin Name	Pin Number DIP	Pin Number PLCC	Pin Type	Pin Function Description
Inputs				
V_{IN}	19	23	$R_T - R_B$	**Analog Input.** The input voltage conversion range lies between the voltages applied to the RT and RB pins.
R_T	17	20	2.6V	**Reference Voltage Top Input.** R_T is the top input to the reference resistor ladder. A DC voltage applied to R_T defines the positive end of the V_{IN} conversion range.
R_B	23	27	0.6V	**Reference Voltage Bottom Input.** R_B is the bottom input to the reference resistor ladder. A DC voltage applied to R_B defines the negative end of the V_{IN} conversion range.
VR+	16	19		**Reference Voltage Top Source.** VR+ is the internal pull-up reference resistor for self-bias operations.
VR–	22	26		**Reference Voltage Bottom Source.** VR- is the internal pull-down reference resistor for self-bias operations.
$\overline{OE}$	1	2	CMOS	**Output Enable.** (CMOS-compatible) When LOW, D_{7-0} are enabled. When HIGH, D_{7-0} are in a high-impedance state.
CONV	12	14	CMOS	**Convert (Clock) Input.** (CMOS-compatible) V_{IN} is sampled on the falling edge of CONV.
Outputs				
D_{7-0}	10–3	12–9, 7–4	CMOS/ TTL	**Data Outputs (D7 = MSB).** Eight-bit CMOS- and TTL-compatible digital outputs. Data is output following the rising edge of CONV.
ORP[1]	14[1]	17[1]	CMOS/ TTL	**OverRange Positive Output.** When HIGH, ORP indicates that the analog input voltage is at least one LSB higher than the voltage that produces output code FFh. ORP is synchronous with D_{7-0}.
ORN[1]	15[1]	18[1]	CMOS/ TTL	**OverRange Negative Output.** When HIGH, ORN indicates that the analog input voltage is at least one LSB lower than the voltage that produces output code 00h. ORN is synchronous with D_{7-0}.

Pin Descriptions (continued)

Pin Name	Pin Number DIP	Pin Number PLCC	Pin Type	Pin Function Description
Power				
V_{DDA}	14[2], 15[2], 18	17[2], 18[2], 21	+5V	**Analog Supply Voltage.** These should originate from a common +5V source and be decoupled to AGND.
V_{DDD}	11, 13	13, 16	+5V	**Digital Supply Voltage.** +5 Volt power inputs. These should originate from a common +5V power source and be decoupled to AGND.
AGND	20, 21	24, 25	0.0V	**Analog Ground.** Connect to the system analog ground plane.
DGND	2, 24	3, 28	0.0V	**Digital Ground.** Connect to the system analog ground plane.
No Connect				
N/C		1, 8, 15, 22	open	Not Connected.

Notes:
1. TMC1275 Only.
2. TMC1175A Only.

Specification Notes

Bandwidth

The specification for bandwidth of an A/D converter is somewhat different from the normal frequency-response specification used in amplifiers and filters. An understanding of the differences will help in selecting converters properly for particular applications.

A/D conversion comprises two distinct processes: *sampling* and *quantizing*. *Sampling* is "grabbing" a snapshot of the input signal and holding it steady for quantizing. The *quantizing* process is approximating the analog input, which may be any value within the conversion range, with its nearest numerical value. While sampling is a high-frequency process, quantizing operates on a dc signal, held steady by the track/hold circuit. Therefore, the sampling process is what relates to the dynamic characteristics of the converter.

Sampling involves an *aperture time*, the time during which the track/hold is trying to capture the input signal and settle on a dc value to hold. It is analogous to the shutter speed of a camera: the shorter the aperture (or faster the shutter) the less the signal will be blurred, and the less uncertainty there will be in the quantized value.

For example, a 10 MHz sinewave with a 1V peak amplitude (2Vp-p) has a maximum slew rate of $2\pi fA$ at zero crossing, or 62.8V/µs. With an 8-bit A/D converter, q (the quantization step size) = 2V/255 = 7.8mV. The input signal will slew one LSB in 124ps. To limit the error (and noise) contribution due to *aperture effects* to 1/2LSB, the aperture must be shorter than 62ps.

This is the primary reason that the signal to noise ratio drops off as full scale frequency increases. Note, also, that the slew rate is directly proportional to signal amplitude, A. A/Ds will handle lower-amplitude signals of higher bandwidth.

All this is of particular interest in applications such as digitizing analog VGA RGB signals, or the output of a CCD imaging chip. These data are effectively pre-sampled: there is a period of rapid slewing from one pixel value to another, followed by a relatively stable dc level before the signal slews to the next pixel value. The goal is, of course, to sample on these pixel values, not on the slewing between pixels. During the aperture time, the A/D sees essentially a dc signal, and classic bandwidth considerations are not important. As long as the input circuit can slew and settle to the new value in the prescribed period, an accurate conversion will be made.

The TMC1175A/1275 is capable of slewing a full 2V and settling between samples taken as little as 25ns apart, making it ideal for digitizing analog VGA and CCD outputs.

Equivalent Circuits and Threshold Level

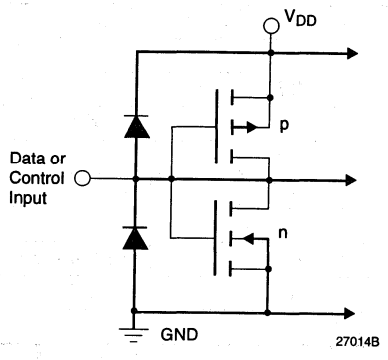


Figure 4. Equivalent Digital Input Circuit

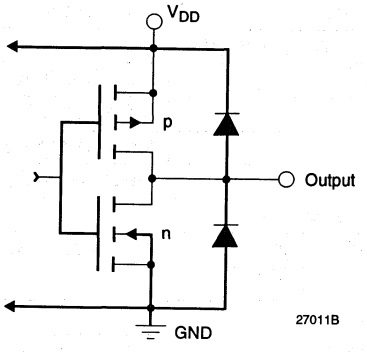


Figure 5. Equivalent Digital Output Circuit

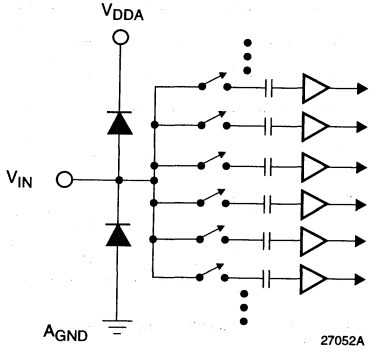


Figure 6. Equivalent Analog Input Circuit

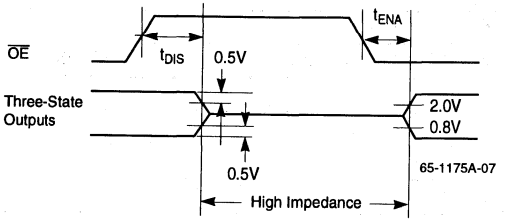


Figure 7. Threshold Levels for Three-State Measurements

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply Voltages					
V_{DDA}	Measured to A_{GND}	-0.5		7.0	V
V_{DDD}	Measured to D_{GND}	-0.5		7.0	V
V_{DDA}	Measured to V_{DDD}	-0.5		0.5	V
A_{GND}	Measured to D_{GND}	-0.5		0.5	V
Digital Inputs					
Applied Voltage[2]	Measured to D_{GND}	-0.5		V_{DDD} + 0.5	V
Forced Current[3,4]		-10.0		10.0	mA
Analog Inputs					
Applied Voltage[2]	Measured to A_{GND}	-0.5		V_{DDA} + 0.5	V
Forced Current[3,4]		-10.0		10.0	mA
Outputs					
Applied Voltage[2]	Measured to D_{GND}	-0.5		V_{DDD} + 0.5	V
Forced Current[3,4]		-6.0		6.0	mA
Short Circuit Duration	Single output in HIGH state to ground			1	sec
Temperature					
Operating, ambient		-20		110	°C
Junction				150	°C
Storage		-65		150	°C
Lead Soldering	10 seconds			300	°C
Vapor Phase Soldering	1 minute			220	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DDD}	Digital Power Supply Voltage		4.75	5.0	5.25	V
V_{DDA}	Analog Power Supply Voltage		4.75	5.0	5.25	V
A_{GND}	Analog Ground (Measured to D_{GND})		-0.1	0	0.1	V
f_S	Conversion Rate	TMC1175A/1275-20			20	Msps
		TMC1175A/1275-30			30	Msps
		TMC1175A/1275-40			40	Msps
t_{PWH}	CONV Pulsewidth, HIGH	TMC1175A/1275-20	15			ns
		TMC1175A/1275-30	13			ns
		TMC1175A/1275-40	12			ns

Operating Conditions (continued)

Parameter			Min	Nom	Max	Units
t_{PWL}	CONV Pulsewidth, LOW	TMC1175A/1275-20	15			ns
		TMC1175A/1275-30	12			ns
		TMC1175A/1275-40	12			ns
V_{RT}	Reference Voltage, Top		2.0	2.6	V_{DDA}	V
V_{RB}	Reference Voltage, Bottom		0	0.6	3.0	V
V_{RT}-V_{RB}	Reference Voltage Differential		1.0		5.0	V
V_{IN}	Analog Input Range		V_{RB}		V_{RT}	V
V_{IH}	Input Voltage, Logic HIGH		0.7 x V_{DDD}		V_{DDD}	V
V_{IL}	Input Voltage, Logic LOW		GND		0.3 x V_{DDD}	V
I_{OH}	Output Current, Logic HIGH				-4.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		-20		75	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Units
I_{DD}	Power Supply Current[1]	V_{DDD} = V_{DDA} = Max, C_{LOAD} = 35pF				
		f_S = 20Msps		20	30	mA
		f_S = 30Msps		25	35	mA
		f_S = 40Msps		30	40	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DDD} = V_{DDA} = Max				
		CONV = LOW		7	18	mA
		CONV = HIGH		10	20	mA
P_D	Total Power Dissipation	V_{DDD} = V_{DDA} = Max, C_{LOAD} = 35pF				
		f_S = 20Msps		100	160	mW
		f_S = 30Msps		125	185	mW
		f_S = 40Msps		150	210	mW
C_{AI}	Input Capacitance, Analog	CONV = LOW		4		pF
		CONV = HIGH		12		pF
R_{IN}	Input Resistance		500	1000		kΩ
I_{CB}	Input Current, Analog				±1	µA
R_{REF}	Reference Resistance		200	270	340	Ω
I_{IH}	Input Current, HIGH	V_{DDD} = Max, V_{IN} = V_{DDD}			±5	µA
I_{IL}	Input Current, LOW	V_{DDD} = Max, V_{IN} = 0V			±5	µA
I_{OZH}	Hi-Z Output Leakage	V_{DDD} = Max, V_{IN} = V_{DDD}			±5	µA
I_{OZL}	Hi-Z Output Leakage	V_{DDD} = Max, V_{IN} = 0V			±5	µA
I_{OS}	Short-Circuit Current				-30	mA

Electrical Characteristics (continued)

Parameter		Conditions	Min	Typ[1]	Max	Units
V_{OH}	Output Voltage, HIGH	I_{OH} = -100µA	V_{DDD}-0.3			V
		I_{OH} = -2.5mA	3.5			V
		I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max			0.4	V
C_{DI}	Digital Input Capacitance			4	10	pF
C_{DO}	Digital Output Capacitance			10		pF

Note:

1. Typical values with V_{DDD} = V_{DDA} = Nom and T_A = Nom, Minimum/Maximum values with V_{DDD} = V_{DDA} = Max and T_A = Min.

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{STO}	Sampling Time Offset		2	5	8	ns
t_{HO}	Output Hold Time	C_{LOAD} = 15pF	5			ns
t_{DO}	Output Delay Time	C_{LOAD} = 15pF			20	ns
t_{ENA}	Output Enable Time				27	ns
t_{DIS}	Output Disable Time				42	ns

System Performance Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Units
E_{LI}	Integral Linearity Error, Independent	V_{RT} - V_{RB} >= 2.0V		±0.5	±0.75	LSB
E_{LD}	Differential Linearity Error	V_{RT} - V_{RB} >= 2.0V		±0.3	±0.5	LSB
BW	Bandwidth[2]	TMC1175A/1275-20 TMC1175A/1275-30 TMC1175A/1275-40			10 12 12	MHz MHz MHz
E_{AP}	Aperture Error			30		ps
E_{OT}	Offset Voltage, Top	R_T – V_{IN} for most positive code transition	-8	-25	-42	mV
E_{OB}	Offset Voltage, Bottom	R_B – V_{IN} for most negative code transition	30	40	50	mV
dg	Differential Gain	f_S = 14.3Msps NTSC 40 IRE Mod Ramp V_{DDA} = +5.0V, T_A=25°C V_{RT} – V_{RB} = 2.0V		1.5	2.7	%
dp	Differential Phase	f_S = 14.3Msps NTSC 40 IRE Mod Ramp V_{DDA} = +5.0V, T_A=25°C V_{RT} – V_{RB} = 2.0V		0.5	1.0	deg

Notes:

1. Values shown in Typ column are typical for V_{DDD} = V_{DDA} = +5V and T_A = 25°C.
2. Bandwidth is the frequency up to which a full-scale sinewave can be digitized without spurious codes.

System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Units
SNR	Signal-to-Noise Ratio	f_S = 20Msps, V_{IN} = 2V p-p				
		f_{IN} = 1.24MHz	44	48		dB
		f_{IN} = 2.48MHz	43	47		dB
		f_{IN} = 6.98MHz	41	45		dB
		f_{IN} = 10.0MHz	37	42		dB
		f_S = 30Msps, V_{IN} = 2V p-p				
		f_{IN} = 1.24MHz	42	47		dB
		f_{IN} = 2.48MHz	40	45		dB
		f_{IN} = 6.98MHz	38	43		dB
		f_{IN} = 10.0MHz	33	39		dB
		f_{IN} = 12.0MHz	30	37		dB
		f_S = 40Msps, V_{IN} = 2V p-p				
		f_{IN} = 1.24MHz	40	45		dB
		f_{IN} = 2.48MHz	38	43		dB
		f_{IN} = 6.98MHz	36	41		dB
		f_{IN} = 10.0MHz	34	38		dB
		f_{IN} = 12.0MHz	32	36		dB
SFDR	Spurious-Free Dynamic Range	f_S = 20Msps, V_{IN} = 2V p-p				
		f_{IN} = 1.24MHz	46	52		dB
		f_{IN} = 2.48MHz	44	51		dB
		f_{IN} = 6.98MHz	41	45		dB
		f_{IN} = 10.0MHz	38	43		dB
		f_S = 30Msps, V_{IN} = 2V p-p				
		f_{IN} = 1.24MHz	42	49		dB
		f_{IN} = 2.48MHz	40	45		dB
		f_{IN} = 6.98MHz	37	41		dB
		f_{IN} = 10.0MHz	35	40		dB
		f_{IN} = 12.0MHz	34	39		dB
		f_S = 40Msps, V_{IN} = 2V p-p				
		f_{IN} = 1.24MHz	40	44		dB
		f_{IN} = 2.48MHz	39	43		dB
		f_{IN} = 6.98MHz	38	41		dB
		f_{IN} = 10.0MHz	36	40		dB
		f_{IN} = 12.0MHz	36	39		dB

Notes:

1. SNR values do not include the harmonics of the fundamental frequency.
2. SFDR is the ratio in dB of fundamental amplitude to the harmonic with the highest amplitude.
3. Values shown in Typ column are typical for V_{DDD} = V_{DDA} =+5V and T_A = 25°C.

Typical Performance Characteristics

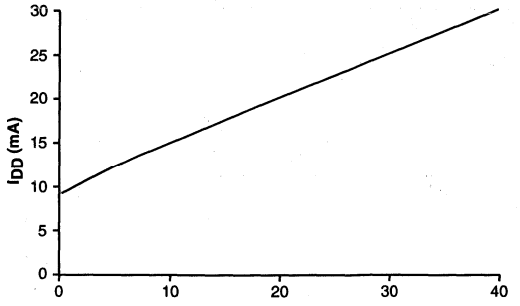


Figure 8. Typical I_{DD} vs f_S

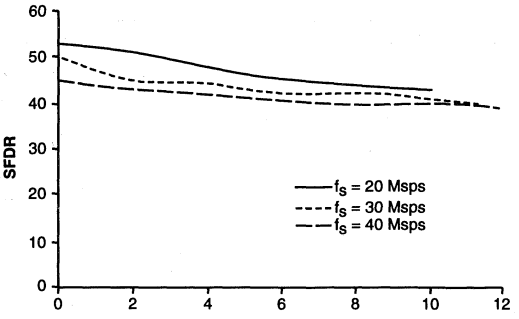


Figure 9. Typical SFDR vs f_{IN} and f_S

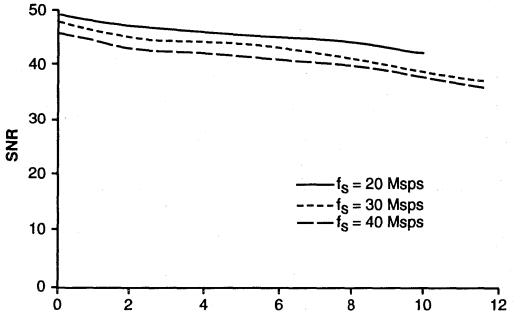


Figure 10. Typical SNR vs f_{IN} and f_S

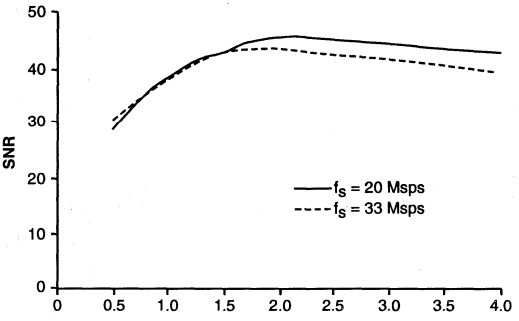


Figure 11. Typical SNR vs Full Scale Input Range

Applications Discussion

The circuit in Figure 12 employs a band-gap reference to generate a variable RT reference voltages for the TMC1175A/1275 as well as a bias voltage to offset the wideband input amplifier to mid-range. An "offset adjust" is also shown for varying the mid-range voltage level. The operational amplifier in the reference circuitry is a standard 741-type.

The voltage reference at R_T can be adjusted from 0.0 to 2.4 volts while R_B is grounded. Diodes are used to restrict the wideband amplifier output to between -0.7V and V_{DD} +0.7V. Diode protection is good practice to limit the analog input voltage at V_{IN} to the safe operating range.

The circuit in Figure 13 shows self-bias of R_T and R_B by connection to VR+ and VR-. This sets up a 0.6 to 2.6 Volt input range for V_{IN}. The input range is susceptible to power supply variation since the voltages on R_T and R_B are directly derived from V_{DDA}. The video input is AC-coupled and biased at a adjustable midpoint of the A/D input range. This circuit offers the advantage of minimum support circuitry for the most cost-sensitive applications.

In Figure 14, an external band-gap reference sets R_T to +1.2 Volts while R_B is grounded. The internal pull-up resistor, R+, provides the bias current for the band-gap reference. The A/D converter input is biased to the mid-point of the input range.

Grounding

The TMC1175A/1275 has separate analog and digital circuits. To keep digital system noise from the A/D converter, it is recommended that power supply voltages (V_{DDD} and V_{DDA}) come from the same source, and that ground connections (D_{GND} and A_{GND}) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin. The digital circuitry that gets its input from the TMC1175A/1275 should be referred to the system digital ground plane.

Printed Circuit Board Layout

Designing with high performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option, even for breadboarding. Overall system per-

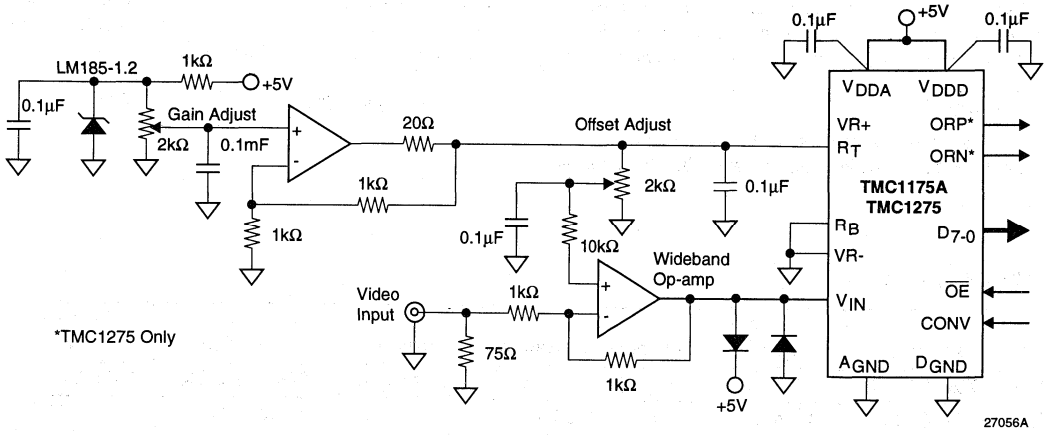


Figure 12. Typical Interface Circuit - High Performance

formance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{IN}, R_T, R_B, VR+, VR-) as short as possible and as far as possible from all digital signals. The TMC1175A/1275 should be located near the board edge, close to the analog input connectors.

2. The power plane for the TMC1175A/1275 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC1175A/1275 is the same as that of the system's digital circuitry, power to the TMC1175A/1275 should be decoupled with ferrite beads and 0.1µF capacitors to reduce noise.

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They supply different circuits on the integrated circuit, each of which generate varying amounts and types of noise. For best results, use 0.1µF ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not be placed under the TMC1175A/1275, the voltage reference, or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC1175A/1275 and its related analog circuitry can have an adverse effect on performance.

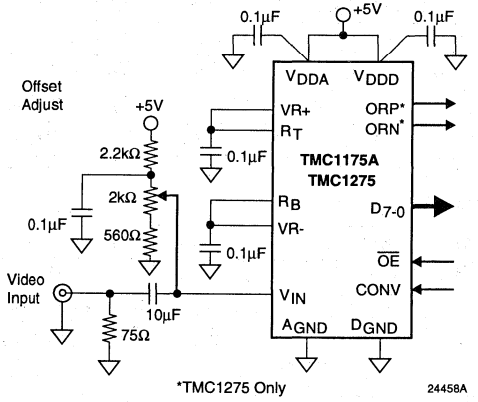


Figure 13. Typical Interface Circuit - Low Cost

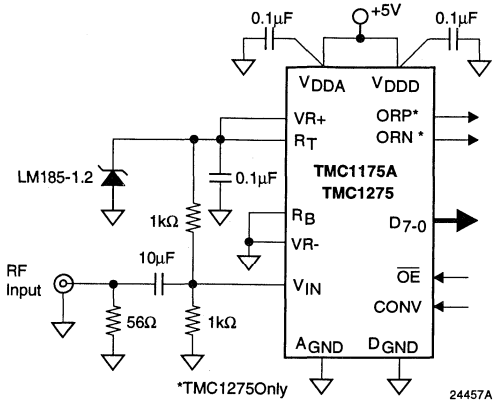


Figure 14. Typical Interface Circuit - Stabilized Reference

6. CONV should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Evaluation Board

An evaluation board is available that implements good interface practices and provide a convenient testbed for developing system applications and circuit variations. An on-board D/A converter is provided to reconstruct the digitized signal and to evaluate converter performance.

Contact your sales representative for information.

Ordering Information

Product Number	Conversion Rate	Temperature Range	Screening	Package	Package Marking
TMC1175AM7C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1175AM7C20
TMC1175AM7C30	30 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1175AM7C30
TMC1175AM7C40	40 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1175AM7C40
TMC1175AN2C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1175AN2C20
TMC1175AN2C30	30 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1175AN2C30
TMC1175AN2C40	40 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1175AN2C40
TMC1175AR3C20	20 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1175AR3C20
TMC1175AR3C30	30 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1175AR3C30
TMC1175AR3C40	40 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1175AR3C40
TMC1275M7C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1275M7C20
TMC1275M7C30	30 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1275M7C30
TMC1275M7C40	40 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1275M7C40
TMC1275N2C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1275N2C20
TMC1275N2C30	30 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1275N2C30
TMC1275N2C40	40 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1275N2C40
TMC1275R3C20	20 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1275R3C20
TMC1275R3C30	30 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1275R3C30
TMC1275R3C40	40 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1275R3C40

TMC1203

Triple Video A/D Converter

8-Bit, 50Msps

Features

- 8-bit resolution
- 50 Msps conversion rate
- Low power: 100mW per channel @ 20 Msps
- Integral track/hold
- Independent clock inputs
- Integral and differential linearity error 0.5 LSB
- Differential phase 0.7 degree
- Differential gain 1.8%
- Single +5V power supply
- Three-state TTL/CMOS-compatible outputs
- Low cost

Applications

- Video digitizing (composite and Y-C)
- VGA and CCD digitizing
- LCD projection panels
- Image scanners
- Personal computer video boards
- Multimedia systems
- Low cost, high speed data conversion
- Digital communications

Description

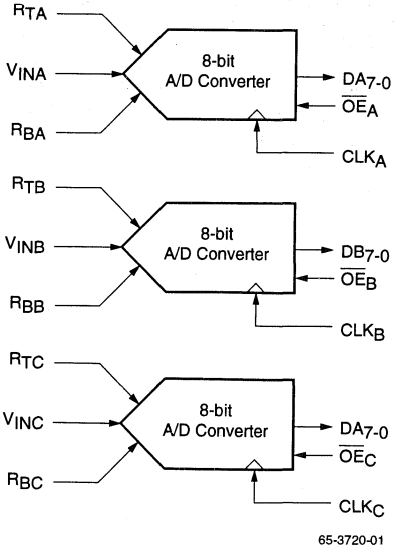
Incorporated into the TMC1203 are three analog-to-digital (A/D) converters, each with independent clocks and reference voltages. Analog signals are converted to Triple 8-bit digital words at sample rates up to 50 Msps (Megasamples per second) per channel.

Integral Track/Hold circuits deliver excellent performance on signals with full-scale spectral components up to 12 MHz. Innovative two-step architecture conversion architecture and submicron CMOS technology reduce typical power dissipation to 100 mW per converter.

Power is derived from a single +5 Volt power supply. Outputs are three-state outputs and TTL/CMOS-compatible.

TMC1203 package is a 80-lead Metric Quad Flat Pack (MQFP). Performance specifications are guaranteed from 0°C to 70°C.

Block Diagram



65-3720-01

Circuit Function

Within the TMC1203 are three 8-bit A/D converters, each employing two-step architecture to convert an analog input to a digital output at rates up to 50 Msps. Input signals are held in integral track/hold stages during the conversion process. Operation is pipelined, with one input sample taken and one output word provided for each CLK_X cycle.

Each of the three converters function identically. In the following descriptions 'X' refers to a generic input/output or clock where 'X' is equivalent to A, B or C.

The first step in the conversion process is a coarse 4-bit quantization. This determines the range of the subsequent fine 4-bit quantization step. To eliminate spurious codes, the fine 4-bit A/D quantizer output is gray-coded and converted to binary before it is combined with the coarse result to form a complete 8-bit result.

Analog Input and Voltage References

Each A/D accepts analog signals in the range R_{BX} to R_{TX} into digital data. Input signals outside this range produce "saturated" 00h or FFh output codes. The device will not be damaged by signals within the range A_{GND} to V_{DDA}.

Input range is very flexible and extends from the +5 Volt power supply to ground. Nominal input range is 2 Volts, extending from 0.6V to 2.6V. Characterization and performance is specified over this range. However, the part will function with a full-scale range from 1.0V to 5.0V. A smaller input range may simplify analog signal conditioning circuitry, at the expense of additional noise sensitivity and some reduced differential linearity performance.

External voltage reference sources are connected to the R_{TX} and R_{BX} pins. R_{BX} can be grounded. Within each A/D converter is a reference resistor ladder comprising 255 resistors that are accessed by the TMC1203 comparators. R_{TX} is connected to the top of the ladder, R_{BX} to the bottom. Gain and offset errors are directly related to the accuracy and stability of the applied reference voltages.

Because a two-step conversion process is employed, it is important that the references remain stable during the ENTIRE conversion process (two clock cycles). The reference voltage can then be changed, but any conversion in progress during a reference change is invalid.

Digital Inputs and Outputs

Sampling of the applied input signal occurs on the "falling" edge of the CLK_X signal (Figure 1). Output data is delayed by 2 1/2 CLK_X cycles and is valid following the "rising" edge of CLK_X. Previous output data remains valid for t_{HO} (Output Hold Time), satisfying any hold time requirement of the receiving circuit. New data becomes valid t_D (Output Delay Time) after this rising edge of CLK_X.

Whenever the analog input signal is sampled and found to be at a level beyond the A/D conversion range, the output limits at 00h or FFh, as appropriate.

Table 1. A/D Output Coding

Input Voltage	Output
R_{TX} + 1 LSB	FF
R_{TX}	FF
R_{TX} - 1 LSB	FE
• • •	• • •
R_{BX} + 128 LSB	80
R_{BX} + 127 LSB	7F
• • •	• • •
R_{BX} + 1 LSB	01
R_{BX}	00
R_{BX} - 1 LSB	00

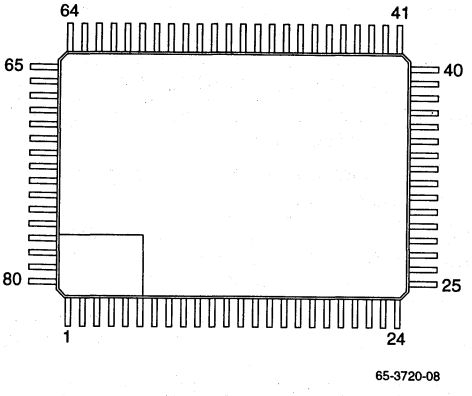
Note: 1 LSB = (R_{TX} - R_{BX}) / 255

The outputs of the TMC1203 are CMOS- and TTL-compatible, and are capable of driving four low-power Schottky TTL loads. An Output Enable control, $\overline{OE}_X$, places the A/D outputs in a high-impedance state when HIGH. The outputs are enabled when $\overline{OE}_X$ is LOW.

Power and Ground

The TMC1203 operates from a single +5 Volt power supply. For optimum performance, it is recommended that A_{GND} and D_{GND} pins of the TMC1203 be connected to the system analog ground plane.

Pin Assignments



65-3720-08

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	21	DGND	41	DC_7	61	V_{DD}
2	DA_5	22	DGND	42	$\overline{OE}_C$	62	$\overline{OE}_B$
3	DA_6	23	NC	43	V_{DD}	63	DB_7
4	DA_7	24	NC	44	V_{DD}	64	DB_6
5	$\overline{OE}_A$	25	DGND	45	CLK_C	65	DB_5
6	V_{DD}	26	DGND	46	NC	66	DB_4
7	V_{DD}	27	V_{DD}	47	V_{DDA}	67	DB_3
8	NC	28	V_{DD}	48	V_{INC}	68	DB_2
9	CLK_A	29	V_{DD}	49	AGND	69	DB_1
10	NC	30	V_{DD}	50	R_{TC}	70	DB_0
11	V_{DDA}	31	NC	51	R_{BC}	71	DGND
12	V_{INA}	32	DGND	52	R_{BB}	72	DGND
13	AGND	33	DGND	53	R_{TB}	73	NC
14	R_{TA}	34	DC_0	54	AGND	74	DGND
15	R_{BA}	35	DC_1	55	V_{INB}	75	DGND
16	DGND	36	DC_2	56	V_{DDA}	76	DA_0
17	DGND	37	DC_3	57	NC	77	DA_1
18	DGND	38	DC_4	58	CLK_B	78	DA_2
19	DGND	39	DC_5	59	NC	79	DA_3
20	DGND	40	DC_6	60	V_{DD}	80	DA_4

Pin Descriptions

Pin Name	Pin Number	Value	Pin Function Description
A/D Converters			
V_{INA}, V_{INB}, V_{INC}	12, 55, 48	R_{TX} to R_{BX}	**Analog Inputs.** The input voltage conversion range lies between the voltage applied to the R_{TX} and R_{BX} pins. R_{TX}, R_{BX}.
R_{TA}, R_{TB}, R_{TC}	14, 53, 50	2.6V	**Reference Voltage, Top Inputs.** DC voltages applied to R_{TA}, R_{TB} and R_{TC} define highest value of V_{INX}.
R_{BA}, R_{BB}, R_{BC}	15, 52, 51	0.6V	**Reference Voltage, Bottom Inputs.** DC voltages applied to R_{BA}, R_{BB} and R_{BC} define highest value of V_{INX}.
CLK_A, CLK_B, CLK_C	9, 58, 45	CMOS	**Convert (Clock) Inputs.** A/D converter clock inputs. CMOS-compatible. V_{INX} is sampled on the falling edge of CLK_X. Clock inputs are separate for the three converters.
DA_{7-0}	4, 3, 2, 80, 79, 78, 77, 76	CMOS/ TTL	**Data outputs, Converter A (D_7 = MSB).** Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLK_X.
DB_{7-0}	63, 64, 65, 66, 67, 68, 69, 70	CMOS/ TTL	**Data outputs, Converter B (D_7 = MSB).** Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLK_X.
DC_{7-0}	41, 40, 39, 38, 37, 36, 35, 34	CMOS/ TTL	**Data outputs, Converter C (D_7 = MSB).** Eight-bit CMOS- and TTL-compatible digital outputs. Valid data is output on the rising edge of CLK_X.
$\overline{OE_A}$, $\overline{OE_B}$, $\overline{OE_C}$	5, 62, 42	CMOS	**Output Enable Inputs.** CMOS-compatible. When LOW, the A/D output is enabled. When HIGH, the output is in a high-impedance state. Output Enables are separate for the three converters.
Power			
V_{DDA}	11, 47, 56	+5V	**Analog Supply Voltage.** +5 Volt power inputs. These should come from the same power source and be decoupled to A_{GND}.
V_{DD}	6, 7, 27, 28, 29, 30, 43, 44, 60, 61	+5V	**Digital Supply Voltage.** +5 Volt power inputs. These should come from the same power source and be decoupled to A_{GND}.
A_{GND}	13, 49, 54	0.0V	**Analog Ground.** Ground connections. These pins should be connected to the system analog ground plane.
D_{GND}	16, 17, 18, 19, 20, 21, 22, 25, 26, 32, 33, 71, 72, 74, 75	0.0V	**Digital Ground.** Ground connections. These pins should be connected to the system analog ground plane.
No Connect			
N/C	1, 8, 10, 23, 24, 31, 46, 57, 59, 73	open	**Not Connected.**

Specification Notes

Bandwidth

Bandwidth specification of an A/D converter is somewhat different from the normal frequency-response specification used in amplifiers and filters. An understanding of the differences will help in selecting converters properly for particular applications.

A/D conversion comprises two distinct processes: sampling and quantizing. Sampling is *grabbing* a snapshot of the input signal and holding it steady for quantizing. The quantizing process is approximating the analog input to its nearest numerical value within the conversion range. While sampling is a high-frequency process, quantizing operates on a dc signal, held steady by the track/hold circuit. Therefore, the sampling process relates to the dynamic characteristics of an A/D converter.

Sampling involves an aperture time, the time needed for the track/hold circuit to capture the input signal and settle on a dc value to hold. It is analogous to the shutter speed of a camera: the shorter the A/D aperture (or faster the shutter) the less the signal (or picture) will be blurred, and the less uncertainty there will be in the quantized value. This is not to be confused with the camera lens opening (aperture), which is entirely different.

For example, a 10 MHz sinewave with a 1V peak amplitude (2Vp-p) has a maximum slew rate of $2\pi fA$ at zero crossing, or 62.8V/ms. With an 8-bit A/D converter, q (the quantization step size) = 2V/255 = 7.8mV. The input signal will slew one LSB in 124ps. To limit the error (and noise) contribution due to aperture effects to 1/2LSB, the aperture must be shorter than 62ps.

This is the primary reason that the signal to noise ratio drops off as full scale frequency increases. Notice that the slew rate is directly proportional to signal amplitude, A. A/Ds will handle lower-amplitude signals of higher bandwidth, but other distortion effects will be worsened.

All this is of particular interest in applications such as digitizing analog VGA RGB signals, or the output of a CCD imaging chip. These data are effectively pre-sampled: there is a period of rapid slewing from one pixel value to another, followed by a relatively stable dc level before the signal slews to the next pixel value. The goal is, of course, to sample on these stable pixel values, not on the slewing between pixels. During the aperture time, the A/D sees essentially a dc signal, and bandwidth considerations are less important. As long as the input circuit can slew and settle to the new value in the prescribed period, an accurate conversion will be made.

The TMC1203 is capable of slewing a full 2V and settling between samples taken as little as 25ns apart, making it ideal for digitizing analog VGA and CCD outputs.

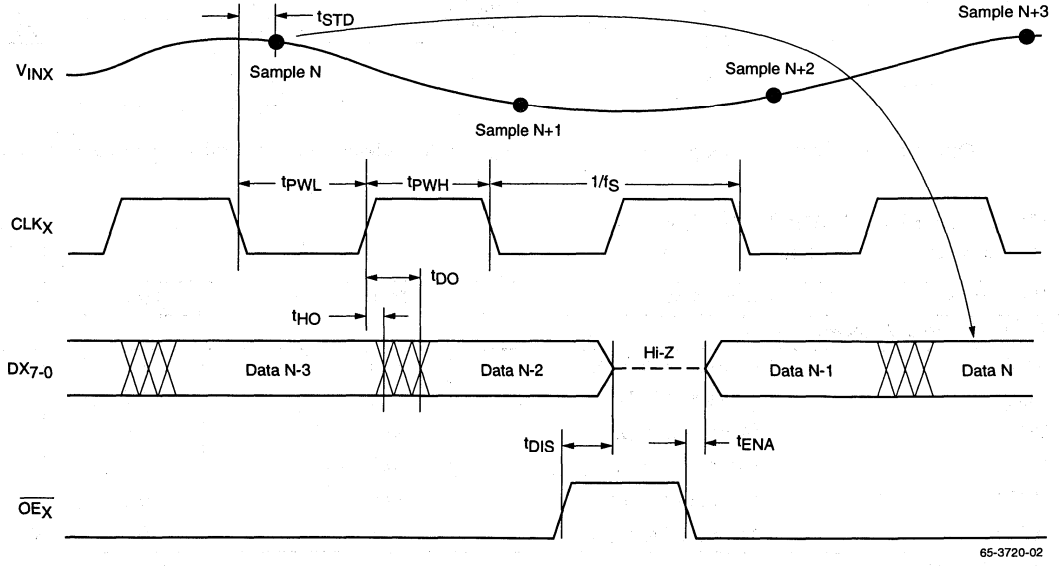


Figure 1. Timing

Equivalent Circuits

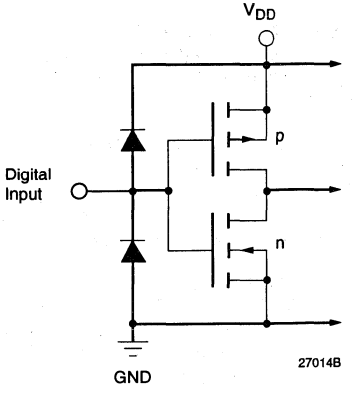


Figure 2. Equivalent Digital Input Circuit

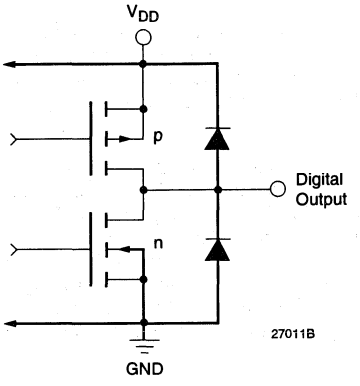


Figure 3. Equivalent Digital Output Circuit

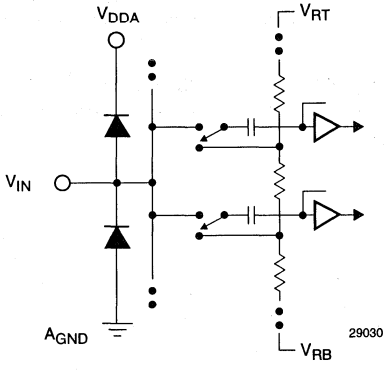


Figure 4. Equivalent Analog Input Circuit

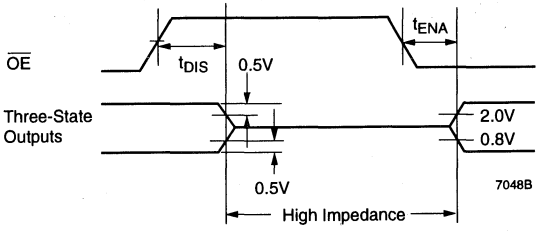


Figure 5. Threshold Levels for Three-State Measurements

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Condition	Min	Typ	Max	Unit
Power Supply Voltages					
VDDA	Measured to AGND	-0.5		+7.0	V
VDDP	Measured to DGND	-0.5		+7.0	V
VDD	Measured to DGND	-0.5		+7.0	V
VDDA	Measured to VDD	-0.5		+0.5	V
VDDP	Measured to VDD	-0.5		+0.5	V
AGND	Measured to DGND	-0.5		+0.5	V
Digital Inputs					
Applied Voltage	Measured to DGND[2]	-0.5		VDD + 0.5	V
Forced current [3, 4]		-10.0		+10.0	mA

Absolute Maximum Ratings (continued)

(beyond which the device may be damaged)[1]

Parameter	Condition	Min	Typ	Max	Unit
Analog Inputs					
Applied Voltage	Measured to A_{GND}[2]	-0.5		V_{DDA}+0.5	V
Forced current [3, 4]		-10.0		+10.0	mA
Digital Outputs					
Applied voltage	Measured to D_{GND2}	-0.5		V_{DD} + 0.5	V
Forced current [3, 4]		-6.0		+6.0	mA
Short circuit duration	Single output in HIGH state to ground)			1 second	
Temperature					
Operating, ambient		-20		110	°C
Junction				+150	°C
Lead, soldering	10 seconds			+300	°C
Vapor Phase soldering	1 minute			+220	°C
Storage		-65		+150	°C
Electrostatic Discharge[5]				±150	V

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

Parameter		Min.	Nom	Max.	Units
V_{DD}, V_{DDA}, V_{DDP}	Power Supply Voltage	4.75	5.0	5.25	V
A_{GND}	Analog Ground (Measured to D_{GND})	-0.1	0	0.1	V
V_{RTX}	Reference Voltage, Top		2.6	V_{DDA}	V
V_{RBX}	Reference Voltage, Bottom	0	0.6		V
V_{RTX}-V_{RBX}	Reference Voltage Differential	1.0	2.0	5.0	V
V_{INX}	Analog Input Range	V_{RB}		V_{RT}	V
V_{IH}	Input Voltage, Logic HIGH	0.7 V_{DD}		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW	GND		0.3 V_{DD}	V
I_{OH}	Output Current, Logic HIGH			-4.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Min.	Typ[1]	Max.	Units
I_{DD}	Power Supply Current[1]	$V_{DD} = V_{DDA} = V_{DDP}$ = Max., C_{LOAD} = 35pF, $f_{CK} = f_S$ (3 A/Ds)				
		f_S = 20 Msps		60	90	mA
		f_S = 40 Msps		85	120	mA
		f_S = 50 Msps		98	135	mA
I_{DDQ}	Power Supply Current, Quiescent	$V_{DD} = V_{DDA}$ = Max.				
		CLK_X = LOW		24	45	mA
		CLK_X = HIGH		36	55	mA
PD	Total Power Dissipation	$V_{DD} = V_{DDA} = V_{DDP}$ = Max., C_{LOAD} = 35pF, $f_{CK} = f_S$ (3 A/Ds)				
		f_S = 20 Msps		300	470	mW
		f_S = 40 Msps		425	630	mW
		f_S = 50 Msps		490	710	mW
C_{AI}	Input Capacitance, Analog	CLK_X = LOW		4		pF
		CLK_X = HIGH		12		pF
R_{IN}	Input Resistance		500			kΩ
R_{REF}	Reference Resistance		200	270	340	Ω
I_{CB}	Input Current, Analog				±1	µA
I_{IH}	Input Current, HIGH	V_{DD} = Max., $V_{IN} = V_{DD}$			±5	µA
I_{IL}	Input Current, LOW	V_{DD} = Max., V_{IN} = 0V			±5	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max., $V_{IN} = V_{DD}$			±5	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max., $V_{IN} = V_{DD}$			±5	µA
I_{OS}	Short-Circuit Current				-35	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = -100mA	V_{DD}-0.3			V
		I_{OH} = -2.5mA	3.5			V
		I_{OH} = Max.	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max.			0.4	V
C_{DI}	Digital Input Capacitance			4	10	pF
C_{DO}	Digital Output Capacitance			10		pF

Note:

1. Typical values with $V_{DD} = V_{DDA}$ = Nom and T_A = Nom, Minimum/Maximum values with $V_{DD} = V_{DDA}$ = Max. and T_A = Min..

Preliminary Information

Switching Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
f_S	Conversion Rate	TMC1203-20			20	Msps
		TMC1203-40			40	Msps
		TMC1203-50			50	Msps
t_{PWH}	CLKX Pulsewidth, HIGH	TMC1203-20	14			ns
		TMC1203-40	14			ns
		TMC1203-50	3			ns
t_{PWL}	CLKX Pulsewidth, LOW	TMC1203-20	8			ns
		TMC1203-40	8			ns
		TMC1203-50	7			ns
E_{AP}	Aperture Error			30		ps
t_{STO}	Sampling Time Offset		1	2	5	ns
t_{STS}	Sampling Time Skew			150	400	ps
t_{HO}	Output Hold Time	CLOAD = 15pF	9			ns
t_{DO}	Output Delay Time				14	ns
t_{ENA}	Output Enable Time				27	ns
t_{DIS}	Output Disable Time				42	ns

System Performance Characteristics

Parameter		Conditions	Min.[2]	Typ[1]	Max.[2]	Units
E_{LI}	Integral Linearity Error, Independent	V_{RT} = 2.6V		±0.5		LSB
E_{LD}	Differential Linearity Error	V_{RB} = 0.6V		±0.5		LSB
BW	Bandwidth[1]	TMC1203-20			10	MHz
		TMC1203-30			12	MHz
		TMC1203-40			12	MHz
		TMC1203-50			12	MHz
E_{OT}	Offset Voltage, Top (R_T - V_{IN} for most positive code transition)	V_{RT} = 2.6V, V_{RB} = 0.6V	-40		80	mV
E_{OB}	Offset Voltage, Bottom (R_B - V_{IN} for most negative code transition)	V_{RT} = 2.6V, V_{RB} = 0.6V	-95		-30	mV
dg	Differential Gain	f_S = 14.3Msps NTSC 40 IRE Mod Ramp V_{DDA} = +5.0V, T_A=25°C V_{RT} = 2.6V, V_{RB} = 0.6V		1.8		%
dp	Differential Phase	f_S = 14.3Msps NTSC 40 IRE Mod Ramp V_{DDA} = +5.0V, T_A=25°C V_{RT} = 2.6V, V_{RB} = 0.6V		0.7		deg
XTALK	Channel Crosstalk	f_N = 5.0 MHz		45		dB

System Performance Characteristics (continued)

Parameter		Conditions	Min.[2]	Typ[1]	Max.[2]	Units
SNR[3]	Signal-to-Noise Ratio	f_S = 20Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_N = 1.24MHz		46		dB
		f_N = 2.48MHz		46		dB
		f_N = 6.98MHz		45		dB
		f_N = 10.0MHz		45		dB
		f_S = 40Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_N = 1.24MHz		42		dB
		f_N = 6.98MHz		41		dB
		f_N = 12.0MHz		40		dB
		f_N = 20.0MHz		38		dB
		f_S = 50Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_N = 1.24MHz		40		dB
		f_N = 6.98MHz		40		dB
		f_N = 12.0MHz		40		dB
SFDR[4]	Spurious-Free Dynamic Range	f_S = 20Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_N = 1.24MHz		53		dB
		f_N = 2.48MHz		48		dB
		f_N = 6.98MHz		44		dB
		f_N = 10.0MHz		40		dB
		f_S = 40Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_N = 1.24MHz		49		dB
		f_N = 6.98MHz		44		dB
		f_N = 12.0MHz		38		dB
		f_S = 50Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_N = 1.24MHz		46		dB
		f_N = 6.98MHz		40		dB
		f_N = 12.0MHz		37		dB

Notes:

1. Values shown in Typ. column are typical for V_{DD} = V_{DDA} =+5V and T_A = 25°C.
2. Values shown in Min. and Max. columns are for V_{DD} = V_{DDA} and T_A over entire range specified under Operating Conditions.
3. SNR values do not include the harmonics of the fundamental frequency.
4. SFDR is the ratio in dB of fundamental amplitude to the harmonic with the highest amplitude.
5. Characteristics specified for V_{RT} = 2.6V, V_{RB} = 0.6V.
6. Bandwidth is the frequency up to which a full-scale sinewave can be digitized without spurious codes.

Typical Performance Characteristics

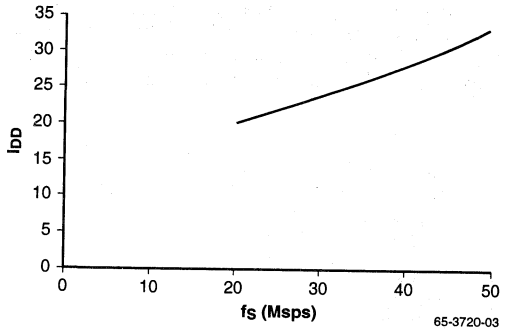


Figure 6. Typical I_{DD} vs f_S (Single A/D)

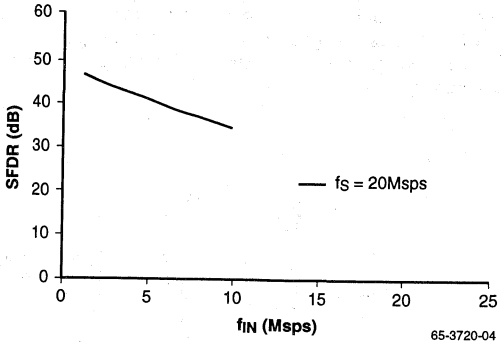


Figure 7. Typical SFDR vs f_{IN}

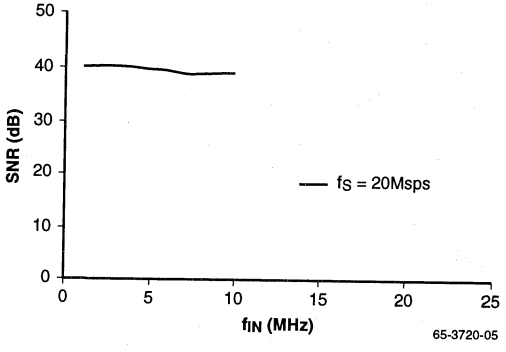


Figure 8. Typical SNR vs f_{IN}

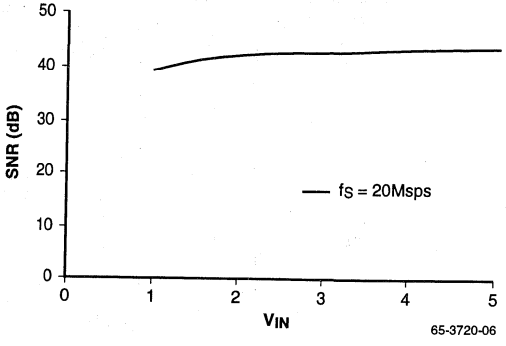


Figure 9. Typical SNR vs Full Scale Input Range

Application Notes

The circuit in Figure 10 employs a band-gap reference to generate a variable R_{TX} reference voltages for the TMC1203 as well as a bias voltage to offset the wideband input amplifiers to mid-range. The operational amplifier in the reference circuitry is a standard 741-type.

The voltage reference at R_{TX} can be adjusted from 0.0 to 2.4 volts while R_{BX} is grounded. Schottky diodes are used to restrict the wideband amplifier output to between -0.3V and V_{DD} +0.3V. Diode protection is good practice to limit the analog input voltage at V_{INX} to the safe operating range.

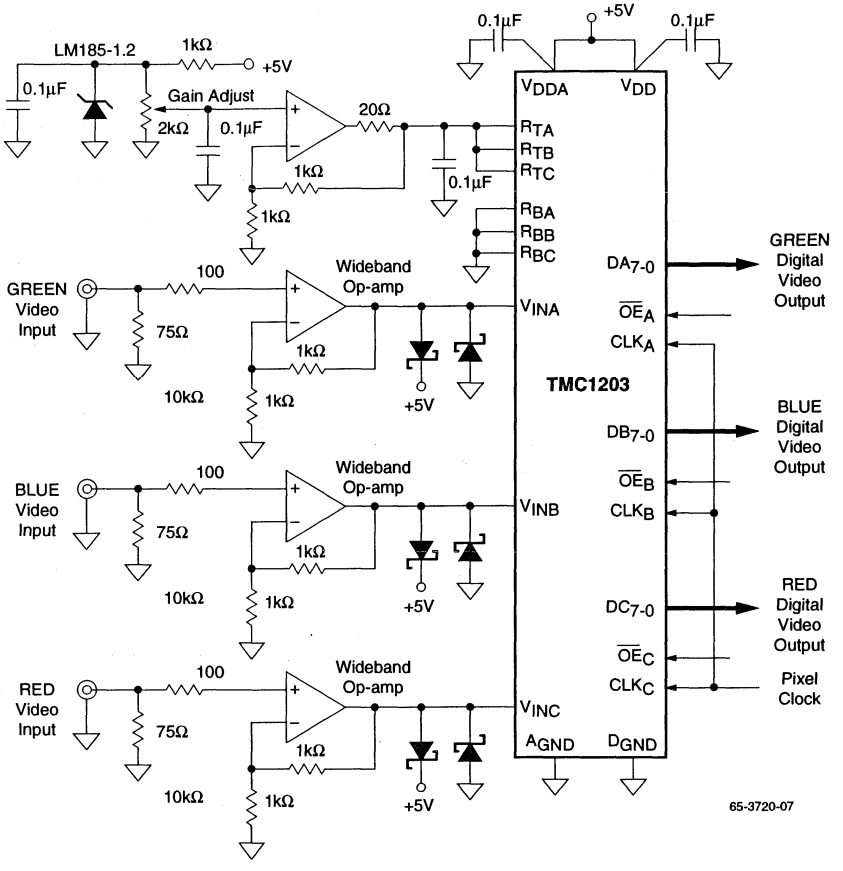


Figure 10. Typical Interface Circuit - High Performance

Grounding

The TMC1203 has separate analog and digital circuits. To keep digital system noise from the A/D converter, it is recommended that power supply voltages (V_{DD} and V_{DDA}) come from the same source, and that ground connections (D_{GND} and A_{GND}) be made to the analog ground plane, and as close as possible to the device pins. Power supply pins should be individually decoupled at the pin. The digital circuitry that gets its input from the TMC1203 should be referred to the system digital ground plane.

Printed Circuit Board Layout

Designing with high performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_N, R_{TX}, R_{BX}) as short as possible and as far as possible from all digital signals. The TMC1203 should be located close to the analog input connectors.

2. The power plane for the TMC1203 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC1203 is the same as that of the system's digital circuitry, power to the TMC1203 should be decoupled with ferrite beads and 0.1µF capacitors to reduce noise.

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They supply different circuits on the integrated circuit, each of which generate varying amounts and types of noise. For best results, use 0.1µF ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not be placed under the TMC1203, the voltage reference, or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC1203 and its related analog circuitry can have an adverse effect on performance.

6. CLK$_X$ should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line, if needed, to eliminate overshoot and ringing.

Related Products

- TMC1175A, TMC1275 8-Bit Video A/D Converters
- TMC1173A, TMC1273 3V, Low-Power 8-Bit Video A/D Converters
- TMC1103 Triple 8-bit A/D with Clamps and PLL
- TMC3003/TMC3503 Triple Video D/A Converters
- TMC2242B/TMC2243/TMC2246A Digital Filters

Ordering Information

Product Number	Conversion Rate (Msps)	Temperature Range	Screening	Package	Package Marking
TMC1203KLC20	20 Msps	T_A = 0°C to 70°C	Commercial	80-Lead MQFP	1203KLC20
TMC1203KLC40	40 Msps	T_A = 0°C to 70°C	Commercial	80-Lead MQFP	1203KLC40
TMC1203KLC50	50 Msps	T_A = 0°C to 70°C	Commercial	80-Lead MQFP	1203KLC50

TMC3003

Triple Video D/A Converter

10 bit, 80 Msps

Features

- 10-bit resolution
- 80, 50, and 30 megapixels per second
- Sync and blank controls
- Sync on green D/A output
- 1.0V p-p video into 37.5Ω or 75Ω load
- Enhancement of ADV7122
  - Internal bandgap voltage reference
  - Double-buffered data for low distortion
- TTL-compatible inputs
- Low glitch energy
- Single +5 Volt power supply

Applications

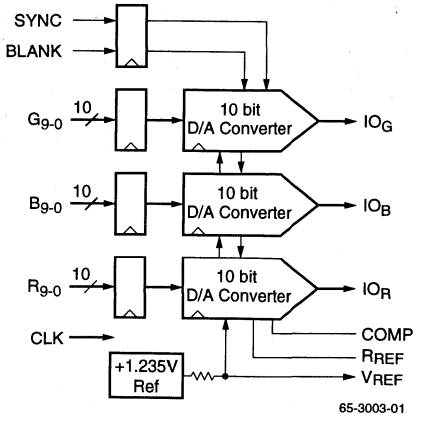
- Video signal conversion
  - RGB
  - YC_BC_R
  - Composite, Y, C
- Multimedia systems
- Image processing
- True-color graphics systems (1 billion colors)
- Broadcast television equipment
- High-Definition Television (HDTV) equipment
- Direct digital synthesis

Description

The TMC3003 is a high-speed triple 10-bit D/A converter especially suited for video and graphics applications. It offers 10-bit resolution, TTL-compatible inputs, low power consumption, and requires only a single +5 Volt power supply. It has single-ended current outputs, $\overline{SYNC}$ and $\overline{BLANK}$ control inputs, and a separate current source for adding sync pulses to the Green D/A converter output. It is ideal for generating analog RGB from digital RGB and driving computer display and video monitors. Three speed grades are available: 30, 50, and 80 Msps.

The TMC3003 triple D/A converter is available in a 44-lead plastic J-leaded PLCC. It is fabricated on a sub-micron CMOS process with performance guaranteed from 0°C to 70°C.

Block Diagram



Functional Description

The TMC3003 is a low-cost triple 10-bit CMOS D/A converter designed to directly drive computer CRT displays and video transmission lines at pixel rates of up to 80 Msps. It comprises three identical 10-bit D/A converters with registered data inputs, common clock, and internal voltage reference. An independent current source allows sync to be added to the green D/A converter output.

Digital Inputs

All digital inputs are TTL-compatible. Data are registered on the rising edge of the CLK signal. The analog output changes t_{DO} after the rising edge of CLK. There is one stage of pipeline delay on the chip. The guaranteed clock rates of the TMC3003 are 80, 50, and 30 MHz.

$\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$

$\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs control the output level (Figure 1 and Table 1) of the D/A converters during CRT retrace intervals. $\overline{\text{BLANK}}$ forces the D/A outputs to the blanking level while $\overline{\text{SYNC}}$ turns off a separate current source which is connected to the green D/A converter. This connection adds a 40 IRE sync pulse to the D/A output and brings that D/A output to 0.0 Volts during the sync tip. $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ are registered on the rising edge of CLK.

$\overline{\text{BLANK}}$ gates the D/A inputs and sets the pedestal voltage. If $\overline{\text{BLANK}}$ = HIGH, the D/A inputs are added to a pedestal which offsets the current output. If $\overline{\text{BLANK}}$ = LOW, data inputs and the pedestal are disabled.

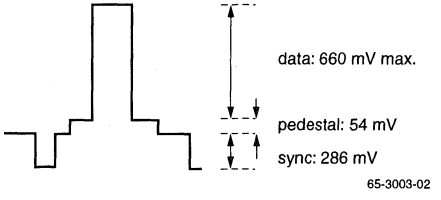


Figure 1. Nominal Output Levels

D/A Outputs

Each D/A output is a current source. To obtain a voltage output a resistor must be connected to ground. Output voltage of the D/A converters depends upon this resistor, the reference voltage, and the value of the gain-setting resistor connected between R_{REF} and GND.

Normally, a source termination resistor of 75 Ohms is connected between the D/A current output pin and GND near the D/A converter. A 75 Ohm coaxial cable may then be connected with another 75 Ohm termination resistor at the far end of the cable. This "double termination" presents the D/A converter with a net resistive load of 37.5 Ohms.

The TMC3003 may also be operated with a single 75 Ohm terminating resistor. To lower the output voltage swing to the desired range, the value of the resistor on R_{REF} should be increased.

Voltage Reference

The TMC3003 has an internal bandgap voltage reference of +1.235 Volts. An external voltage reference may be connected to the V_{REF} pin, overriding the internal voltage reference. All three D/A converters are driven from the same reference.

A 0.1µF capacitor must be connected between the COMP pin and V_{DD} to stabilize internal bias circuitry and ensure low-noise operation.

Power and Ground

The TMC3003 D/A converter requires a single +5.0 Volt power supply. The analog (V_{DD}) power supply voltage should be decoupled to GND to reduce power supply induced noise. 0.1µF decoupling capacitors should be placed as close as possible to the power pins.

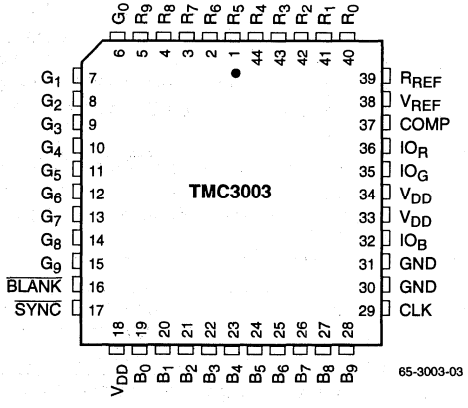
The high slew-rate of digital data makes capacitive coupling to the outputs of any D/A converter a potential problem. Since the digital signals contain high-frequency components of the CLK signal, as well as the video output signal, the resulting data feedthrough often looks like harmonic distortion or reduced signal-to-noise performance. All ground pins should be connected to a common solid ground plane for best performance.

Table 1. Output Voltage versus Input Code, $\overline{SYNC}$, and $\overline{BLANK}$

V_{REF} = 1.235 V, R_{REF} = 590 Ω, R_L = 37.5 Ω

RGB9-0 (MSB...LSB)	Red and Blue D/As			Green D/A		
	$\overline{SYNC}$	$\overline{BLANK}$	VOUT	$\overline{SYNC}$	$\overline{BLANK}$	VOUT
11 1111 1111	X	1	0.7140	1	1	1.0000
11 1111 1110	X	1	0.7134	1	1	0.9994
11 1111 1101	X	1	0.7127	1	1	0.9987
•	•	•	•	•	•	•
•	•	•	•	•	•	•
10 0000 0000	X	1	0.3843	1	1	0.6703
01 1111 1111	X	1	0.3837	1	1	0.6697
•	•	•	•	•	•	•
•	•	•	•	•	•	•
00 0000 0010	X	1	0.0553	1	1	0.3413
00 0000 0001	X	1	0.0546	1	1	0.3406
00 0000 0000	X	1	0.0540	1	1	0.3400
xx xxxx xxxx	X	0	0.0000	1	0	0.2860
xx xxxx xxxx	X	0	0.0000	0	0	0.0000

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Value	Description
Clock and Pixel I/O			
CLK	29	TTL	**Clock.** The clock input is TTL-compatible and all pixel data is registered on the rising edge of CLK. It is recommended that CLK be driven by a dedicated TTL buffer to avoid reflection induced jitter, overshoot, and undershoot.
R_{9-0}	5, 4, 3, 2, 1, 44, 43, 42, 41, 40	TTL	**Red pixel data inputs.** The Red digital input is TTL-compatible and registered on the rising edge of CLK.
G_{9-0}	15, 14, 13, 12, 11, 10, 9, 8, 7, 6	TTL	**Green pixel data inputs.** The Green digital input is TTL-compatible and registered on the rising edge of CLK.
B_{9-0}	28, 27, 26, 25, 24, 23, 22, 21, 20, 19	TTL	**Blue pixel data inputs.** The Blue digital input is TTL-compatible and registered on the rising edge of CLK.
Controls			
$\overline{SYNC}$	17	TTL	**Sync pulse Input.** Bringing $\overline{SYNC}$ LOW, turns off a 40 IRE (7.62 mA) current source which forms a sync pulse on the Green D/A converter output. $\overline{SYNC}$ is registered on the rising edge of CLK along with pixel data and has the same pipeline latency as $\overline{BLANK}$ and pixel data. $\overline{SYNC}$ does not override any other data and should be used only during the blanking interval. Since this is a single-supply D/A and all signals are positive-going, sync is added to the bottom of the Green D/A range. So turning SYNC OFF means turning the current source ON. When a sync pulse is desired, the current source is turned OFF. If the system does not require sync pulses from the Green D/A converter, $\overline{SYNC}$ should be connected to GND.
$\overline{BLANK}$	16	TTL	**Blanking Input.** When $\overline{BLANK}$ is LOW, pixel inputs are ignored and the D/A converter outputs are driven to the blanking level. $\overline{BLANK}$ is registered on the rising edge of CLK and has the same pipeline latency as $\overline{SYNC}$.
Video Outputs			
IO_R	36	0.714 Vp-p	**Red D/A output.** The current source outputs of the D/A converters are capable of driving RS-343A/SMPTE-170M compatible levels into doubly-terminated 75 Ohm lines.
IO_G	35	1 V p-p	**Green D/A output.** The current source outputs of the D/A converters are capable of driving RS-343A/SMPTE-170M compatible levels into doubly-terminated 75 Ohm lines. Sync pulses may be added to the Green D/A output.
IO_B	32	0.714 Vp-p	**Blue D/A output.** The current source outputs of the D/A converters are capable of driving RS-343A/SMPTE-170M compatible levels into doubly-terminated 75 Ohm lines.
Voltage Reference			
V_{REF}	38	+1.235 V	**Voltage Reference output/input.** An internal voltage source of +1.235 Volts is output on this pin. An external +1.235 Volt reference may be applied here which overrides the internal reference. Decoupling V_{REF} to GND with a 0.1µF ceramic capacitor is required.

Pin Descriptions (continued)

Pin Name	Pin Number	Value	Description
R_{REF}	39	560 Ω	**Current-setting resistor.** The full-scale output current of each D/A converter is determined by the value of the resistor connected between R_{REF} and GND. The nominal value for R_{REF} is found from: $R_{REF} = 9.1(V_{REF}/I_{FS})$ where I_{FS} is the full-scale (white) output current (in amps) from the D/A converter (without sync). Sync is 0.4 * I_{FS}. D/A full-scale (white) current may also be calculated from: $I_{FS} = V_{FS}/ R_L$ Where V_{FS} is the white voltage level and R_L is the total resistive load (in ohms) on each D/A converter. V_{FS} is the blank to full-scale voltage.
COMP	37	0.1 µF	**Compensation capacitor.** A 0.1 µF ceramic capacitor must be connected between COMP and V_{DD} to stabilize internal bias circuitry.
Power and Ground			
V_{DD}	18, 33, 34	+5 V	Power supply
GND	30, 31	0.0 V	Ground

Equivalent Circuits

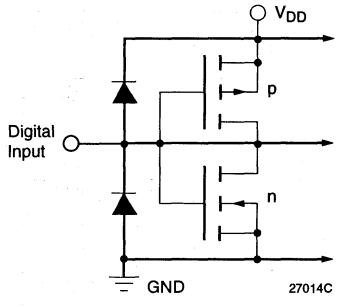


Figure 2. Equivalent Digital Input Circuit

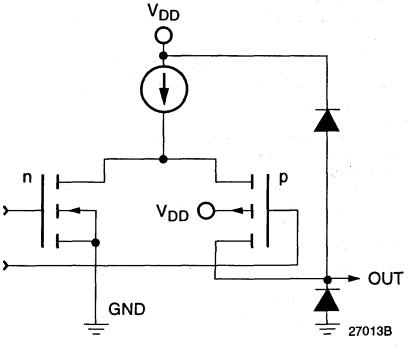


Figure 3. Equivalent Analog Output Circuit

Equivalent Circuits (continued)

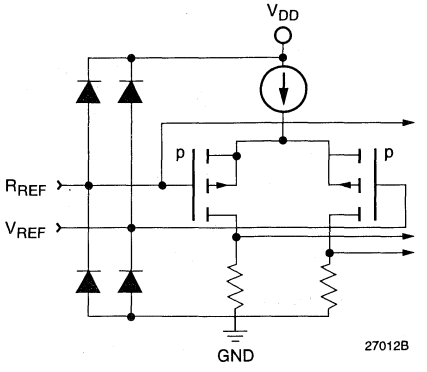


Figure 4. Equivalent Analog Input Circuit

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltage				
V_{DD} (Measured to GND)	-0.5		7.0	V
Inputs				
Applied Voltage (measured to GND)[2]	-0.5		V_{DD} + 0.5	V
Forced Current[3,4]	-10.0		10.0	mA
Outputs				
Applied Voltage (measured to GND)[2]	-0.5		V_{DD} + 0.5	V
Forced Current[3,4]	-60.0		60.0	mA
Short Circuit Duration (single output in HIGH state to ground)			infinite	second
Temperature				
Operating, Ambient	-20		110	°C
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C
Storage	-65		150	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_S	Conversion Rate	TMC3003-30			30	Msps
		TMC3003-50			50	Msps
		TMC3003-80			80	Msps
t_{PWH}	CLK Pulsewidth, HIGH		4			ns
t_{PWL}	CLK Pulsewidth, LOW		4			ns
t_s	Input Data Setup Time		3			ns
t_h	Input Date Hold Time		2			ns
V_{REF}	Reference Voltage, External		1.0	1.235	1.5	V
C_C	Compensation Capacitor			0.1		µF
R_L	Output Load			37.5		Ω
V_{IH}	Input Voltage, Logic HIGH		2.0		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW		GND		0.8	V
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Units
I_{DD}	Power Supply Current[2]	V_{DD} = Max				
		TMC3003-30			100	mA
		TMC3003-50			100	
		TMC3003-80			125	
PD	Total Power Dissipation[2]	V_{DD} = Max				
		TMC3003-30			525	mW
		TMC3003-50			525	
		TMC3003-80			655	
R_O	Output Resistance			100		kΩ
C_O	Output Capacitance	I_{OUT} = 0mA			30	pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = 2.4V			-1	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0.4V			1	µA
I_{REF}	V_{REF} Input Bias Current			0	±100	µA
V_{REF}	Reference Voltage Output			1.235		V
V_{OC}	Output Compliance	Referred to V_{DD}	-0.4	0	+1.5	V
C_{DI}	Digital Input Capacitance			4	10	pF

Notes:

1. Values shown in Typ column are typical for V_{DD} = +5V and T_A = 25°C.
2. Minimum/Maximum values with V_{DD} = Max and T_A = Min.

Switching Characteristics

Parameter		Conditions[2]	Min	Typ[1]	Max	Units
t_D	Clock to Output Delay	V_{DD} = Min		10	15	ns
t_{SKEW}	Output Skew			1	2	ns
t_R	Output Risetime	10% to 90% of Full Scale		2	3	ns
t_F	Output Falltime	90% to 10% of Full Scale		2	3	ns
t_{SET}	Output Settling Time	to 3%/FS		15		ns

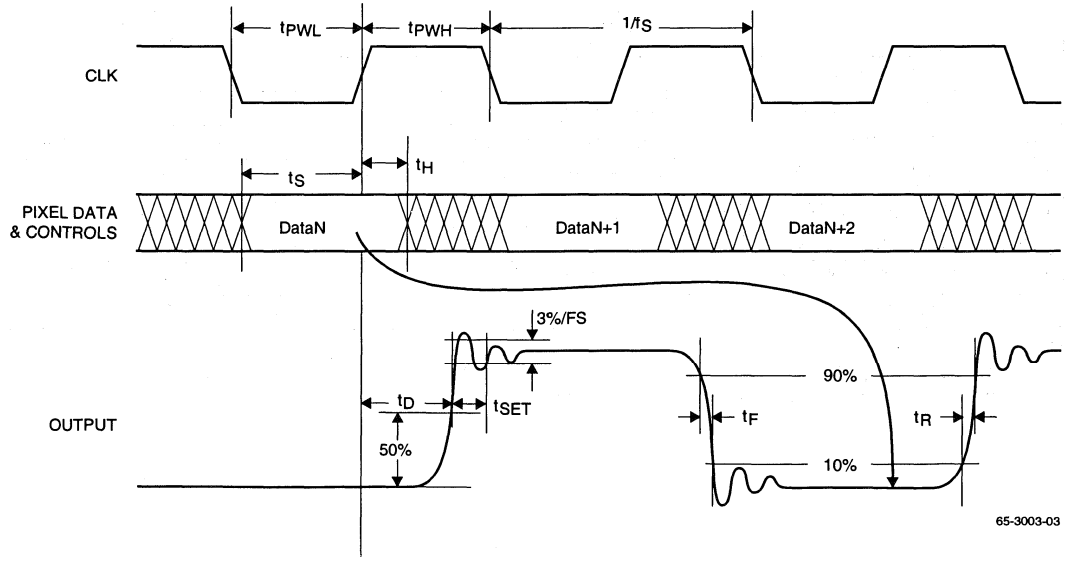
Notes:
1. Values shown in Typ column are typical for V_{DD} = +5V and T_A = 25°C.
2. V_{REF} = 1.235V, R_{LOAD} = 37.5Ω, R_{REF} = 590Ω.

System Performance Characteristics

Parameter		Conditions[2]	Min	Typ[1]	Max	Units
E_{LI}	Integral Linearity Error	V_{DD}, V_{REF} = Nom		±0.1	±0.25	%/FS
E_{LD}	Differential Linearity Error	V_{DD}, V_{REF} = Nom		±0.1	±0.25	%/FS
E_{DM}	DAC to DAC Matching	V_{DD}, V_{REF} = Nom		3	10	%
E_G	Absolute Gain Error	V_{DD}, V_{REF} = Nom			TBD	%/FS
TC_E	Gain Error Tempco	V_{DD}, V_{REF} = Nom		TBD		PPM/°C
V_{OF}	Output Offset Current	V_{DD} = Max, R, G, B = 000h			20	mA
PSR	Power Supply Rejection				0.05	%/%

Notes:
1. Values shown in Typ column are typical for V_{DD} = +5V and T_A = 25°C.
2. V_{REF} = 1.235V, R_{LOAD} = 37.5Ω, R_{REF} = 590Ω.

Timing Diagram



Applications Discussion

Figure 4 illustrates a typical TMC3003 interface circuit. In this example, an optional 1.2 Volt bandgap reference is connected to the V_{REF} output, overriding the internal voltage reference source.

Grounding

It is important that the TMC3003 power supply is well-regulated and free of high-frequency noise. Careful power supply decoupling will ensure the highest quality video signals at the output of the circuit. The TMC3003 has separate analog and digital circuits. To keep digital system noise from the D/A converter, it is recommended that power supply voltages (V_{DD}) come from the system analog power source and all ground connections (GND) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor D/A conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{REF}, I_{REF}, COMP, IO_R, IO_G, IO_B) as short as possible and as far as possible from all digital signals. The TMC3003 should be located near the board edge, close to the analog output connectors.

2. The power plane for the TMC3003 should be separate from that which supplies the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC3003 is the same as that of the system's digital circuitry, power to the TMC3003 should be decoupled with 0.1µF and 0.01µF capacitors and isolated with a ferrite bead.

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. If the digital power supply has a dedicated power plane layer, it should not be placed under the TMC3003, the voltage reference, or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the TMC3003 and its related analog circuitry can have an adverse effect on performance.

5. CLK should be handled carefully. Jitter and noise on this clock will degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

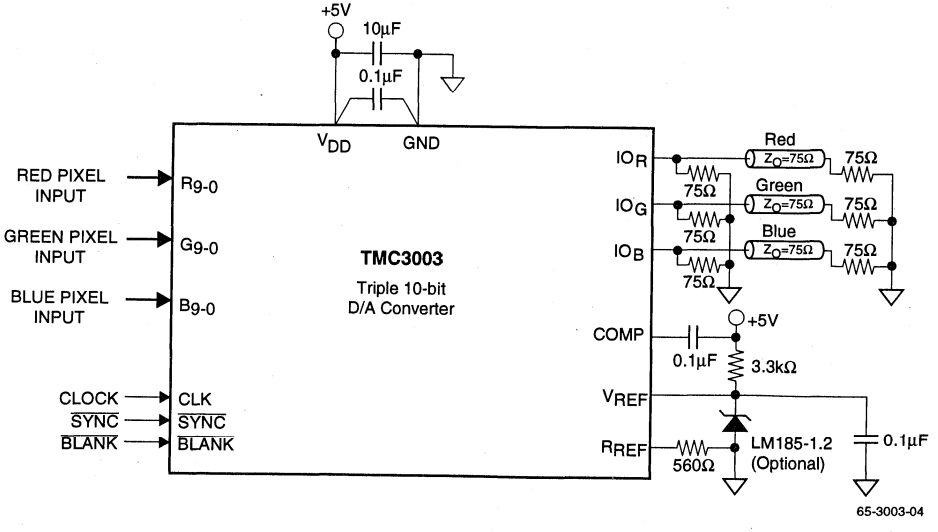


Figure 4. Typical Interface Circuit

Related Products

- TMC3503 Triple 8-bit 80 Msps D/A Converters
- TMC1175A 40 Msps CMOS 8-bit A/D Converter
- TMC1275 40 Msps CMOS 8-bit A/D Converter
- TMC22091, TMC22191 Digital Video Encoders
- TMC2242A/TMC2243/TMC2246A Video Filters
- TMC2249A Digital Mixer
- TMC2250A Matrix Multiplier
- TMC2272A Colorspace Converter
- TMC2302 Image Manipulation Sequencer
- TMC2340A Digital Synthesizer
- TMC2081 Digital Video Mixer

Ordering Information

Product Number	Conversion Rate (Msps)	Temperature Range	Screening	Package	Package Marking
TMC3003R2C30	30 Msps	T_A = 0°C to 70°C	Commercial	44-Lead PLCC	3003R2C30
TMC3003R2C50	50 Msps	T_A = 0°C to 70°C	Commercial	44-Lead PLCC	3003R2C50
TMC3003R2C80	80 Msps	T_A = 0°C to 70°C	Commercial	44-Lead PLCC	3003R2C80

TMC3503

Triple Video D/A Converter

8 bit, 80 Msps

Features

- 8-bit resolution
- 80, 50, and 30 megapixels per second
- ±0.5 LSB linearity error
- Sync, blank, and white controls
- Independent sync current output
- 1.0V p-p video into 37.5Ω or 75Ω load
- Enhancemenet of ADV7120
  - Internal bandgap voltage reference
  - Double-buffered data for low distortion
  - Power-down sleep mode
- Double-buffered data for low distortion
- TTL-compatible inputs
- Low glitch energy
- Single +5 Volt power supply

Applications

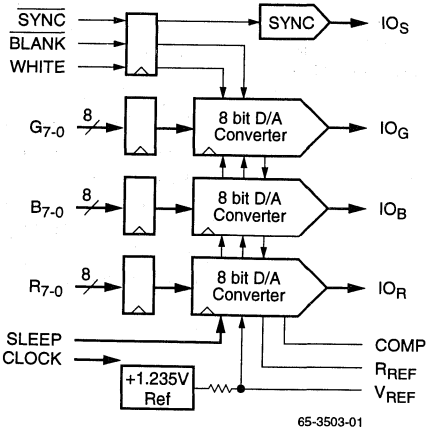
- Video signal conversion
  - RGB
  - YC_BC_R
  - Composite, Y, C
- Multimedia systems
- Image processing
- True-color graphics systems
- Broadcast television equipment
- High-Definition Television (HDTV) equipment
- Direct digital synthesis

Description

The TMC3503 is a high-speed triple 8-bit D/A converter especially suited for video and graphics applications. It offers 8-bit resolution, TTL-compatible inputs, low power consumption, a power-down sleep mode, and requires only a single +5 Volt power supply. It has single-ended current outputs, $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, WHITE, and SLEEP control inputs, and a separate current source for adding sync pulses to any D/A converter output. It is ideal for generating analog RGB from digital RGB and driving computer display and video monitors. Three speed grades are available: 30, 50, and 80 Msps.

The TMC3503 triple D/A converter is available in a 44-lead plastic J-leaded PLCC. It is fabricated on a sub-micron CMOS process with performance guaranteed from 0°C to 70°C.

Block Diagram



Functional Description

The TMC3503 is a low-cost triple 8-bit CMOS D/A converter designed to directly drive computer CRT displays at pixel rates up to 80 Msps. It comprises three identical 8-bit D/A converters with registered data inputs, common clock, and internal voltage reference. An independent current source allows sync to be added to any D/A converter output.

Digital Inputs

All digital inputs are TTL-compatible. Data are registered on the rising edge of the CLK signal. The analog output changes t_{DO} after the rising edge of CLK. There is one stage of pipeline delay on the chip. The guaranteed clock rates of the TMC3503 are 80, 50, and 30 MHz.

$\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$

$\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs control the output level (Figure 1 and Table 1) of the D/A converters during CRT retrace intervals. $\overline{\text{BLANK}}$ forces the D/A outputs to the blanking level while $\overline{\text{SYNC}}$ turns off a separate current source which is brought off the chip through the IO_S pin.

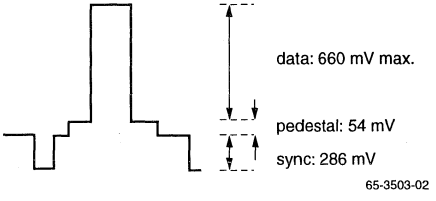


Figure 1. Nominal Output Levels

IO_S may be connected to any one D/A output, or used independently. It is commonly tied to the green D/A converter for "Sync on Green" operation. This connection adds a 40 IRE sync pulse to the D/A output and brings that D/A output to 0.0 Volts during the sync tip. $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ are registered on the rising edge of CLK.

$\overline{\text{BLANK}}$ gates the D/A inputs and sets the pedestal voltage. If $\overline{\text{BLANK}}$ = HIGH, the D/A inputs are added to a pedestal which offsets the current output. If $\overline{\text{BLANK}}$ = LOW, data inputs and the pedestal are disabled.

WHITE

The WHITE control drives all three D/As to full-scale, overriding the data inputs. It is overridden by the $\overline{\text{BLANK}}$ input, and is independent of $\overline{\text{SYNC}}$.

SLEEP

The SLEEP control, when HIGH, places the TMC3503 in a power-down state. This function operates asynchronously.

D/A Outputs

Each D/A output is a current source. To obtain a voltage output, a resistor must be connected to ground. Output voltage depends upon this external resistor, the reference voltage, and the value of the gain-setting resistor connected between R_{REF} and GND.

Normally, a source termination resistor of 75 Ohms is connected between the D/A current output pin and GND near the D/A converter. A 75 Ohm coaxial cable may then be connected with another 75 Ohm termination resistor at the far end of the cable. This "double termination" presents the D/A converter with a net resistive load of 37.5 Ohms.

The TMC3503 may also be operated with a single 75 Ohm terminating resistor. To lower the output voltage swing to the desired range, the value of the resistor on R_{REF} should be increased.

Voltage Reference

The TMC3503 has an internal bandgap voltage reference of +1.235 Volts. An external voltage reference may be connected to the V_{REF} pin, overriding the internal voltage reference. All three D/A converters are driven from the same reference.

A 0.1µF capacitor must be connected between the COMP pin and V_{DD} to stabilize internal bias circuitry and ensure low-noise operation.

Power and Ground

The TMC3503 D/A converter requires a single +5.0 Volt power supply. The analog (V_{DD}) power supply voltage should be decoupled to GND to reduce power supply induced noise. 0.1µF decoupling capacitors should be placed as close as possible to the power pins.

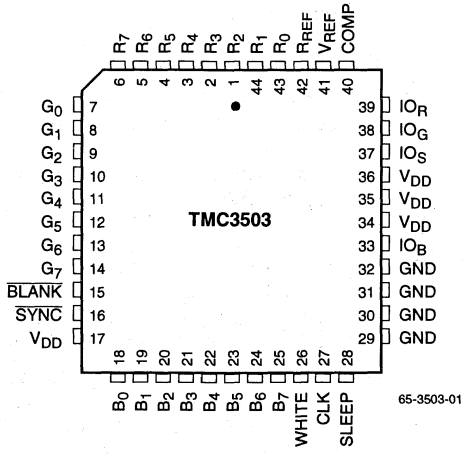
The high slew-rate of digital data makes capacitive coupling to the outputs of any D/A converter a potential problem. Since the digital signals contain high-frequency components of the CLK signal, as well as the video output signal, the resulting data feedthrough often looks like harmonic distortion or reduced signal-to-noise performance. All ground pins should be connected to a common solid ground plane for best performance.

Table 1. Output Voltage versus Input Code, $\overline{SYNC}$, $\overline{BLANK}$, and WHITE

V_{REF} = 1.235 V, R_{REF} = 590 Ω, R_L = 37.5 Ω

RGB7-0 (MSB...LSB)	All D/As				D/A with IOS Connected			
	$\overline{SYNC}$	$\overline{BLANK}$	WHITE	V_{OUT}	$\overline{SYNC}$	$\overline{BLANK}$	WHITE	V_{OUT}
XXXX XXXX	X	1	1	0.714	1	1	1	1.000
1111 1111	X	1	0	0.714	1	1	0	1.000
1111 1110	X	1	0	0.711	1	1	0	0.997
1111 1101	X	1	0	0.709	1	1	0	0.995
• •	• •	• •	• •	• •	• •	• •	• •	• •
0000 0000	X	1	0	0.385	1	1	0	0.671
1111 1111	X	1	0	0.383	1	1	0	0.669
• •	• •	• •	• •	• •	• •	• •	• •	• •
0000 0010	X	1	0	0.059	1	1	0	0.345
0000 0001	X	1	0	0.057	1	1	0	0.343
0000 0000	X	1	0	0.054	1	1	0	0.340
XXXX XXXX	X	0	X	0.000	1	0	X	0.286
XXXX XXXX	X	0	X	0.000	0	0	X	0.000

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Value	Pin Function Description
Clock and Pixel I/O			
CLK	27	TTL	**Clock Input.** The clock input is TTL-compatible and all pixel data is registered on the rising edge of CLK. It is recommended that CLK be driven by a dedicated TTL buffer to avoid reflection induced jitter, overshoot, and undershoot.
R_{7-0} G_{7-0} B_{7-0}	6-1, 44-43 14-7 25-18	TTL	**Red, Green, and Blue Pixel Inputs.** The R, G, and B digital inputs are TTL-compatible and registered on the rising edge of CLK.
Controls			
$\overline{SYNC}$	16	TTL	**Sync Pulse Input.** Bringing $\overline{SYNC}$ LOW, turns off a 40 IRE (7.62 mA) current source which forms a sync pulse on any D/A converter output connected to IO_S. $\overline{SYNC}$ is registered on the rising edge of CLK along with pixel data and has the same pipeline latency as $\overline{BLANK}$ and pixel data. $\overline{SYNC}$ does not override any other data and should be used only during the blanking interval. If the system does not require sync pulses, $\overline{SYNC}$ and IO_S should be connected to GND.
$\overline{BLANK}$	15	TTL	**Blanking Input.** When $\overline{BLANK}$ is LOW, pixel inputs are ignored and the D/A converter outputs are driven to the blanking level. $\overline{BLANK}$ is registered on the rising edge of CLK and has the same two-pipe latency as $\overline{SYNC}$ and Data.
WHITE	26	TTL	**Force Full Scale Input.** When WHITE is HIGH, pixel inputs are ignored and the D/A converter outputs are driven to their full-scale output level. A $\overline{BLANK}$ input overwrites a WHITE input. WHITE is register on the rising edge of CLK and has the same two-pipe latency as $\overline{SYNC}$ and Data.
SLEEP	28	TTL	**Power-down Control Input.** When HIGH, SLEEP places the D/A converter in a low-power-dissipation mode. The D/A current sources and the digital processing are disabled. The last data loaded into the input and D/A registers is retained. This control is asynchronous.
Video Outputs			
IO_R IO_G IO_B	39 38 33	0.714 V_{p-p}	**Red, Green, and Blue Data Outputs.** The current source outputs of the D/A converters are capable of driving RS-343A/SMPTE-170M compatible levels into doubly-terminated 75 Ohm lines. Sync pulses may be added to any D/A output.
IO_S	37	0.714 V_{p-p}	**SYNC Current Output.** When this pin is connected to any of the D/A converter outputs, a 40 IRE offset is added to the video level. When the $\overline{SYNC}$ input is LOW, the current is turned off, bring the sync tip voltage to 0.0V. If no sync pulse is required, IO_S should be grounded. When $\overline{SYNC}$ is HIGH, the current flowing out of IO_S is: $IO_S = 3.64 (V_{REF} / R_{REF})$
Voltage Reference			
V_{REF}	41	+1.235 V	**Voltage Reference Input/Output.** An internal voltage source of +1.235 Volts is output on this pin. An external +1.235 Volt reference may be applied here which overrides the internal reference. Decoupling V_{REF} to GND with a 0.1µF ceramic capacitor is required.

Pin Descriptions (continued)

Pin Name	Pin Number	Value	Pin Function Description
R_{REF}	42	590 Ω	**Current-setting Resistor.** The full-scale output current of each D/A converter is determined by the value of the resistor connected between R_{REF} and GND. The nominal value for R_{REF} is found from: $R_{REF} = 9.1 (V_{REF}/I_{FS})$ where I_{FS} is the full-scale (white) output current (amps) from the D/A converter (without sync). Sync is 0.4 I_{FS}. D/A full-scale (white) current may also be calculated from: $I_{FS} = V_{FS}/R_L$ Where V_{FS} is the white voltage level and R_L is the total resistive load (ohms) on each D/A converter. V_{FS} is the blank to full-scale voltage.
COMP	40	0.1 µF	**Compensation Capacitor.** A 0.1 µF ceramic capacitor must be connected between COMP and V_{DD} to stabilize internal bias circuitry.
Power, Ground			
V_{DD}	17, 34–36	+5 V	**Power Supply.**
GND	29–32	0.0V	**Ground.**

Equivalent Circuits

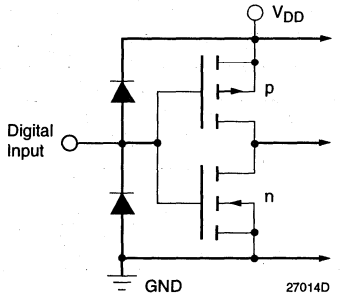


Figure 2. Equivalent Digital Input Circuit

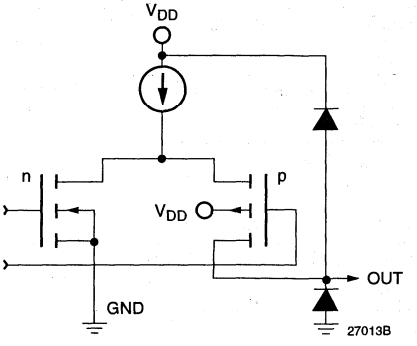


Figure 3. Equivalent Analog Output Circuit

Equivalent Circuits (continued)

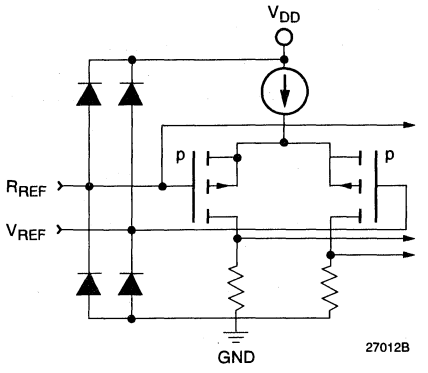


Figure 4. Equivalent Analog Input Circuit

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltage				
V_{DD} (Measured to GND)	-0.5		7.0	V
Inputs				
Applied Voltage (measured to GND)[2]	-0.5		V_{DD} + 0.5	V
Forced Current[3,4]	-10.0		10.0	mA
Outputs				
Applied Voltage (measured to GND)[2]	-0.5		V_{DD} + 0.5	V
Forced Current[3,4]	-60.0		60.0	mA
Short Circuit Duration (single output in HIGH state to ground)			infinite	second
Temperature				
Operating, Ambient	-20		110	°C
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C
Storage	-65		150	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_S	Conversion Rate	TMC3503-30			30	Msps
		TMC3503-50			50	Msps
		TMC3503-80			80	Msps
t_{PWH}	CLK Pulsewidth, HIGH		4			ns
t_{PWL}	CLK Pulsewidth, LOW		4			ns
t_s	Input Data Setup Time		3			ns
t_h	Input Date Hold Time		2			ns
V_{REF}	Reference Voltage, External		1.0	1.235	1.5	V
C_C	Compensation Capacitor			0.1		µF
R_L	Output Load			37.5		Ω
V_{IH}	Input Voltage, Logic HIGH		2.0		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW		GND		0.8	V
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions[3]	Min	Typ[1]	Max	Units
I_{DD}	Power Supply Current[2]	V_{DD} = Max				
		TMC3503-30			100	mA
		TMC3503-50			100	mA
		TMC3503-80			125	mA
I_{DDS}	Power Supply Current, Sleep Mode	V_{DD} = Max			3	mA
PD	Total Power Dissipation[2]	V_{DD} = Max				
		TMC3503-30			525	mW
		TMC3503-50			525	mW
		TMC3503-80			655	mW
R_O	Output Resistance			100		kΩ
C_O	Output Capacitance	I_{OUT} = 0mA			30	pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = 2.4V			-1	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0.4V			1	µA
I_{REF}	V_{REF} Input Bias Current			0	±100	µA
V_{REF}	Reference Voltage Output			1.235		V
V_{OC}	Output Compliance	Referred to V_{DD}	-0.4	0	+1.5	V
C_{DI}	Digital Input Capacitance			4	10	pF

Notes:

1. Values shown in Typ column are typical for V_{DD} = +5V and T_A = 25°C
2. Minimum/Maximum values with V_{DD} = Max and T_A = Min
3. V_{REF} = 1.235V, R_{LOAD} = 37.5Ω, R_{REF} = 590Ω

Switching Characteristics

Parameter		Conditions[2]	Min	Typ[1]	Max	Units
t_D	Clock to Output Delay	V_{DD} = Min		10	15	ns
t_{SKEW}	Output Skew			1	2	ns
t_R	Output Risetime	10% to 90% of Full Scale		2	3	ns
t_F	Output Falltime	90% to 10% of Full Scale		2	3	ns
t_{SET}	Output Settling Time	to 3%/FS		15		ns

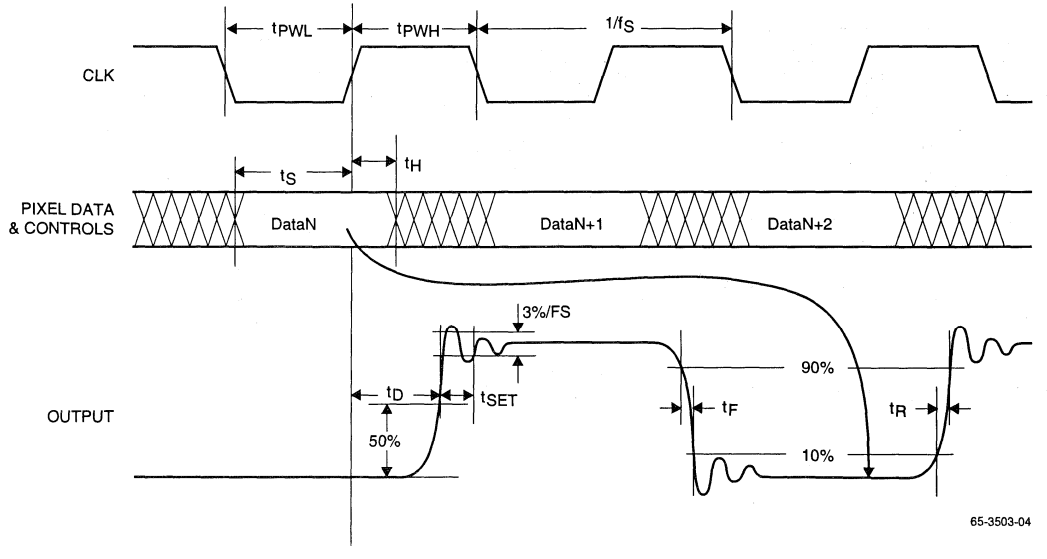
Notes:
1. Values shown in Typ column are typical for V_{DD} = +5V and T_A = 25°C.
2. V_{REF} = 1.235V, R_{LOAD} = 37.5Ω, R_{REF} = 590Ω.

System Performance Characteristics

Parameter		Conditions[2]	Min	Typ[1]	Max	Units
E_{LI}	Integral Linearity Error	V_{DD}, V_{REF} = Nom		±0.2	±0.3	%/FS
E_{LD}	Differential Linearity Error	V_{DD}, V_{REF} = Nom		±0.2	±0.3	%/FS
E_{DM}	DAC to DAC Matching	V_{DD}, V_{REF} = Nom		3	10	%
E_G	Absolute Gain Error	V_{DD}, V_{REF} = Nom			TBD	%/FS
TC_{EG}	Gain Error Tempco	V_{DD}, V_{REF} = Nom		TBD		PPM/°C
V_{OF}	Output Offset Current	V_{DD} = Max, R, G, B = 000h $\overline{SYNC}$ = $\overline{BLANK}$ = 0			20	mA
PSRR	Power Supply Rejection Ratio				0.05	%/%

Notes:
1. Values shown in Typ column are typical for V_{DD} = +5V and T_A = 25°C.
2. V_{REF} = 1.235V, R_{LOAD} = 37.5Ω, R_{REF} = 590Ω.

Timing Diagram



Application Notes

Figure 4 illustrates a typical TMC3503 interface circuit. In this example, an optional 1.2 Volt bandgap reference is connected to the V_{REF} output, overriding the internal voltage reference source.

Grounding

It is important that the TMC3503 power supply is well-regulated and free of high-frequency noise. Careful power supply decoupling will ensure the highest quality video signals at the output of the circuit. The TMC3503 has separate analog and digital circuits. To keep digital system noise from the D/A converter, it is recommended that power supply voltages (V_{DD}) come from the system analog power source and all ground connections (GND) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor D/A conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{REF}, I_{REF}, COMP, IO_S, IO_R, IO_G, IO_B) as short as possible and as far as possible from all digital signals. The TMC3503 should be located near the board edge, close to the analog output connectors.

2. The power plane for the TMC3503 should be separate from that which supplies the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC3503 is the same as that of the system's digital circuitry, power to the TMC3503 should be decoupled with 0.1µF and 0.01µF capacitors and isolated with a ferrite bead.

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. If the digital power supply has a dedicated power plane layer, it should not be placed under the TMC3503, the voltage reference, or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the TMC3503 and its related analog circuitry can have an adverse effect on performance.

5. CLK should be handled carefully. Jitter and noise on this clock will degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

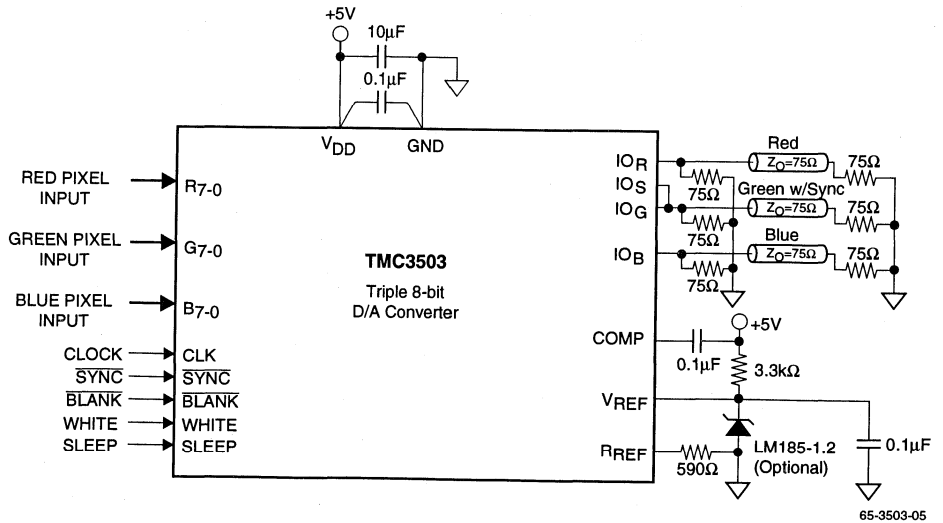


Figure 4. Typical Interface Circuit

Related Products

- TMC3003 Triple 10-bit 80 Msps D/A Converter
- TMC1175A 40 Msps CMOS 8-bit A/D Converter
- TMC1275 40 Msps CMOS 8-bit A/D Converter
- TMC22091, TMC22191 Digital Video Encoders
- TMC2242A/TMC2243/TMC2246A Video Filters
- TMC2249A Digital Mixer
- TMC2250A Matrix Multiplier
- TMC2272A Colorspace Converter
- TMC2302 Image Manipulation Sequencer
- TMC2340A Digital Synthesizer
- TMC2081 Digital Video Mixer

Ordering Information

Product Number	Conversion Rate (Msps)	Temperature Range	Screening	Package	Package Marking
TMC3503R2C30	30 Msps	T_A = 0°C to 70°C	Commercial	44-Lead PLCC	3503R2C30
TMC3503R2C50	50 Msps	T_A = 0°C to 70°C	Commercial	44-Lead PLCC	3503R2C50
TMC3503R2C80	80 Msps	T_A = 0°C to 70°C	Commercial	44-Lead PLCC	3503R2C80

Section 3 – High Speed Communications

Fibre Channel/ESCON

RCC700A

Fibre Channel/ESCON™/ATM Transceiver

194 to 266 Megabaud

Features

- 194 to 266 Megabaud data rates
- Compliant with Fibre Channel and ESCON standards
- Submicron CMOS technology
- PLL clock and data recovery
- Clock synthesizer
- Selectable 8 bit/10 bit encode, 10 bit/8 bit decode
- Parity generate/check
- Low power dissipation: 570 mW typ. at 200 Megabaud
- Byte sync on K28.1, K28.5 or K28.7
- Single power supply: +5V
- CMOS/TTL compatible parallel data inputs/outputs
- PECL compatible serial data inputs/outputs
- Available in 64-pin PQFP, 68-pin PLCC

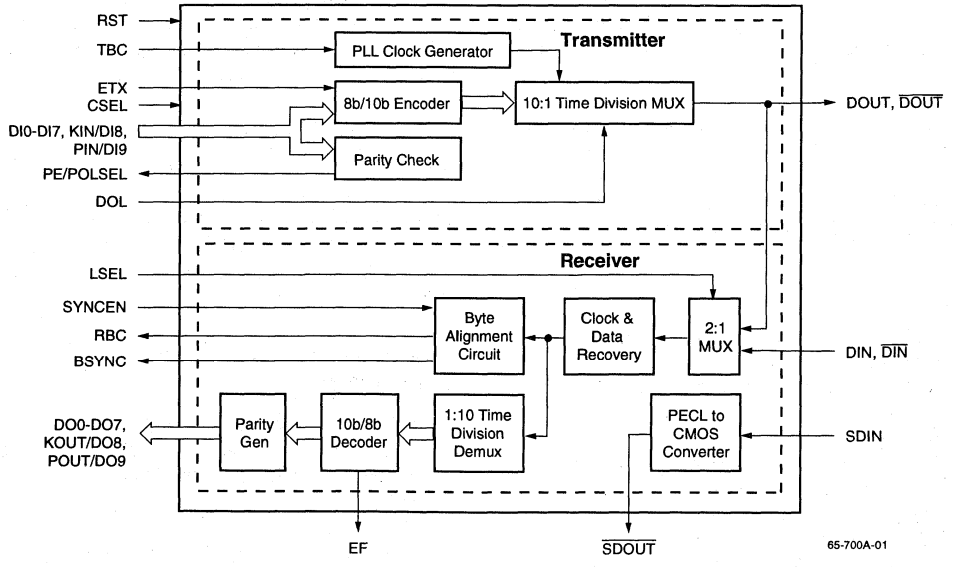
Applications

- Fibre Channel and ESCON Transceiver
- ATM Transceiver
- High-speed Fiber Optics or Copper links
- High-resolution graphic display terminal
- LAN Switching
- Video data transmission

Description

The RCC700A is a monolithic transmitter/receiver IC integrating a complete phase-locked loop clock recovery and data retiming/regeneration subsystem, a phase-locked loop clock synthesizer, a 10:1 mux, a 1:10 demux, an 8-bit/10-bit encoder, and an 10-bit/8-bit decoder. It operates with a single +5V power supply. The RCC700A provides a complete physical interface in compliance with the Fibre Channel Physical Layer Standard (FC-PH) specifications at 265.625 Megabaud (Mbaud), and Enterprise Systems Connection Architecture (ESCON) specifications at 200 Mbaud. RCC700A can also be used for the transport of Asynchronous Transfer Mode (ATM) LAN operating at 194.4 Mbaud (155.52 Megabits per second OC-3 data rate with 8b/10b overhead). 8 bit/10 bit encoder and 10 bit/8 bit decoder can be disabled through an external pin.

Block Diagram



ESCON™ is a trademark of International Business Machines.

Rev. 0.9.0

Functional Description

Transmitter Section

The RCC700A transmitter section includes a phase-locked loop synthesizer, an 8-bit/10-bit encoder, an input parity checker and a 10:1 multiplexer. The RCC700A accepts a CMOS/TTL data byte (DI0-DI7) along with the K character indicator (KIN) and parity bit (PIN) for CSEL = 0. For CSEL = 1, KIN and PIN become DI8 and DI9, respectively.

The Parity Check circuitry calculates the odd parity of the input data byte and compares it with PIN. If the calculated parity differs from PIN, the transmitter flags the error by bringing the parity error bit, PE to a HIGH level. For example, for DI0-DI7=00000101, PIN should be 1. If PIN is not equal to 1, PE=1.

The RCC700A transmitter section encodes the CMOS/TTL input data bye (DI0-DI7) into a 10-bit word using IBM's 8-bit/10-bit coding (see Table 1). The encoder is disabled if CSEL = 1, and enabled if CSEL = 0. The encoded word is then converted to a serial high speed data stream (DOUT/$\overline{\text{DOUT}}$) at 194 to 266 Mbaud via a 10:1 time division mux. The serial data stream (DOUT/$\overline{\text{DOUT}}$) is transmitted at PECL levels (positive shifted ECL levels, Vth = +3.7V).

The RCC700A features a Data Output Low function (DOL) that can force the data output (DOUT, $\overline{\text{DOUT}}$) to logic LOW for protection of the fiber optic module transmitter diode. DOL is controlled by the Protocol IC or the fiber optic transmitter module. The RCC700A also incorporates an Error Transmit input (ETX). The RCC700A sends a violating code when ETX is brought to a logic HIGH. If ETX stays HIGH for more than one byte clock cycle, the transmitter will send error bytes of alternate running disparities in order to maintain the DC balance of the line (100111 1011 or 011000 0100).

The 194 to 266 MHz clock used for the serial stream is generated using a PLL clock generator which multiplies the input frequency, 19.4 to 26.6 MHz, by a factor of 10. The input clock reference for the PLL clock generator, Transmit Byte Clock (TBC), typically comes from a crystal oscillator or from the system.

Receiver Section

The RCC700A receiver section includes a complete phase-locked loop clock recovery and data retiming/regeneration subsystem, a byte alignment circuit, a 1:10 demultiplexer, an 10-bit/8-bit decoder, a disparity/code violation checker and a parity generator. The RCC700A accepts a differential data stream (DIN/$\overline{\text{DIN}}$) at 194 to 266 Mbaud, recovers the clock and regenerates the encoded serial data. The recovered encoded data is then converted to 10 parallel data lines via a 1:10 time division demultiplexer and decoded into an 8-bit byte via the 10-bit/8-bit decoder. The decoder is disabled if CSEL = 1, and enabled if CSEL = 0. K Command characters are also detected and indicated by bringing the KOUT pin to a HIGH level. The odd parity of the output 8-bit byte (DO0-DO7) is calculated and available at pin POUT. For example, for DO0-DO7=00000101, POUT should be 1. For CSEL = 1, KOUT and POUT become D08 and D09, respectively. The RCC700A also generates a Receive Byte Clock (RBC) for driving the CMOS protocol layer IC. All the outputs to the protocol layer IC are at CMOS levels.

Running disparity and coding is checked during the 10-bit/8-bit decoding and violations are flagged by bringing the Error Flag (EF) to a HIGH level. If consecutive bytes have more 1s or more 0s, or if running disparity is different from expected for the received code, or the transmission character is not part of Table 1, EF goes HIGH. If 100111 1011 or 011000 0100 is received, EF=1, KOUT=1, DO0-DO7=00000000.

The RCC700A contains a byte synchronization circuitry. When enabled (SYNCEN HIGH), the RCC700A will automatically resynchronize the demultiplexer to byte align with the leading seven bits (00111 11 or 11000 00) of the transmission character, corresponding to reception of K28.1, K28.5 or K28.7).

SYNCEN pin gives the protocol layer IC the flexibility to request the RCC700A to align only when required, e.g. at power up or after loss of byte synchronization. The RCC700A also incorporates a PECL to CMOS converter to translate the PECL output signal from an optical receiver module SDIN to a CMOS output signal. This allows for direct interfacing with the CMOS protocol layer circuit. SDIN is active HIGH. Therefore, $\overline{\text{SDOUT}}$ will be at a CMOS level LOW when an optical signal is present at the input of the fiber optics receiver module.

Loopback Test Mode

The RCC700A features an internal differential loopback for on-board diagnostic of the device. When loop select (LSEL) is HIGH, the receiver accepts the output data from the transmitter section (DOUT, $\overline{\text{DOUT}}$). When LSEL is LOW, i.e., tied to GND, the receiver accepts the incoming input data (DIN, $\overline{\text{DIN}}$).

Use of Table 1 for Encoding/ Decoding

The following information describes how Table 1 can be used for generating valid transmission characters (encoding) and checking the validity of received transmission characters (decoding).

The transmission character is labelled "abcdeifghj". The transmission order is a,b,c...j in that order. HGFEDCBA cor-

responds to the data inputs DI7...DI0 in that order. In the table, each valid data byte and special code byte has two columns corresponding to the current value of the running disparity (CURRENT RD- or CURRENT RD+). Running disparity is a binary parameter with either the value + or -.

The transmitter calculates the new running disparity based on the contents of the transmitted character. Similarly, the receiver calculates the new running disparity based on the contents of the received character.

The first six bits of the character, "abcdei," form one sub-block, and "fghj" forms another sub-block for computing running disparity. Running disparity (CURRENT RD+ or CURRENT RD-) at the beginning of the 6-bit sub-block is the running disparity at the end of the last transmission character. Running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the transmission character is the running disparity at the end of the 4-bit sub-block.

Running disparity at the end of sub-block is positive, if it contains more 1s than 0s. It is also positive if it is 000111 for the 6-bit sub-block and 0011 for the 4-bit sub-block. Otherwise, the running disparity is the same as at the beginning of the sub-block.

CURRENT RD is used to select the transmission character for the data byte or special code.

While decoding the received character, the column corresponding to the current value of the receiver's running disparity shall be searched for the received transmission character. If the received transmission character is found in the proper column, the transmission character is considered valid and the associated data or special code byte decoded. Otherwise, the character is considered invalid and EF pin is held HIGH for that byte. Independent of the transmission character's validity, the received transmission character shall be used to calculate a new value of running disparity.

Detection of code violation (EF=HIGH) does not necessarily indicate that the transmission character in which the code violation was detected is in error. Code violation may occur due to the prior error which altered the running disparity of the bit stream but did not result in a detectable error at the transmission character in which it occurred. An example of an error scenario where the error is flagged after it happens is shown below (see Table 1).

Reset Function

For CSEL = 0, during normal operation, the reset input pin, RST, is LOW and is not used. Under total failure of receive PLL to acquire lock, this reset function can be used. When RST goes HIGH for at least 1 byte clock, the chip is reset, i.e. the receive PLL acquires lock to the bit clock derived from the TBC reference byte frequency and then to the incoming data.

For CSEL = 1, RST is normally HIGH and is LOW for at least 1 byte clock to reset.

Table 1. Example of Error Scenario

	RD	Character	RD	Character	RD	Character	RD
Transmitted character stream	-	D21.1	-	D10.2	-	D23.5	+
Transmitted bit stream	-	101010 1001	-	010101 0101	-	111010 1010	+
Bit stream after error	-	101010 1011	+	010101 0101	+	111010 1010	+
Decoded character stream	-	D21.0	+	D10.2	+	Error	+

Table 2. 8b/10b Encoding

DATA[3] BYTE NAME	BITS HGF	BITS EDCBA[1]	CURRENT RD- abcdei	CURRENT RD- fghj[2]	CURRENT RD+ abcdei	CURRENT RD+ fghj[2]
D0.0	000	00000	100111	0100	011000	1011
D1.0	000	00001	011101	0100	100010	1011
D2.0	000	00010	101101	0100	010010	1011
D3.0	000	00011	110001	1011	110001	0100
D4.0	000	00100	110101	0100	001010	1011
D5.0	000	00101	101001	1011	101001	0100
D6.0	000	00110	011001	1011	011001	0100
D7.0	000	00111	111000	1011	000111	0100
D8.0	000	01000	111001	0100	000110	1011
D9.0	000	01001	100101	1011	100101	0100
D10.0	000	01010	010101	1011	010101	0100
D11.0	000	01011	110100	1011	110100	0100
D12.0	000	01100	001101	1011	001101	0100
D13.0	000	01101	101100	1011	101100	0100
D14.0	000	01110	011100	1011	011100	0100
D15.0	000	01111	010111	0100	101000	1011
D16.0	000	10000	011011	0100	100100	1011
D17.0	000	10001	100011	1011	100011	0100
D18.0	000	10010	010011	1011	010011	0100
D19.0	000	10011	110010	1011	110010	0100
D20.0	000	10100	001011	1011	001011	0100
D21.0	000	10101	101010	1011	101010	0100
D22.0	000	10110	011010	1011	011010	0100
D23.0	000	10111	111010	0100	000101	1011
D24.0	000	11000	110011	0100	001100	1011
D25.0	000	11001	100110	1011	100110	0100
D26.0	000	11010	010110	1011	010110	0100
D27.0	000	11011	110110	0100	001001	1011
D28.0	000	11100	001110	1011	001110	0100
D29.0	000	11101	101110	0100	010001	1011
D30.0	000	11110	011110	0100	100001	1011
D31.0	000	11111	101011	0100	010100	1011
D0.1	001	00000	100111	1001	011000	1001
D1.1	001	00001	011101	1001	100010	1001
D2.1	001	00010	101101	1001	010010	1001
D3.1	001	00011	110001	1001	110001	1001
D4.1	001	00100	110101	1001	001010	1001
D5.1	001	00101	101001	1001	101001	1001
D6.1	001	00110	011001	1001	011001	1001
D7.1	001	00111	111000	1001	000111	1001
D8.1	001	01000	111001	1001	000110	1001
D9.1	001	01001	100101	1001	100101	1001
D10.1	001	01010	010101	1001	010101	1001
D11.1	001	01011	110100	1001	110100	1001
D12.1	001	01100	001101	1001	001101	1001
D13.1	001	01101	101100	1001	101100	1001
D14.1	001	01110	011100	1001	011100	1001
D15.1	001	01111	010111	1001	101000	1001

DATA[3] BYTE NAME	BITS HGF	BITS EDCBA[1]	CURRENT RD- abcdei	CURRENT RD- fghj[2]	CURRENT RD+ abcdei	CURRENT RD+ fghj[2]
D16.1	001	10000	011011	1001	100100	1001
D17.1	001	10001	100011	1001	100011	1001
D18.1	001	10010	010011	1001	010011	1001
D19.1	001	10011	110010	1001	110010	1001
D20.1	001	10100	001011	1001	001011	1001
D21.1	001	10101	101010	1001	101010	1001
D22.1	001	10110	011010	1001	011010	1001
D23.1	001	10111	111010	1001	000101	1001
D24.1	001	11000	110011	1001	001100	1001
D25.1	001	11001	100110	1001	100110	1001
D26.1	001	11010	010110	1001	010110	1001
D27.1	001	11011	110110	1001	001001	1001
D28.1	001	11100	001110	1001	001110	1001
D29.1	001	11101	101110	1001	010001	1001
D30.1	001	11110	011110	1001	100001	1001
D31.1	001	11111	101011	1001	010100	1001
D0.2	010	00000	100111	0101	011000	0101
D1.2	010	00001	011101	0101	100010	0101
D2.2	010	00010	101101	0101	010010	0101
D3.2	010	00011	110001	0101	110001	0101
D4.2	010	00100	110101	0101	001010	0101
D5.2	010	00101	101001	0101	101001	0101
D6.2	010	00110	011001	0101	011001	0101
D7.2	010	00111	111000	0101	000111	0101
D8.2	010	01000	111001	0101	000110	0101
D9.2	010	01001	100101	0101	100101	0101
D10.2	010	01010	010101	0101	010101	0101
D11.2	010	01011	110100	0101	110100	0101
D12.2	010	01100	001101	0101	001101	0101
D13.2	010	01101	101100	0101	101100	0101
D14.2	010	01110	011100	0101	011100	0101
D15.2	010	01111	010111	0101	101000	0101
D16.2	010	10000	011011	0101	100100	0101
D17.2	010	10001	100011	0101	100011	0101
D18.2	010	10010	010011	0101	010011	0101
D19.2	010	10011	110010	0101	110010	0101
D20.2	010	10100	001011	0101	001011	0101
D21.2	010	10101	101010	0101	101010	0101
D22.2	010	10110	011010	0101	011010	0101
D23.2	010	10111	111010	0101	000101	0101
D24.2	010	11000	110011	0101	001100	0101
D25.2	010	11001	100110	0101	100110	0101
D26.2	010	11010	010110	0101	010110	0101
D27.2	010	11011	110110	0101	001001	0101
D28.2	010	11100	001110	0101	001110	0101
D29.2	010	11101	101110	0101	010001	0101
D30.2	010	11110	011110	0101	100001	0101
D31.3	010	11111	101011	0101	010100	0101

Table 2. 8b/10b Encoding (continued)

DATA[3] BYTE NAME	BITS HGF	BITS EDCBA[1]	CURRENT RD- abcdei	CURRENT RD- fghj[2]	CURRENT RD+ abcdei	CURRENT RD+ fghj[2]
D0.3	011	00000	100111	0011	011000	1100
D1.3	011	00001	011101	0011	100010	1100
D2.3	011	00010	101101	0011	010010	1100
D3.3	011	00011	110001	1100	110001	0011
D4.3	011	00100	110101	0011	001010	1100
D5.3	011	00101	101001	1100	101001	0011
D6.3	011	00110	011001	1100	011001	0011
D7.3	011	00111	111000	1100	000111	0011
D8.3	011	01000	111001	0011	000110	1100
D9.3	011	01001	100101	1100	100101	0011
D10.3	011	01010	010101	1100	010101	0011
D11.3	011	01011	110100	1100	110100	0011
D12.3	011	01100	001101	1100	001101	0011
D13.3	011	01101	101100	1100	101100	0011
D14.3	011	01110	011100	1100	011100	0011
D15.3	011	01111	010111	0011	101000	1100
D16.3	011	10000	011011	0011	100100	1100
D17.3	011	10001	100011	1100	100011	0011
D18.3	011	10010	010011	1100	010011	0011
D19.3	011	10011	110010	1100	110010	0011
D20.3	011	10100	001011	1100	001011	0011
D21.3	011	10101	101010	1100	101010	0011
D22.3	011	10110	011010	1100	011010	0011
D23.3	011	10111	111010	0011	000101	1100
D24.3	011	11000	110011	0011	001100	1100
D25.3	011	11001	100110	1100	100110	0011
D26.3	011	11010	010110	1100	010110	0011
D27.3	011	11011	110110	0011	001001	1100
D28.3	011	11100	001110	1100	001110	0011
D29.3	011	11101	101110	0011	010001	1100
D30.3	011	11110	011110	0011	100001	1100
D31.3	011	11111	101011	0011	010100	1100
D0.4	100	00000	100111	0010	011000	1101
D1.4	100	00001	011101	0010	100010	1101
D2.4	100	00010	101101	0010	010010	1101
D3.4	100	00011	110001	1101	110001	0010
D4.4	100	00100	110101	0010	001010	1101
D5.4	100	00101	101001	1101	101001	0010
D6.5	100	00110	011001	1101	011001	0010
D7.5	100	00111	111000	1101	000111	0010
D8.5	100	01000	111001	0010	000110	1101
D9.5	100	01001	100101	1101	100101	0010
D10.4	100	01010	010101	1101	010101	0010
D11.4	100	01011	110100	1101	110100	0010
D12.4	100	01100	001101	1101	001101	0010
D13.4	100	01101	101100	1101	101100	0010
D14.4	100	01110	011100	1101	011100	0010
D15.4	100	01111	010111	0010	101000	1101
D16.4	100	10000	011011	0010	100100	1101
D17.4	100	10001	100011	1101	100011	0010
D18.4	100	10010	010011	1101	010011	0010
D19.4	100	10011	110010	1101	110010	0010
D20.4	100	10100	001011	1101	001011	0010
D21.4	100	10101	101010	1101	101010	0010
D22.4	100	10110	011010	1101	011010	0010
D23.4	100	10111	111010	0010	000101	1101
D24.4	100	11000	110011	0010	001100	1101
D25.4	100	11001	100110	1101	100110	0010
D26.4	100	11010	010110	1101	010110	0010
D27.4	100	11011	110110	0010	001001	1101
D28.4	100	11100	001110	1101	001110	0010
D29.4	100	11101	101110	0010	010001	1101
D30.4	100	11110	011110	0010	100001	1101
D31.4	100	11111	101011	0010	010100	1101
D0.5	101	00000	100111	1010	011000	1010
D1.5	101	00001	011101	1010	100010	1010
D2.5	101	00010	101101	1010	010010	1010
D3.5	101	00011	110001	1010	110001	1010
D4.5	101	00100	110101	1010	001010	1010
D5.5	101	00101	101001	1010	101001	1010
D6.5	101	00110	011001	1010	011001	1010
D7.5	101	00111	111000	1010	000111	1010
D8.5	101	01000	111001	1010	000110	1010
D9.5	101	01001	100101	1010	100101	1010
D10.5	101	01010	010101	1010	010101	1010
D11.5	101	01011	110100	1010	110100	1010
D12.5	101	01100	001101	1010	001101	1010
D13.5	101	01101	101100	1010	101100	1010
D14.5	101	01110	011100	1010	011100	1010
D15.5	101	01111	010111	1010	101000	1010
D16.5	101	10000	011011	1010	100100	1010
D17.5	101	10001	100011	1010	100011	1010
D18.5	101	10010	010011	1010	010011	1010
D19.5	101	10011	110010	1010	110010	1010
D20.5	101	10100	001011	1010	001011	1010
D21.5	101	10101	101010	1010	101010	1010
D22.5	101	10110	011010	1010	011010	1010
D23.5	101	10111	111010	1010	000101	1010
D24.5	101	11000	110011	1010	001100	1010
D25.5	101	11001	100110	1010	100110	1010
D26.5	101	11010	010110	1010	010110	1010
D27.5	101	11011	110110	1010	001001	1010
D28.5	101	11100	001110	1010	001110	1010
D29.5	101	11101	101110	1010	010001	1010
D30.5	101	11110	011110	1010	100001	1010
D31.5	101	11111	101011	1010	010100	1010

Table 2. 8b/10b Encoding (continued)

DATA[3] BYTE NAME	BITS HGF	BITS EDCBA	CURRENT RD- abcdei	CURRENT RD- fghj[2]	CURRENT RD+ abcdei	CURRENT RD+ fghj[2]
D0.6	110	00000	10011	0110	01100	0110
D1.6	110	00001	01110	0110	10001	0110
D2.6	110	00010	10110	0110	01001	0110
D3.6	110	00011	11000	0110	11000	0110
D4.6	110	00100	11010	0110	00101	0110
D5.6	110	00101	10100	0110	10100	0110
D6.6	110	00110	01100	0110	01100	0110
D7.6	110	00111	11100	0110	00011	0110
D8.6	110	01000	11100	0110	00011	0110
D9.6	110	01001	10010	0110	10010	0110
D10.6	110	01010	01010	0110	01010	0110
D11.6	110	01011	11010	0110	11010	0110
D12.6	110	01100	00110	0110	00110	0110
D13.6	110	01101	10110	0110	10110	0110
D14.6	110	01110	01110	0110	01110	0110
D15.6	110	01111	01011	0110	10100	0110
D16.6	110	10000	01101	0110	10010	0110
D17.6	110	10001	10001	0110	10001	0110
D18.6	110	10010	01001	0110	01001	0110
D19.6	110	10011	11001	0110	11001	0110
D20.6	110	10100	00101	0110	00101	0110
D21.6	110	10101	10101	0110	10101	0110
D22.6	110	10110	01101	0110	01101	0110
D23.6	110	10111	11101	0110	00010	0110
D24.6	110	11000	11001	0110	00110	0110
D25.6	110	11001	10011	0110	10011	0110
D26.6	110	11010	01011	0110	01011	0110
D27.6	110	11011	11011	0110	00100	0110
D28.6	110	11100	00111	0110	00111	0110
D29.6	110	11101	10111	0110	01000	0110
D30.6	110	11110	01111	0110	10000	0110
D31.6	110	11111	10101	0110	01010	0110

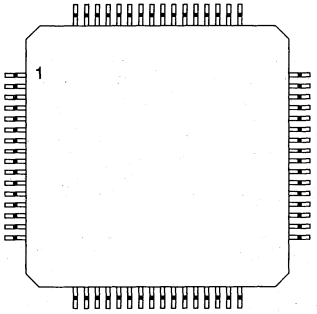
DATA[3] BYTE NAME	BITS HGF	BITS EDCBA	CURRENT RD- abcdei	CURRENT RD- fghj[2]	CURRENT RD+ abcdei	CURRENT RD+ fghj[2]
D0.7	111	00000	10011	0001	01100	1110
D1.7	111	00001	01110	0001	10001	1110
D2.7	111	00010	10110	0001	01001	1110
D3.7	111	00011	11000	1110	11000	0001
D4.7	111	00100	11010	0001	00101	1110
D5.7	111	00101	10100	1110	10100	0001
D6.7	111	00110	01100	1110	01100	0001
D7.7	111	00111	11100	1110	00011	0001
D8.7	111	01000	11100	0001	00011	1110
D9.7	111	01001	10010	1110	10010	0001
D10.7	111	01010	01010	1110	01010	0001
D11.7	111	01011	11010	1110	11010	1000
D12.7	111	01100	00110	1110	00110	0001
D13.7	111	01101	10110	1110	10110	1000
D14.7	111	01110	01110	1110	01110	1000
D15.7	111	01111	01011	0001	10100	1110
D16.7	111	10000	01101	0001	10010	1110
D17.7	111	10001	10001	0111	10001	0001
D18.7	111	10010	01001	0111	01001	0001
D19.7	111	10011	11001	1110	11001	0001
D20.7	111	10100	00101	0111	00101	0001
D21.7	111	10101	10101	1110	10101	0001
D22.7	111	10110	01101	1110	01101	0001
D23.7	111	10111	11101	0001	00010	1110
D24.7	111	11000	11001	0001	00110	1110
D25.7	111	11001	10011	1110	10011	0001
D26.7	111	11010	01011	1110	01011	0001
D27.7	111	11011	11011	0001	00100	1110
D28.7	111	11100	00111	1110	00111	0001
D29.7	111	11101	10111	0001	01000	1110
D30.7	111	11110	01111	0001	10000	1110
D31.7	111	11111	10101	0001	01010	1110

DATA[4] BYTE NAME	BITS HGF	BITS EDCBA[1]	CURRENT RD- abcdei	CURRENT RD- fghj[2]	CURRENT RD+ abcdei	CURRENT RD+ fghj[2]
K28.0	000	11100	001111	0100	110000	1011
K28.1	001	11100	001111	1001	110000	0110
K28.2	010	11100	001111	0101	110000	1010
K28.3	011	11100	001111	0011	110000	1100
K28.4	100	11100	001111	0010	110000	1101
K28.5	101	11100	001111	1010	110000	0101
K28.6	110	11100	001111	0110	110000	1001
K28.7	111	11100	001111	1000	110000	0111
K23.7	111	10111	111010	1000	000101	0111
K27.7	111	11011	110110	1000	001001	0111
K29.7	111	11101	101110	1000	010001	0111
K30.7	111	11110	011110	1000	100001	0111

Notes:

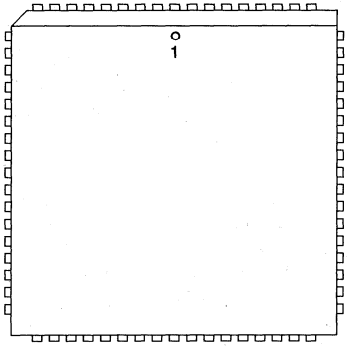
1. "HGF EDC BA" corresponds to DI7 ...0 in that order
2. a is to be transmitted first, followed by b, c, d ....j in that order
3. Kin=0
4. Kin=1

Pin Assignments



65-700A-02

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DO2	17	DI7	33	DOUT	49	$\overline{\text{SDOUT}}$
2	DO1	18	DI6	34	$\overline{\text{DOUT}}$	50	CSEL
3	DO0	19	DI5	35	LSEL	51	SYNCEN
4	DVCC	20	DI4	36	AGND	52	BSYNC
5	DVCC	21	DI3	37	AVCC	53	DVCC
6	DGND	22	DI2	38	AVCC	54	DGND
7	DGND	23	DI1	39	AGND	55	DVCC
8	POUT/DO9	24	DI0	40	AGND	56	DGND
9	KOUT/DO8	25	DGND	41	AVCC	57	DVCC
10	EF	26	TBC	42	AVCC	58	DGND
11	RBC	27	DVCC	43	AGND	59	DO7
12	DGND	28	RST	44	AVCC	60	DO6
13	PE/POLSEL	29	DGND	45	AGND	61	DO5
14	PIN/DI9	30	DVCC	46	SDIN	62	DO4
15	KIN/DI8	31	DOL	47	$\overline{\text{DIN}}$	63	DO3
16	ETX	32	DGND	48	DIN	64	DGND



65-700A-07

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DGND	18	POUT/DO9	35	DI0	52	AGND
2	DVCC	19	KOUT/DO8	36	DGND	53	AVCC
3	DGND	20	EF	37	TBC	54	AVCC
4	DO7	21	RBC	38	NC	55	AGND
5	DO6	22	DGND	39	RST	56	AVCC
6	DO5	23	PE/POLSEL	40	DGND	57	AGND
7	DO4	24	PIN/DI9	41	DVCC	58	SDIN
8	DO3	25	KIN/DI8	42	DOL	59	$\overline{\text{DIN}}$
9	DGND	26	ETX	43	DGND	60	DIN
10	DGND	27	DGND	44	DOUT	61	DGND
11	DO2	28	DI7	45	$\overline{\text{DOUT}}$	62	$\overline{\text{SDOUT}}$
12	DO1	29	DI6	46	NC	63	CSEL
13	DO0	30	DI5	47	LSEL	64	SYNCEN
14	DVCC	31	DI4	48	AGND	65	BSYNC
15	DVCC	32	DI3	49	AVCC	66	DVCC
16	DGND	33	DI2	50	AVCC	67	DGND
17	DGND	34	DI1	51	AGND	68	DVCC

Pin Descriptions

Name	Pin Number		Function
	64-pin PQFP	68-pin PLCC	
DVCC	4, 5, 27, 30, 53, 55, 57	2, 14, 15, 41, 66, 68	Positive supply for digital circuitry. The nominal value is 5V ±5%. VCC should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
AVCC	37, 38, 41, 42, 44	49, 50, 53, 54, 56	Positive supply for analog circuitry. The nominal value is 5V ±5%. VCC should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
DGND	6, 7, 12, 25, 29, 32, 54, 56, 58, 64	1, 3, 9, 10, 16, 17, 22, 27, 36, 40, 43, 61, 67	Chip ground for digital circuitry. DGND should be connected to the printed circuit board's ground plane at the pins.
AGND	36, 39, 40, 43, 45	48, 51, 52, 55, 57	Chip ground for analog circuitry. AGND should be connected to the printed circuit board's ground plane at the pins.
DI0-DI7	24, 23, 22, 21, 20, 19, 18, 17	35, 34, 33, 32, 31, 30, 29, 28	Transmitter input data (TTL levels).

Pin Descriptions (continued)

Name	Pin Number		Function
	64-pin PQFP	68-pin PLCC	
TBC	26	37	Transmit Byte Clock input (TTL level). Input reference frequency for the internal high speed clock generator: 19.4 to 26.6 MHz.
KIN/DI8	15	25	K character indicator input/Transmitter input data (TTL levels). If CSEL = 0, this pin in KIN. If CSEL = 1, this pin is DI8.
PIN/DI9	14	24	Odd parity input /Transmitter input data (TTL levels). If CSEL = 0, this pin in PIN. If CSEL = 1, this pin is DI9.
PE/ POLSEL	13	23	Parity Error indicator output/Polarity Select Input (CMOS/TTL levels). For CSEL = 0, This pin is PE. For CSEL = 1, This pin is POLSEL. PE will stay low when the on-chip calculated odd parity matches the incoming parity PIN. If there is a parity error, the PE flag is raised to a level HIGH. If POLSEL = 0, the receive data output timing specifications are with respect to the positive edge of RBC. If POLSEL = 1, the above specifications are with respect to the negative edge of RBC.
DOUT/ $\overline{\text{DOUT}}$	33,34	44,45	Transmitter differential output data (PECL levels). The output is a current mode driver with a nominal current driver of 8 mA. To generate a 0.8 V swing, use a 100Ω resistor across DOUT, $\overline{\text{DOUT}}$.
DOL	31	42	Data Output Low control input (TTL level). When HIGH, it forces the output to a logic low state (DOUT = LOW and $\overline{\text{DOUT}}$ = HIGH) to protect the fiber optic source. Connect to GND or leave open when not used.
LSEL	35	47	Loop Select input (TTL level). Internal differential loopback for "on-board" diagnostic of the device. When loop select (LSEL) is HIGH, the receiver accepts the output data from the transmitter section (DOUT/$\overline{\text{DOUT}}$). When LSEL is LOW, i.e. tied to GND, the receiver accepts the incoming input data (DIN/$\overline{\text{DIN}}$). Connect to GND or leave open when not used.
DIN/$\overline{\text{DIN}}$	48, 47	60, 59	Receiver differential input data (PECL levels).
SYNCEN	51	64	Byte Synchronization Enable input (TTL level). When SYNCEN is HIGH, the RCC700A will automatically resynchronize the demultiplexer to byte align with the received K28.1, K28.5 or K28.7 for both negative and positive running disparities (RD- and RD+). Connect to GND or leave open when not used.
BSYNC	52	65	Byte Synchronized output flag (CMOS levels). BSYNC goes to a HIGH level for one byte clock when SYNCEN is HIGH and the RCC700A detects and resynchronizes on K28.1, K28.5 or K28.7.
SDIN	46	58	Signal Detect input (PECL level). PECL input of the PECL to CMOS converter for the signal detect flag of the fiber optics receiver module. Leave open when not used.
$\overline{\text{SDOUT}}$	49	62	Signal Detect Output (CMOS level). CMOS output of the PECL to CMOS converter for the signal detect flag of the fiber optics receiver module. $\overline{\text{SDOUT}}$ is LOW when SDIN is HIGH.
DO0-DO7	3, 2, 1, 63, 62, 61, 60, 59	13, 12, 11, 8, 7, 6, 5, 4	Receiver output data/Receive output data (CMOS levels).
KOUT/DO8	9	19	K character indicator output / Receive Output Data (CMOS level). If CSEL = 0, this pin is KOUT. If CSEL = 1, this pin is DO8.
POUT/DO9	8	18	Odd parity output/Receive output data (CMOS level). If CSEL = 0, this pin is POUT. POUT is HIGH when the parity of the DO0...DO7 byte is even. If CSEL = 1, this pin is DO9.

Pin Descriptions (continued)

Name	Pin Number		Function
	64-pin PQFP	68-pin PLCC	
RBC	11	21	Receive Byte Clock output (CMOS level): 19.4 to 26.6 MHz.
EF	10	20	Error Flag output (CMOS level). EF goes HIGH to flag running disparity and coding violations detected during the 10b/8b decoding.
RST	28	39	Asynchronous reset input (TTL level). For CSEL = 0, this pin is normally LOW, and when HIGH for at least one byte clock, is used to reset all functions of the chip. This is a master reset. For CSEL = 1, this pin is normally HIGH, and when LOW for at least one byte clock, provides reset.
ETX	16	26	Error Transmit input (TTL level). This pin is only applicable of CSEL = 0 and is a No Connect for CSEL = 1. This pin is normally LOW. This pin, when HIGH, is used to force DC balanced alternating violation codes on its serial output.
CSEL	50	63	Select input (TTL level). This pin is normally low and enables the 8b/10b encoder/decoder circuitry. When high, the 8b/10b encoder/decoder is disabled and the following pins are affected: PIN/DI9, KIN/DI8, POUT/DO9, KOUT/DO8, PE/POLSEL, RST, and ETX.
NC	—	38, 46	No connection.

Absolute Maximum Ratings[1]

Parameter	Min	Max	Unit
Storage temperature range	-65	150	°C
Junction temperature range	-55	150	°C
Lead temperature range (soldering, 10 seconds)		300	°C
Positive power supply, V_{CC}	0	6	V
Voltage applied to any TTL inputs	-1	6	V
Voltage applied to any CMOS inputs	-1	6	V
Voltage applied to any PECL inputs	-1	6	V
Voltage applied to any CMOS outputs	-1	6	V
Voltage applied to any PECL outputs	-1	6	V
Current from any CMOS outputs	-50	50	mA
Current from any PECL outputs	-50	50	mA

Note:

1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Units
T_A	Ambient operating temperature	0		70	°C
V_{CC}	Positive supply voltage (DVCC and AVCC)	4.75	5.0	5.25	V
R_I	PECL differential load resistance[1]	80	100	150	Ω

Note:
1. Differential load resistance of 100Ω equals connection of 50Ω to AC ground on each of DOUT, $\overline{DOUT}$.

DC Electrical Characteristics

V_{CC} = 5V ±5%, GND = 0V unless otherwise indicated.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
Transmitter						
V_{IH}	TTL input voltage HIGH		2.0		V_{CC} +0.5	V
V_{IL}	TTL input voltage LOW				0.8	V
I_{IH}	TTL input HIGH current	V_{CC} = max, V_{IN} = 2.7V			100	µA
I_{IL}	TTL input LOW current	V_{CC} = max, V_{IN} = 0.4V	-1		100	µA
C_I	Input capacitance			4	10	pF
V_{OHP}	PECL output voltage HIGH	R_{DIFF} = 100Ω, V_{CC} = 5V	3.5	3.8	4.2	V
V_{OLP}	PECL ouput voltage LOW	R_{DIFF} = 100Ω, V_{CC} = 5V	2.6	3.0	3.4	V
V_{OP}	PECL output voltage amplitude	V_{OHP} - V_{OLP}, V_{CC} = 5V	0.6	0.8	1.0	V
I_O	PECL output current			8		mA
Receiver						
V_{IH}	TTL input voltage HIGH		2.0		V_{CC} +0.5	V
V_{IL}	TTL input voltage LOW		0		0.8	V
I_{IH}	TTL input HIGH current	V_{CC} = max, Vin = 2.7V			100	µA
I_{IL}	TTL input LOW current	V_{CC} = max, Vin = 0.4V			-100	µA
V_{CM}	Com. mode range (DIN, $\overline{DIN}$)		2.8		4.5	V
V_{DIFF}	Diff. input voltage (DIN, $\overline{DIN}$)		0.4			V
I_{IPH}	PECL input HIGH current	V_{IH} = V_{CC} -0.88V			100	µA
I_{IPL}	PECL input LOW current	V_{IL} = V_{CC} - 1.81V	-100			µA
V_{OHC}	CMOS output voltage HIGH	I_{OH}= -4.1mA (-8.1mA for RBC)	3.5		V_{CC}	V
V_{OLC}	CMOS output voltage LOW	I_{OL}= 4.1 mA (8.1 mA for RBC)	0		0.5	V
I_{OLC}	Output current (except RBC)	Forcing V_{OH}, V_{OL}	4			mA
I_{OLC}	Output current (RBC)	Forcing V_{OH}, V_{OL}	8			mA
I_{CC}	Supply current (200 Mbaud)[1]	V_{CC} = 5.25V		110	140	mA
	(266 Mbaud)	V_{CC} = 5.25V		135	150	mA
PD	Power dissipation (200 Mbaud)[1]	Based on I_{CC}		570		mW
	(266 Mbaud)	Based on I_{CC}		690		mW

Note:
1. Under both transmit and receive output switching conditions

Preliminary Information

AC Electrical Characteristics[1]

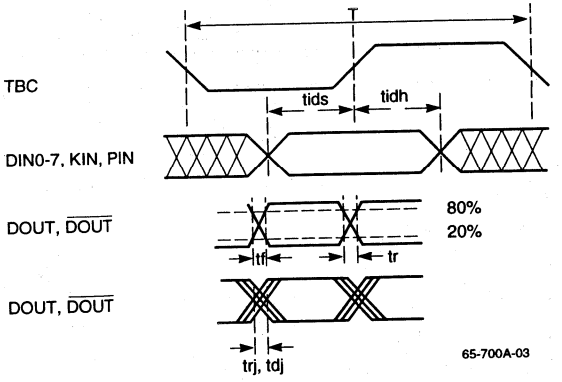
V_{CC} = 5V ±5%, GND = 0V unless otherwise indicated.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
Transmitter						
T	TBC Period	266 Mbaud		37.7		ns
		200 Mbaud		50		ns
t_{acq}	Acquisition time	Note 2			1	ms
t_{ids}[6]	DIN0..7, KIN, PIN valid to TBC setup ↑		4			ns
t_{idh}[6]	TBC ↑ to DIN0..7, KIN, PIN invalid hold		4			ns
F_{out}	Output data rate		194		266	Mbaud
t_r, t_f	DOUT, $\overline{DOUT}$ rise and fall times	20% to 80% points			500	ps
t_{rj}	DOUT, $\overline{DOUT}$ pk-pk random jitter	Note 3		220		ps
t_{dj}	DOUT, $\overline{DOUT}$ pk-pk deterministic jitter	Note 4		125		ps
Receiver						
f_{cc}	Input data rate variation				±1000	ppm
D	Input data transition density to acquire and maintain lock		0.25			
t_{acq}	Loop acquisition time for 10E-12 BER				2500	bits
f_c	Loop capture range		±1000			ppm
t_j	DIN, $\overline{DIN}$ input peak to peak jitter	Note 5			0.07T	ns
t_h	RBC pulsewidth HIGH		0.4T	0.5T	0.6T	ns
t_{od}[6, 7]	RBC ↑ to DO0..7 KOUT, POUT, BSYNC delay (CSEL = 0, or CSEL = 1, POLSEL = 0)	200 Mbaud	20		30	ns
		266 Mbaud	15		25	ns
T	RBC period	266 Mbaud		37.7		ns
		200 Mbaud		50.0		ns

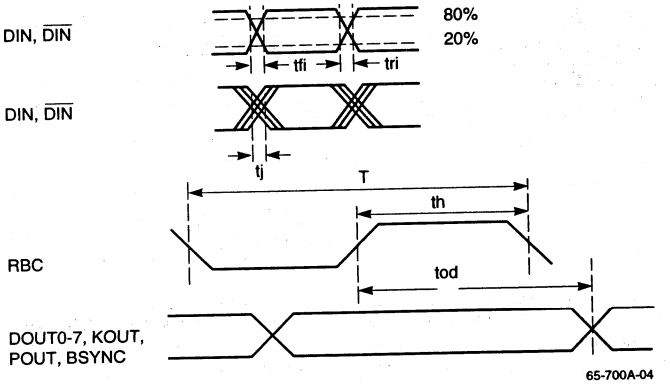
Notes:

1. Test conditions (unless otherwise indicated): PECL input rise and fall times, ≤2 ns, RLOAD = 100Ω across DOUT, $\overline{DOUT}$; TTL input rise and fall times ≤15 ns. Receiver input data rate = 200 or 265.625 Mbaud and ±1000 ppm; transition density ≥ 0.25.
2. Acquisition time is the time to establish lock once the device is powered up to the operating VCC range.
3. Input test pattern K28.7. Jitter measured at 50% amplitude, for a BER of 10E-12 with receiver running asynchronously.
4. Input test pattern K28.5. Jitter measured at 50% amplitude.
5. Guaranteed by design.
6. For CSEL = 0, the input pins are DI0..7, KIN and PIN, and the output pins are DO0..7, KOUT, and POUT. For CSEL = 1, the input pins are DI0..DI9, and the output pins are DO0..9.
7. For CSEL = 1 and POLSEL = 1, the timing specifications are with respect to the negative edge of RBC.

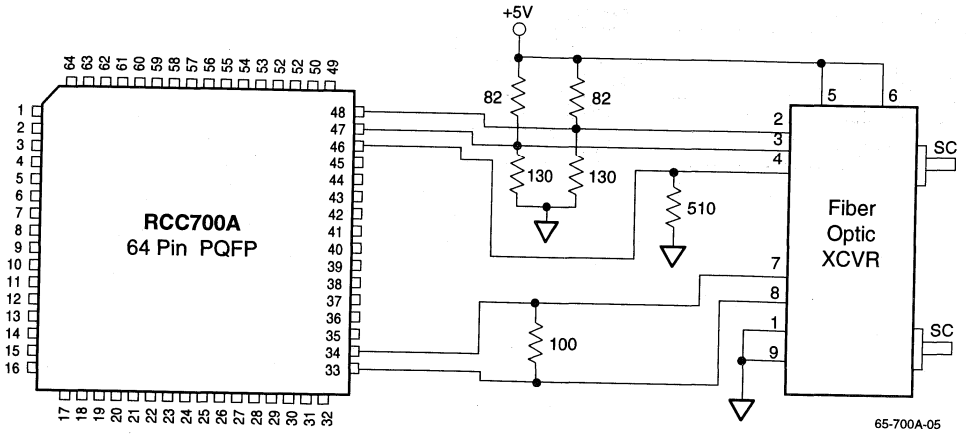
Transmitter Timing



Receiver Timing



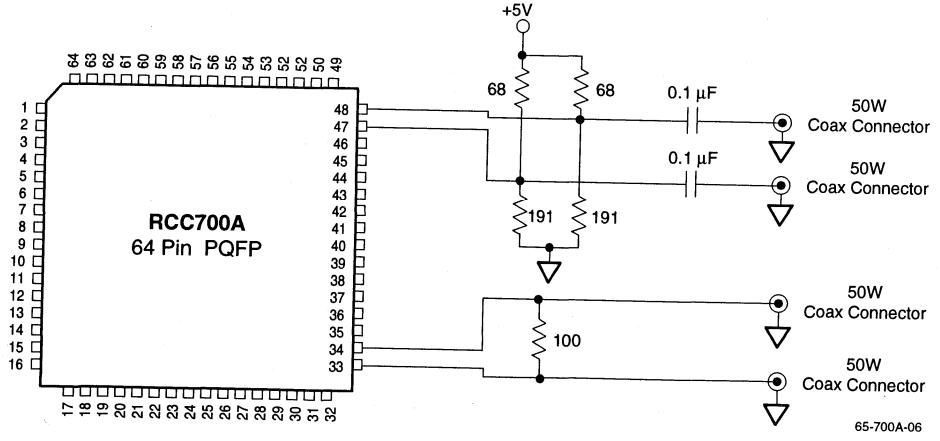
Applications Discussion



Interconnection of RCC700A to a Fiber Optic Transceiver

Recommended Fiber Optic Transceivers:

1. HP BR-5302
2. Siemens V23806-A7-C2



Interconnection of RCC700A to a Coax Cable

Ordering Information

Part Number	Package
RCC700AKA-200	64 PQFP
RCC700AQD-200	68 PLCC
RCC700AKA-266	64 PQFP
RCC700AQD-266	68 PLCC

Section 4 – Personal Computers

DC-DC Converters

Sound Drivers

Video Products

RC5010

Step-up Regulator for Notebook PCs

Features

- High efficiency – 85% typical
- Low quiescent current – 215 µA
- Adjustable output – 1.3V to 30V
- High switch current – 200 mA
- Bandgap reference – 1.31V
- Accurate oscillator frequency – ±10%
- Remote shutdown capability
- Low battery detection circuitry
- Low component count
- 8 pin SOIC

Applications

- Notebooks, sub-notebooks & PDAs
- LCD panels

Functional Description

The RC5010 monolithic IC is a low power switch mode regulator designed for notebook and sub notebook power supply applications. This DC-to-DC converter IC provides all of the active components needed to create supplies for portable computers (load power up to 400 mW, or up to 10W with an external power transistor). Contained internally are an oscillator, switch, reference, comparator, and logic, plus a discharged battery detection circuit.

The RC5010 can be used in PCMCIA Flash Memory cards, RF LAN cards, etc. where a non-standard voltage supply is needed.

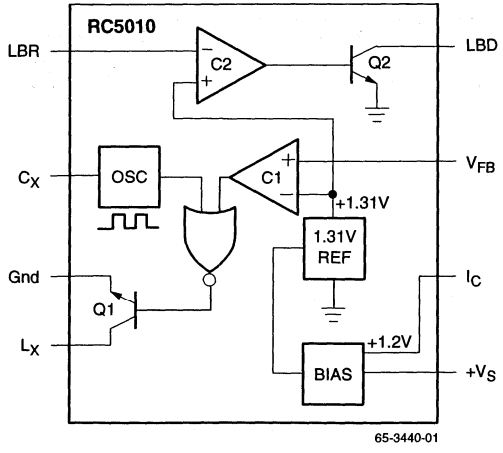
The regulator can achieve 85% efficiency in most applications while operating over a wide supply voltage range, 2.2V to 30V, at a very low quiescent current drain of 0.2mA, and 2µA in shutdown mode.

The standard application circuit requires seven external components for step-up operation: an inductor, a steering diode, three resistors, a low value timing capacitor, and an electrolytic filter capacitor. The combination of low supply current, small package, and ease of application makes the RC5010 adaptable to a wide range of battery operated notebook computers and PDAs.

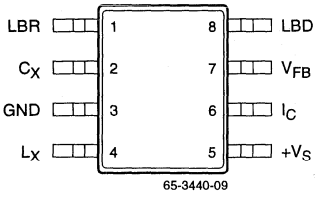
The RC5010 is most suited for single ended step-up (V_{OUT} > V_{IN}) circuits because the NPN internal switch transistor is referenced to ground.

With some optional external components the application circuit can be designed to display when the battery voltage falls below a predetermined level; the application can flag low at one level and then shut itself off after the battery decays to a second level. See the applications section for these and other applications.

Block Diagram



Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Function
LBR	1	Low Battery (Set) Resistor
C_X	2	Timing Capacitor
GND	3	Ground
L_X	4	External Inductor
$+V_S$	5	+Supply Voltage
I_C	6	Reference Set Current
V_{FB}	7	Feedback Voltage
LBD	8	Low Battery Detector Output

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Supply Voltage (without external transistor)			30	V
$P_D T_A < 50°C$			300	mW
Operating Temperature	0		70	°C
Storage Temperature	-65		150	°C
Junction Temperature			125	°C
Switch Current (peak)			200	mA
For $T_A > 50°C$ Derate at 4.2mW/°C				

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
θ_{JA}	SO8 thermal resistance		240		°C/W

DC Electrical Characteristics

$+V_S$ = +6.0V, I_C = 5.0 µA and T_A = +25°C unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
$+V_S$	Supply Voltage		2.2		30	V
V_{REF}	Reference Voltage (internal)		1.24	1.31	1.38	V
I_{SY}	Supply Current	Measure at Pin 5 I_4 = 0		215	300	µA
I_{LBD}	Low Battery Detect Output Current Drive	V_8 = 0.4V, V_1 = 1.1V	500	1500		µA
T_C	Reference Set Current		1.0	5.0	50	µA
I_{CO}	Switch Leakage Current	V_4 = 30V		0.01	5.0	µA
I_{SO}	Supply Current (disabled)	$V_C \leq$ 200mV		0.1	5.0	µA
I_1	Low Battery Detect Bias Current	V1 = 1.2V		0.7		µA
I_{CX}	Capacitor Charging Current			8.6		µA
$+V_{THX}$	Capacitor Threshold Voltage +			1.4		V
$-V_{THX}$	Capacitor Threshold Voltage –			0.5		V
I_{FB}	Feedback Input Current	V7 = 1.3V		0.1		µA

$+V_S$ = +6.0V, I_C = 5.0 µA over the full operating temperature range unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
$+V_S$	Supply Voltage		2.6		30	V
V_{REF}	Reference Voltage (internal)		1.20	1.31	1.42	V
I_{SY}	Supply Current	Measure at Pin 5 I_4 = 0		235	350	µA
I_C	Reference Set Current		1.0	5.0	50	µA
I_{CO}	Switch Leakage Current	V_4 = 30V		1.0	30	µA
I_{SO}	Supply Current (Disabled)	$V_C = \leq$ 200 mV		1.0	30	µA
I_{LBD}	Low Battery Detect Output Current Drive	V_8 = 0.4V, V_1 = 1.1V	500	1200		µA

AC Electrical Characteristics

$+V_S$ = +6.0V, I_C = 5.0 µA and T_A = +25°C unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
I_{SW}	Switch Current	V4 = 400mV	100	200		mA
eff	Efficiency			85		%
	Line Regulation	0.5 $V_{OUT} < V_S <$ V_{OUT}		0.04	0.5	%V_O
L_1	Load Regulation	V_S = 0.5 V_{OUT} P_L = 150mW		0.2	0.5	%V_O
F_O	Operating Frequency Range[1]		1.0	25	75	kHz
	Oscillator Frequency Tolerance			±10		%

Note:

1. Guaranteed by design.

PERSONAL COMPUTERS

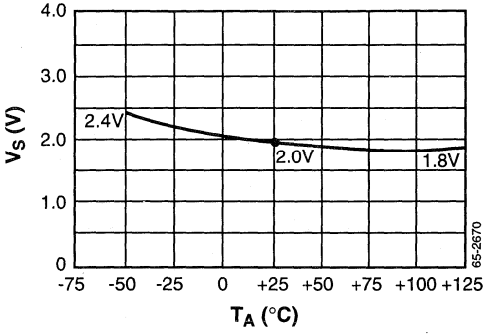
AC Electrical Characteristics (continued)

+V_S = +6.0V, I_C = 5.0 µA and over the full operating temperature range unless otherwise noted.

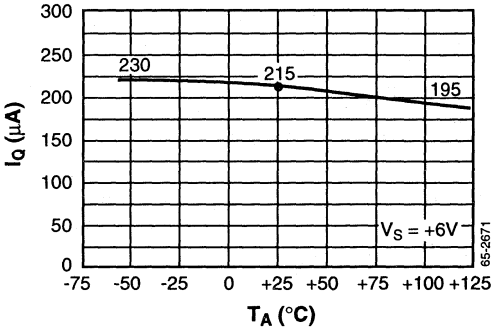
Parameter		Conditions	Min	Typ	Max	Units
	Oscillator Frequency Temperature Drift			±200		ppm/°C
	Line Regulation	0.5 V_{OUT} < V_S < V_{OUT}		0.5	1.0	%V_O
L_1	Load Regulation	V_S = 0.5 V_{OUT} P_L = 150mW		0.5	1.0	%V_O

Typical Performance Characteristics

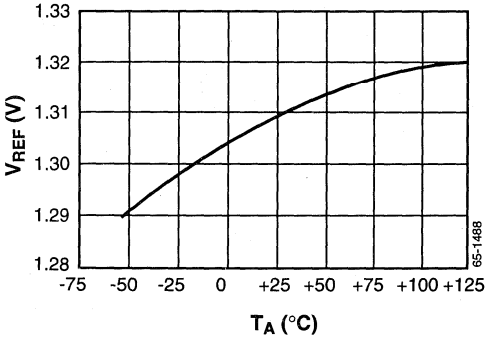
Minimum Supply Voltage vs. Temperature



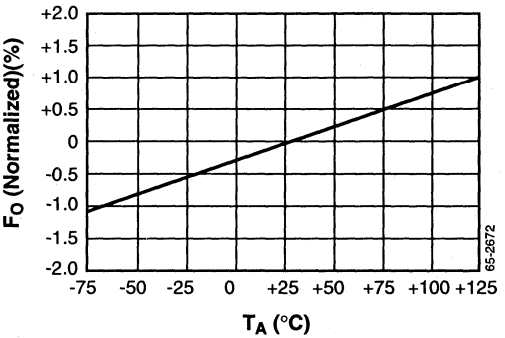
Quiescent Current vs. Temperature



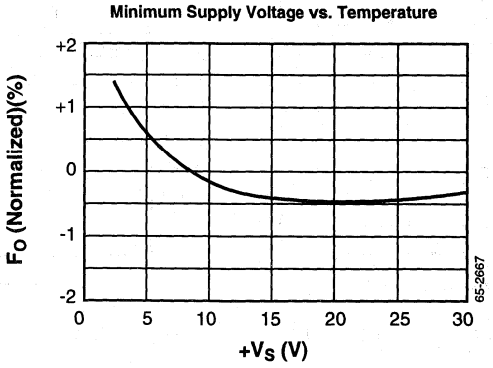
Reference Voltage vs. Temperature



Oscillator Frequency vs. Temperature



Typical Performance Characteristics (continued)



Applications Discussion

LCD Driver Application

Many hand-held electronic devices require a regulated output voltage from a battery supply source. In today's notebook computers, the battery voltage is a function of load, charge conditions, and battery age, and can vary from 6 Volts to 18 Volts. The standard voltages found in a notebook computer are 3.3V, 5V, and 12V. LCD displays require a higher voltage which is adjustable under light conditions, temperature and LCD aging effects. A user may adjust the LCD voltage conditions for better readability and screen perception of the display. This adjustment takes places from 18V to 30V. Figure 1 is a schematic based on the RC5010 step-up converter. The switching frequency of 20 kHz allows to transfer the energy on the output by stepping up the voltage from 7V (or any higher voltage) to a regulated output voltage. LCDs use current from few mA to 30mA. The Power FET isolates the output stage from leaking current when the circuit is switched in power down mode. Under power down mode, the only current used by this application is the leakage current flowing through 1M Ohm resistor connected to the switch or open collector gate. When "ON," the voltage present at pin 6 is 1.4V and will not pull the open collector (drain) to any dangerous breakdown voltage for the logic driver. Figures 2 and 3 represent the efficiency versus the output voltage, load and input voltage. This application can be used also in a PDA hand held device.

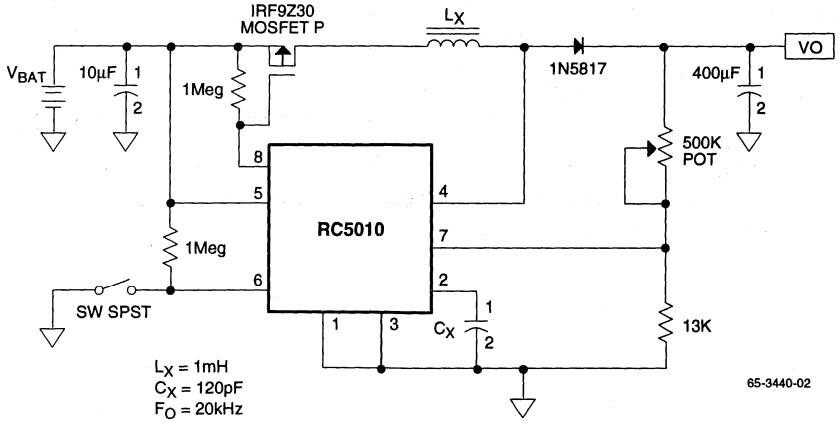


Figure 1. Adjustable Converter for Positive LCD Display Applications

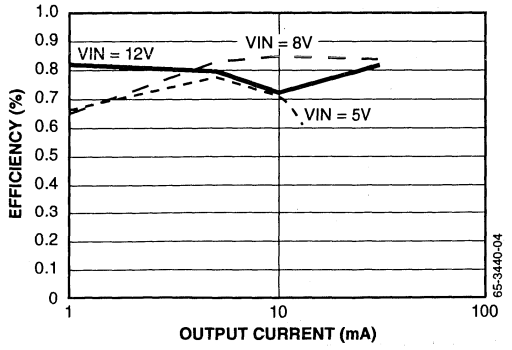


Figure 2. Efficiency vs. Output Current, V_{OUT} = 18V

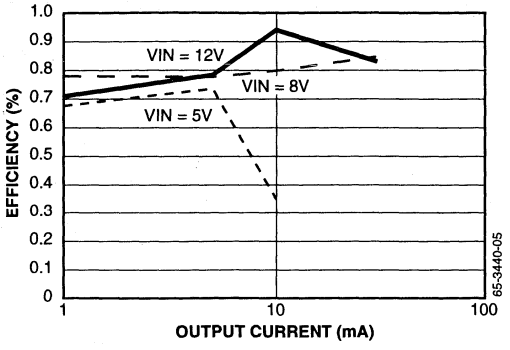


Figure 3. Efficiency vs. Output Current, V_{OUT} = 30V

5V to 12V Step-up Converter for Flash Memory Cards and PCMCIA Applications

Figure 4 is a fixed voltage regulator capable of transfering power from a 5V input voltage (or any other 3.3 to 9V battery operated device) to 12V precise voltage. A 12V regulated supply is required by notebooks on board subsystems, PCMCIA flash memory cards, and other applications found in portable equipment. RF LANs, modem-fax cards, etc. may use this device to set the proper voltage from an unregulated battery. Figures 5, 6, and 7 represent the efficiency versus the output voltage, load and input voltage.

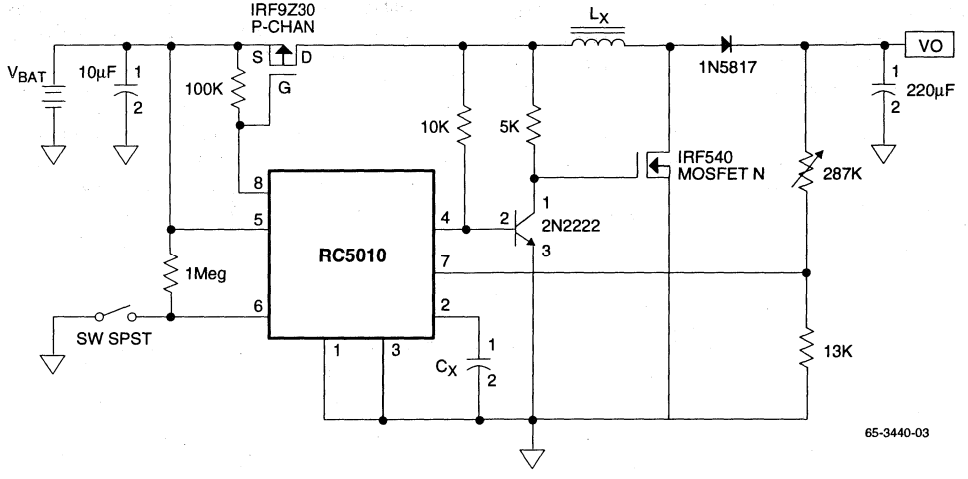


Figure 4. Fixed 12V Converter for Notebook and PDA Applications

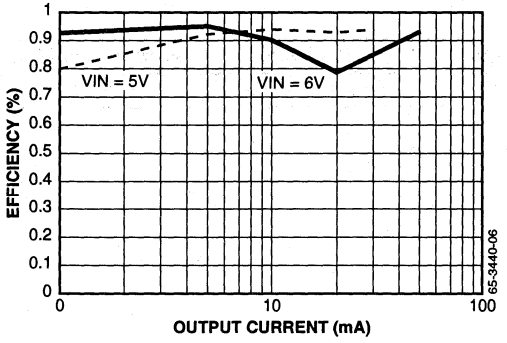


Figure 5. PCMCIA Application V_{OUT} = 12V, Efficiency vs. Output Current (No External Components)

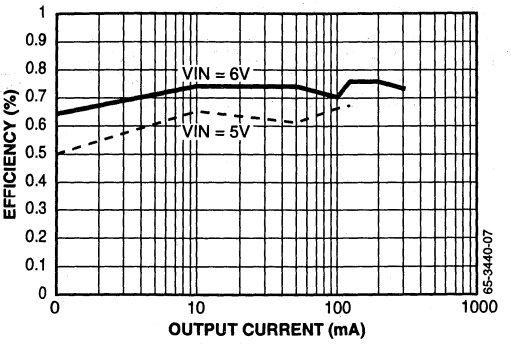


Figure 6. PCMCIA Application (External Components) V_{OUT} = 12V, Efficiency vs. Output Current

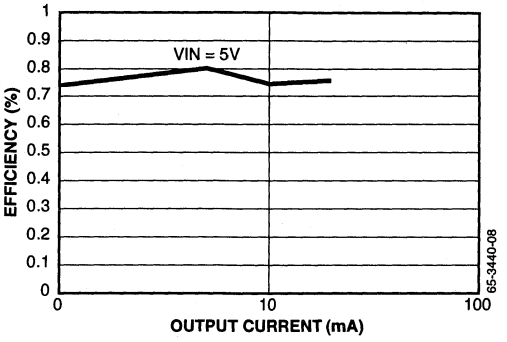


Figure 7. Efficiency vs. Output Current, VOUT = 12V

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC5010M	0° to 70°C	Commercial	8-pin Wide SOIC	RC5010M

RC5032

5V to 3.3V Step-Down DC-DC Converter

Features

- >85% Efficiency
- Fast transient response
- Soft control power-up
- Short circuit protection
- Output voltage fixed 3.3V
- Low TC reference voltage
- Adjustable oscillator frequency
- Drives N-Channel MOSFET
- 8 pin SOIC, 8 pin DIP package

Applications

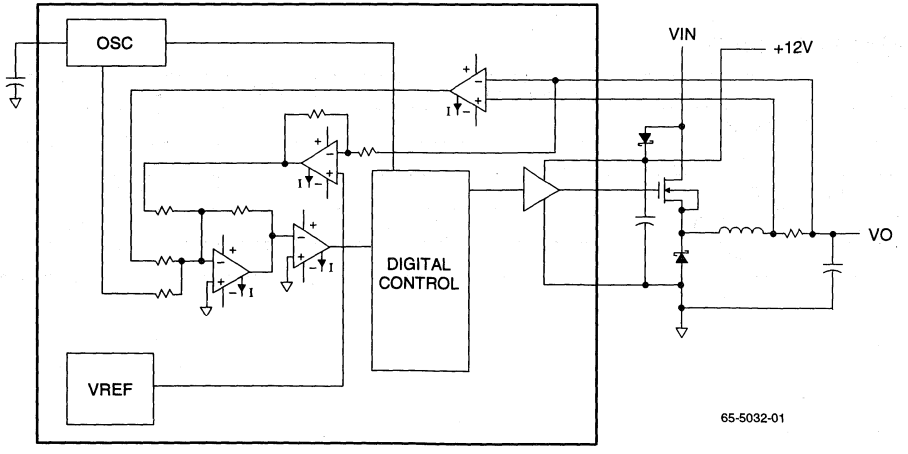
- 3.3V power supply for Pentium™ based desktop CPU motherboards
- Minimum component DC-DC converters

Description

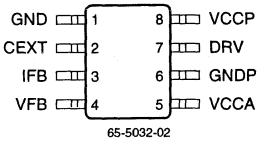
The RC5032 is a step-down DC-DC controller IC dedicated to providing a 5V to 3.3V conversion for various types of CPU power. It can be configured with the proper applications circuitry to deliver load currents greater than 10 Amps. The RC5032 is designed to operate in a standard PWM control mode under heavy load conditions and as a PFM controller in light load conditions. Its highly accurate low TC reference eliminates the need for precision external components in order to achieve tight tolerance voltage regulation.

The programmable oscillator can operate from 200KHz to greater than 1MHz to provide for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs.

Block Diagram



Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
GND	1	Ground
CEXT	2	External capacitor for setting oscillator frequency
IFB	3	Current Feedback Input
VFB	4	Voltage Feedback Input
VCCA	5	Analog VCC
GNDP	6	Power ground for high current driver
DRV	7	FET Driver Output
VCCP	8	VCC for FET output drivers

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
VCCP	Driver Supply				13	V

Note:

1. Functional operation under any of these conditions is NOT implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
VCC	Supply Voltage		4.5	5	7	V
VCCP	Driver Supply		9		13	V
VIH	Input Voltage, Logic HIGH		2			V
VIL	Input Voltage, Logic LOW				0.8	V
	Ambient Temp		0		70	°C

DC Electrical Characteristics

(V_{CC} = 5V, Fosc = 650 KHz, and T_A = 0–70°C)

Parameter		Conditions	Min	Typ	Max	Units
V_O	Output Voltage		3.1	3.4	3.6	V
I_O	Output Current	See Figure 1 for application		7		A
Vref Acc	Reference Accuracy			1	3	%
VTC	Output Voltage TC			40		ppm
LDR	Load Regulation	0.5 to 7A		0.5		%V_O
LIR	Line Regulation	V_{CC} = ±5%		0.07		%V_O
V_R	Output Voltage Ripple			30		mV
Cum Acc	Cumulative Accuracy[1]	T_A = 0–70°C		3	5	%
Eff	Efficiency	Iload > 4A	85	88		%
Iodr	Output Driver I	Open Loop	0.5	0.7		A
Pd	Power Dissipation			0.1		W

Notes:

1. Output Voltage accuracy, Tempco, load regulation, ripple, and transient performance determine the Cumulative Accuracy.

AC Electrical Characteristics

(V_{CC} = 5V, Fosc = 650 KHz, and T_A = 25°C)

Parameter		Conditions	Min	Typ	Max	Units
Tr	Response Time	Il=0.5A to 7A		10		µs
Fosc	Oscillator Range		0.2		1.2	MHz
Osc Acc	Fosc Accuracy			10		%
Dtc	Max Duty Cycle	PWM mode	90	95		%
Dtcm	Min Duty Cycle	PFM mode			100	ns
Iscp	Short Circuit Prot			250		mV
Trimax	Response to Imax			15	30	µs
Tssp	Soft start response			1		ms

Test Circuit

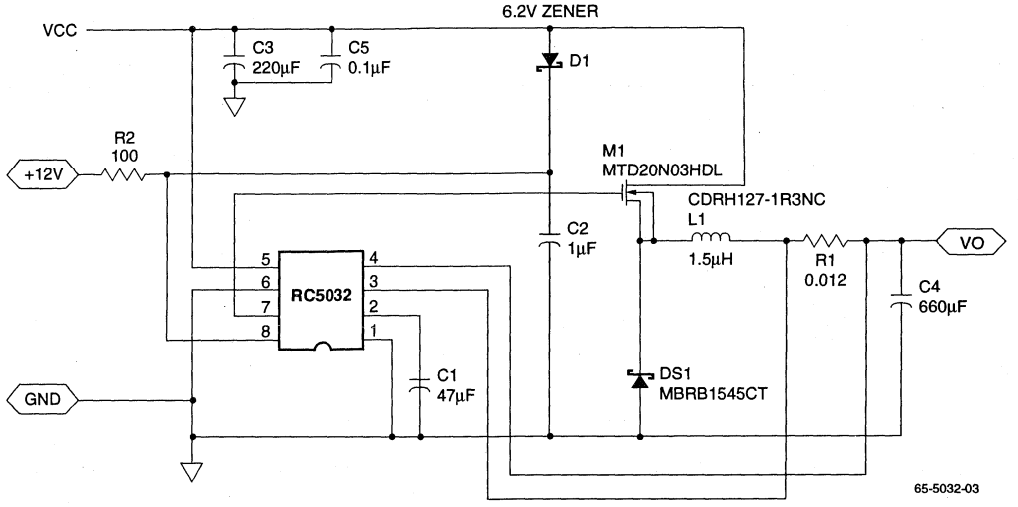


Figure 1. RC5032 7A Schematic

Table 1. Components for RC5032

RC5032 Standard Application Circuit Bill of Materials			
Ref Designator	**Quantity**	**Part No.**	**Manufacturer**
L1	1	CDRH127-1R3NC	Sumida
M1	1	MTD20N03HDL	Motorola
DS1	1	MBRB1545CT	Motorola
D1	1	6.2V Zener	any
R1	1	LRC-2512	IRC
C3	1	OS-CON 10SA220M	Sanyo
C4	2	OS-CON 10SA330M	Sanyo
C2	1	1uF	Monolithic ceramic Cap
C1	1	47pF	SMD Cap
C5	1	0.1uF	SMD Cap
R2	1	100Ω	SMD Res

Ordering Information

Product Number	Package	θJA
RC5032M	8 SOIC	85°C/W

RC5033

Adjustable Synchronous DC-DC Converter

Features

- >85% Efficiency
- 350uA quiescent current in shutdown
- Fast transient response
- Soft control power-up
- Over-Voltage Protection
- Output voltage range from 2.0V to 3.6V
- Factory trimmed low TC reference voltage
- Adjustable oscillator frequency
- Drives N-Channel MOSFETs
- 16 pin SOIC package

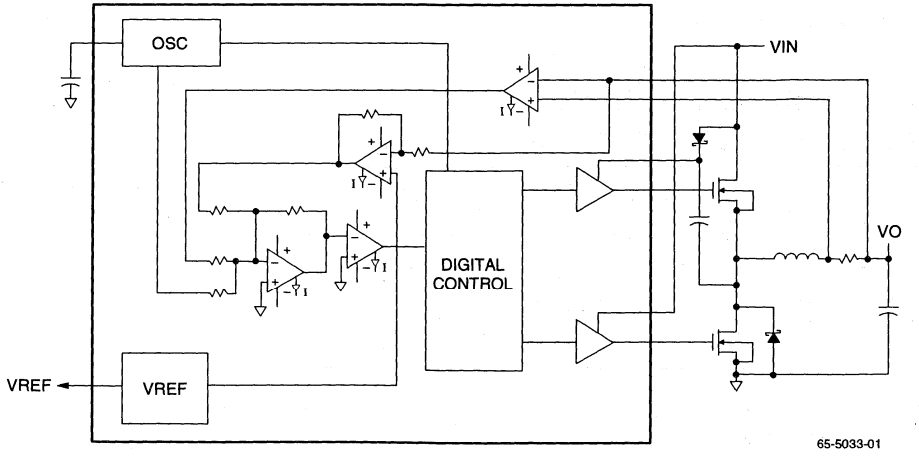
Applications

- 3.3V power supply for Pentium™ based CPU motherboards
- 3.45V power supply for AMD-K5™ CPU
- 2.5V or 3.6V power supply for PowerPC™

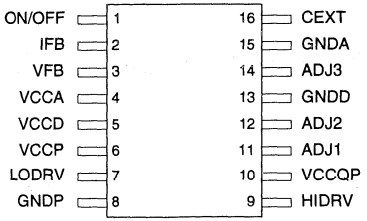
Description

The RC5033 is a synchronous mode DC-DC controller IC dedicated to providing a 5V to 2.0V up to 3.6V conversion for various types of CPU power . It can be configured in both the synchronous and non-synchronous modes and with the proper applications circuitry can be used to deliver load current greater than 10 Amps. The RC5033 is designed to operate in a standard PWM control mode under heavy load conditions and as a PFM controller in light load conditions. Its highly accurate low TC reference eliminates the need for precision external components in order to achieve tight tolerance voltage regulation. Through the use of external resistors, the RC5033 can generate accurate output voltages from 2.0V up to 3.6V. An integrated Over-Voltage protection function constantly monitors the output voltage and shuts down the power to the CPU in the event of a out-of-tolerance voltage situation, thereby protecting the CPU. The programmable oscillator can operate from 200KHz to greater than 1MHz to provide for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs.

Block Diagram



Pin Assignments



65-5033-02

Pin Definitions

Pin Name	Pin Number	Pin Function Description
On/Off	1	A low level on this pin will power down; tie to VCCD if not used.
IFB	2	Current Feedback Input.
VFB	3	Voltage Feedback Input.
VCCA	4	Analog VCC.
VCCD	5	Digital VCC.
VCCP	6	VCC for synchronous FET output drivers.
LODRV	7	Synchronous FET driver output.
GNDP	8	Power ground for high current drivers.
HIDRV	9	High side FET driver output.
VCCQP	10	VCC for High side FET output driver
ADJ1	11	VREF adjust pin.[1]
ADJ2	12	VREF adjust pin.[1]
GNDD	13	Digital ground.
ADJ3	14	VREF adjust pin.[1]
GNDA	15	Analog ground.
CEXT	16	External capacitor for setting oscillator frequency.

Note:
1. See voltage adjust table for function

Output Voltage Selection Table

VOUT	ADJ1	ADJ2	ADJ3
3.5V	N/C	N/C	N/C
3.35V	N/C	[2]	[2]
3.3V	[2]	N/C	[2]
2.9V[1]	3.9K	N/C	N/C
2.5V[1]	2K	N/C	N/C
2.0V[1]	39Ω	N/C	N/C

Note:
1. See Figure 3 for resistor connection.
2. Indicated short pins together.

Preliminary Information

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
V_{CCP}	Driver Voltage				13	V
V_{CCQP}	High Driver Supply				13	V
T_J	Junction Temperature				175	°C
T_A	Ambient Operating Temperature		0		70	°C
T_S	Storage Temperature		-65		150	°C
T_L	Lead Soldering Temperature	(10 seconds)			300	°C

Note:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5	7	V
V_{CCP}	Low Driver Supply		4.5	5	12	V
V_{CCQP}	High Driver Supply		9		13	V
V_{IH}	Input Voltage, Logic HIGH		2			V
V_{IL}	Input Voltage, Logic LOW				0.8	V

PERSONAL COMPUTERS

DC Electrical Characteristics

(V_{CC} = 5V, fosc = 650 KHz, and T_A = +25°C unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Units
V_O	Output Voltage	Nominal, Pin 12 conn. Pin 14, T_A = 0–70°C	3.135	3.3	3.465	V
I_O	Output Current	See Figure for application		5		A
Vref Acc	Voltage Reference Accuracy			1		%
VTC	Output Voltage Tempco			-40		ppm
LDR	Load Regulation	0.5 to 7A		1		%Vo
LIR	Line Regulation	V_{CC} = ±5%		0.14		%Vo
V_R	Output Voltage Ripple			30		mV
Cum Acc	Cumulative Accuracy[2]	T_A = 0–70°C		3		%
Eff	Efficiency	Synchronous mode > 1A	80	85		%
Iodr	Output Driver I	Open Loop	0.5	0.7		A
PD	Power Dissipation			0.1	0.2	W

Notes:

1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.
2. Output Voltage accuracy, Tempco, load regulation, ripple, and transient performance determine the Cumulative Accuracy.

AC Electrical Characteristics[1]

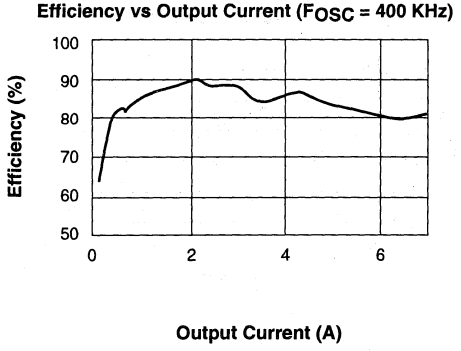
(T_A = +25°C unless otherwise noted)

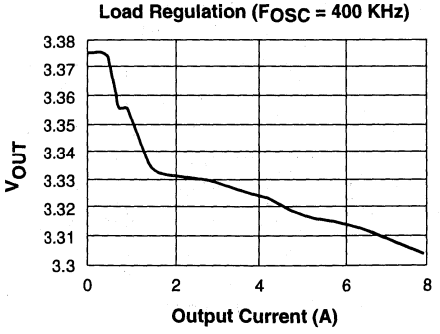
Parameter		Conditions	Min	Typ	Max	Units
Tr	Response Time	Il=0.5A to 5.5A		10		µs
Fosc	Oscillator Range		0.2		1.2	MHz
Osc Acc	Fosc Accuracy			10		%
Dtc	Max Duty Cycle	PWM mode	90	95		%
Dtcm	Min Duty Cycle	PFM mode			100	ns
Imax	Imax Threshold			30		mV
Iscp	Short Circuit Prot			80		mV
Ovp	Over Voltage Prot			20		%Vo
Trimax	Response to Imax			15	30	ns
Tssp	Soft start response			10		µs

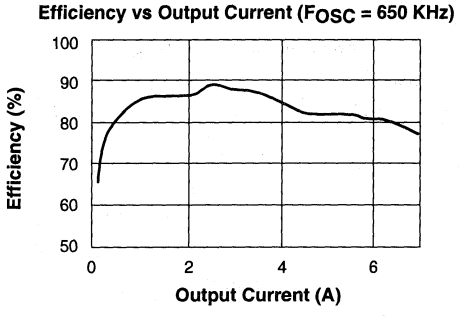
Note:

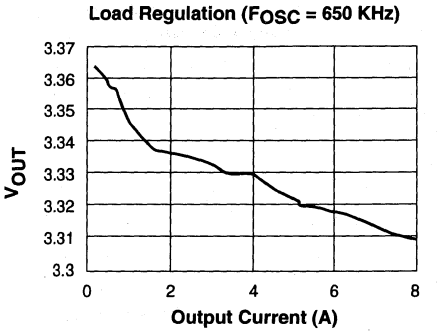
1. Guaranteed by design, not 100% total.

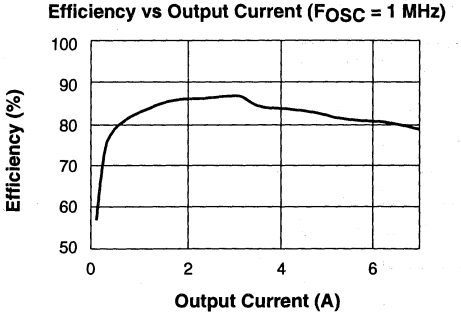
Typical Operating Characteristics[1]

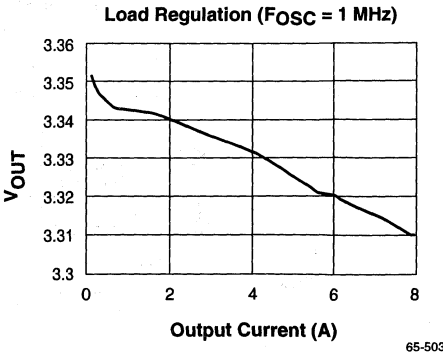












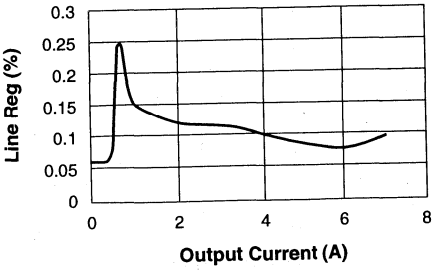
65-5033-03

Note:

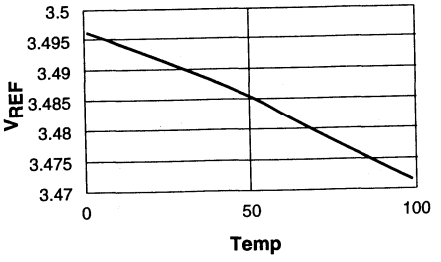
1. Data taken with circuit of Figure 1.

Typical Operating Characteristics (continued)

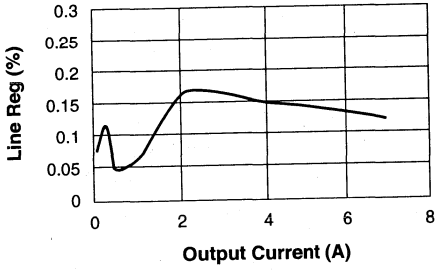
Line Regulation vs. Output Load (F_{OSC} = 400 KHz)



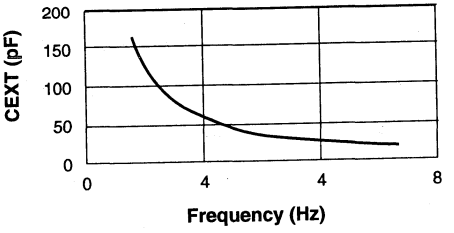
Reference Tempco



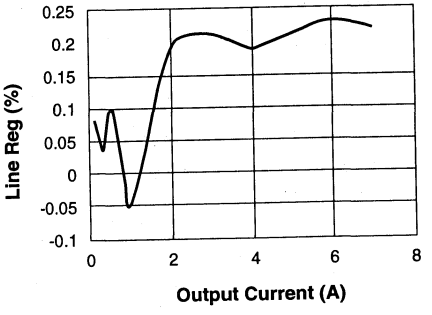
Line Regulation vs. Output Load (F_{OSC} = 650 KHz)



CEXT vs. Oscillator Frequency



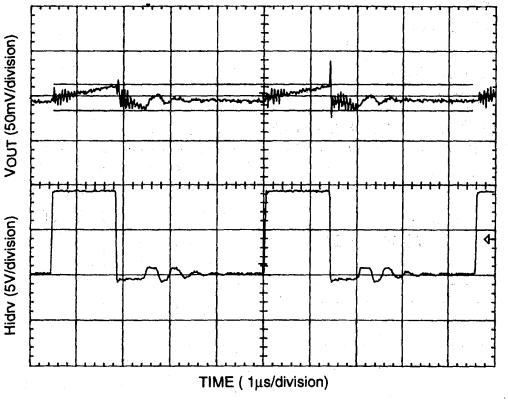
Line Regulation vs. Output Load (F_{OSC} = 1 MHz)



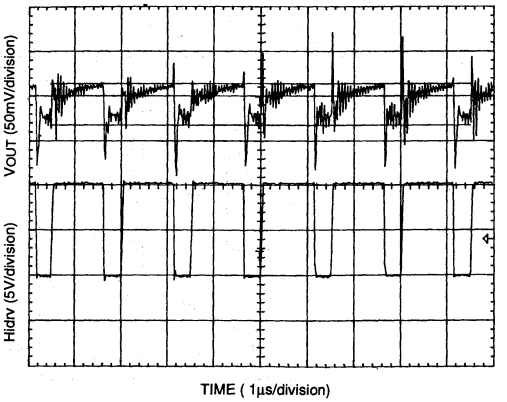
65-5033-04

Preliminary Information

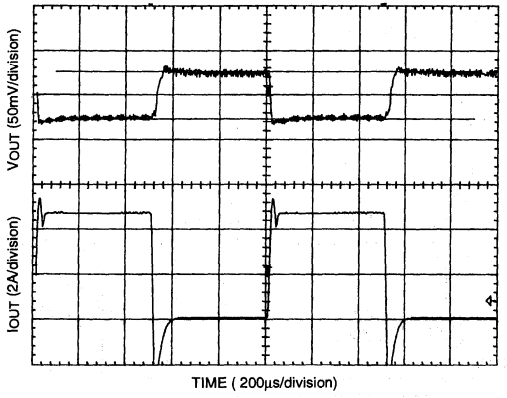
Typical Operating Characteristics (continued)



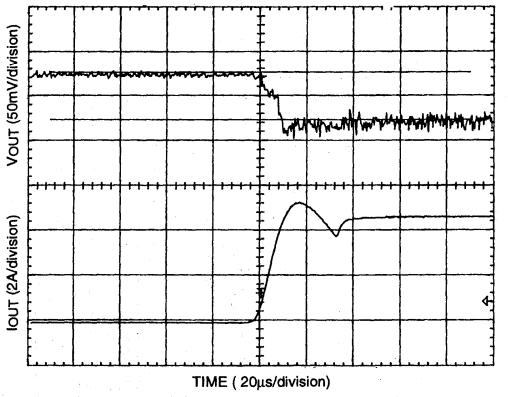
AC Ripple response .2A Load



AC Ripple response 5A Load



Transient Response .2A to 5A Load



Transient Response Magnified

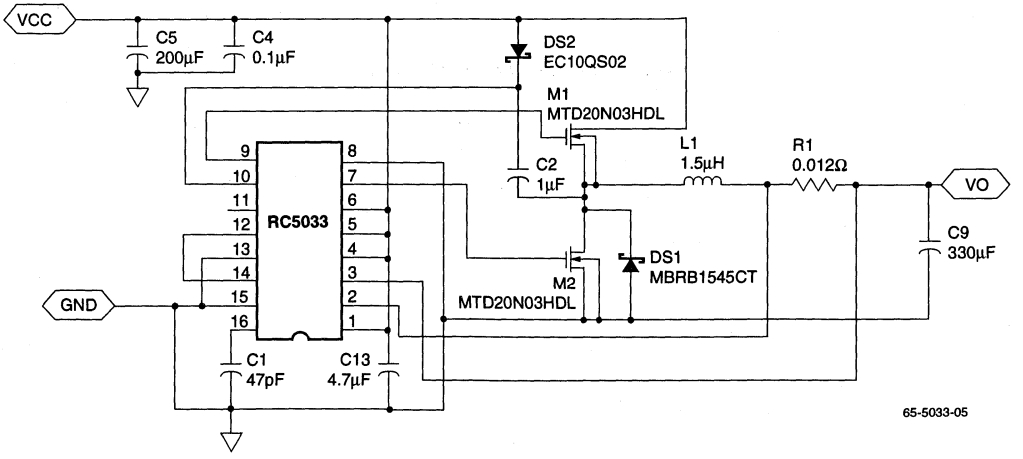


Figure 1. Standard 7A Application Schematic

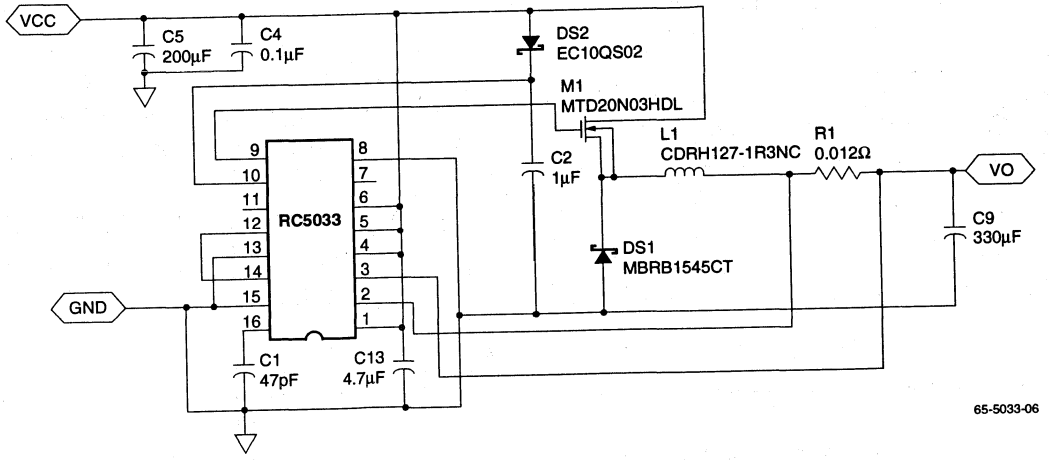


Figure 2. Non-Synchronous 7A Application Circuit

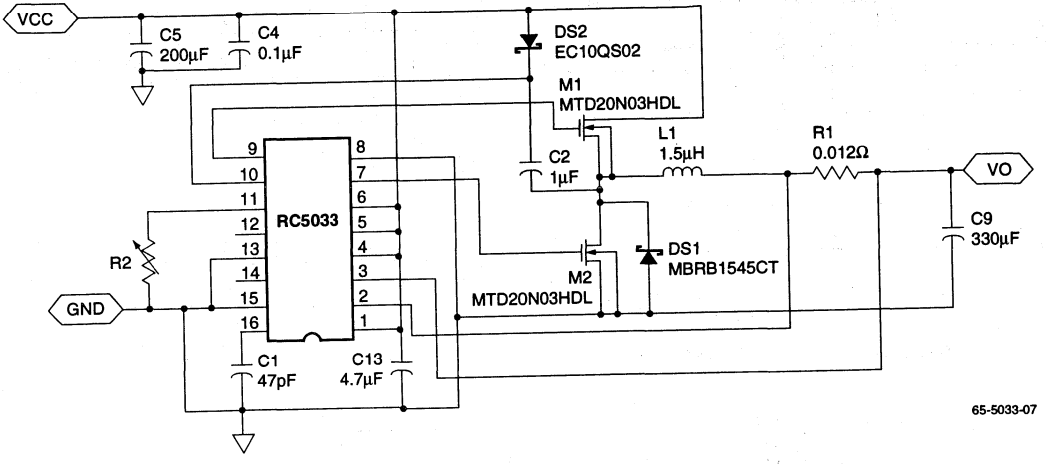


Figure 3. Adjustable Voltage DC-DC Converter

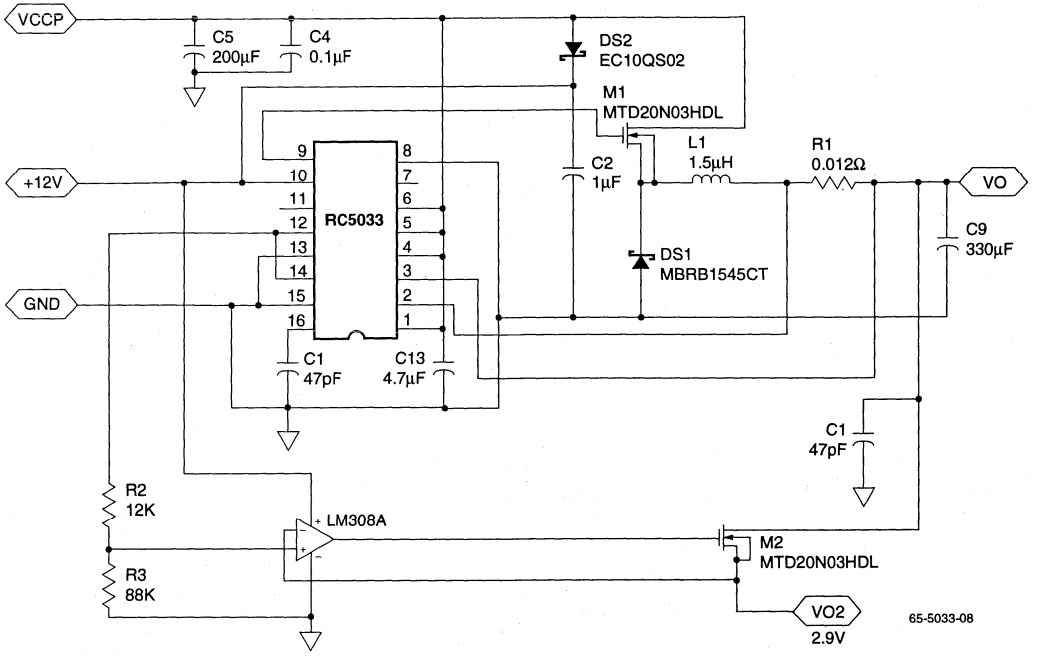
RC5033 Standard Application Circuit Bill of Materials			
Ref Designator	**Quantity**	**Part No.**	**Manufacturer**
L1	1	CDRH127-1R3NC	Sumida
M1,M2	2	MTD20N03HDL	Motorola
DS1	1	MBRB1545CT	Motorola
DS2	1	EC10QS02L	Nihon
R1	1	LRC-2512	IRC
C5	1	OS-CON 10SA220M	Sanyo
C9	1	OS-CON 10SA330M	Sanyo
C2	1	1uF	Monolithic ceramic Cap
C1	1	47pF	SMD Cap
C4	2	0.1uF	SMD Cap

Table 1. Components for RC5033

RC5033 Alternate Suppliers of Components			
Ref Designator	Quantity	Alternate Part No.	Alternate Manufacturer
L1	1	PE-53680	Pulse Engineering
M1,M2	2	2SK1388	Fuji
		IRLZ44N	International Rectifier
		Si4410DY	Temic (Siliconix)
DS1	1	C10T02QL	Nihon
		SR1620C	Rectron
DS2	1	MBRS140T3	Motorola
R1	1	WSL-2512	DALE
C5	1		
C9	1		

Table 2. Alternate Components Selection

Applications Discussion



Dual Power Supply Application

In some CPU power applications there may be a need for a split voltage converter. The circuit in Figure 4 addresses this need with only minimal component count. The basic RC5033 non-synchronous DC-DC converter is augmented with an op-amp, a power MOSFET, and some 1% resistors to provide a dual power supply with one voltage set to 3.3V and the other, slaved off of the 3.3V, set to 2.9V. In this configuration, the RC5033 converts the 5V to 3..3V with high efficiency. By using the op-amp, power FET, and the resistors, a low-dropout linear regulator is realized that can be run off of the 3.3V. The 2.9V linear regulator has a relatively high efficiency just due to the fact that the ratio of 2.9V/3.3V is close to 88%. The power FET is a low Rdson n-channel MOSFET, and thus it is reasonably inexpensive. The opamp can be a garden variety, though the input bias current and output slew rate need to be considered to optimize accuracy and transient response. The overall efficiency of this power supply system will very much depend upon the percentage of power used on each power output. Overall, the efficiency of this system will be lower than if both supplies were implemented as switchers; however, the added savings of the part count reduction may more than compensate for the overall lower efficiency.

Standard Application Circuit

The circuit shown in Figure 1 along with its components and values has been designed as representative of the typical application involving the RC5033 for a Pentium™ CPU. Use of the standard application circuit will deliver the performance curves shown under the Typical Operating Characteristics section of the data sheet. Many users will want to develop their own DC-DC converter solution that is uniquely tailored to a specific application requirement. In that case, the users should review the detailed information in the Design Procedure and Applications Information section of the data sheet.

Detailed Description

The RC5033 is a programmable voltage synchronous controller. When designed around the appropriate external components, it can be configured to deliver more than 10A of output current. During heavy loading conditions the RC5033 functions as a current-mode PWM step down regulator. Under light loading conditions, the regulator functions in the PFM or pulse skipping mode, thereby increasing its efficiency under light loads.

Main Control Loop

The main control loop of the regulator (see Block Diagram) contains two main blocks, the analog control block and the digital control block. The analog control block consists of signal conditioning amplifiers that feed into a set of fast comparators which provide the inputs to the digital control block. The signal conditioning block takes inputs from the IFB(current feedback) and VFB(voltage feedback) pins and then sets up two controlling signal paths. The voltage control path gains up the VFB signal and presents that signal to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents that signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator and the output is then presented to a comparator. This comparator provides the main PWM control signal to the digital control block.

There are three other comparators in the analog control block. The first two control the thresholds of where the RC5033 goes into its pulse skipping mode during light loads and the second controls the point at which the max current comparator disables the output drive signal to the upper power MOSFET. The third comparator determines when the synchronous mode bottom side power MOSFET will be enabled and disabled.

The digital controller section is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV and LODRV output pins that will in turn control the external power MOSFETs. This digital section was designed in high speed schottky transistor logic which allows the RC5033 to clock up to speeds greater then 1MHz. This section is responsible for providing the break-before-make timing that ensures that both external FETs will not be on at the same time.

High Current Output Drivers

The RC5033 contains two identical high current output drivers. These drivers contain high speed bipolar transistors configured in a push-pull configuration. Each output driver is capable of pumping out 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for added switching noise immunity. The HIDRV driver has a power supply, VCCQP, which can be either derived from an external voltage source or can be boot-strapped from a flying-capacitor as is shown in Figure 1. In the boot-strapped mode, C2 is alternately charged from VCC via the schottky diode DS2 and then boosted up when M1 is turned on. This provides a VCCQP voltage equal to 2*VCC - Vds(DS2); or about 9.5V with VCC=5V. This voltage is sufficient to provide the 9V gate drive to the external MOSFET that will be needed for achieving a low Rdson. Since the low side synchronous FET is referenced to ground, there is no need to boost the gate drive voltage and its VCCP power pin can just be tied to VCC.

Internal Reference

The reference in the RC5033 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. For applications that require a voltage other than the voltages provided by the fixed jumper connections, an external resistor will change the reference voltage from 2.0V up to 3.6V. For a guaranteed stable operation under all loading conditions, a 0.1µF capacitor is recommended on the VREF output pin.

Over -Voltage Protection

The RC5033 provides a constant monitor of the output voltage for over-voltage protection. Should the voltage at the VFB pin exceed 20% of the selected program voltage, then an overvoltage condition will be assumed to exist and the RC5033 will shut down the output drive signals to the power FETs.

Oscillator

The RC5033 oscillator is designed as a fixed current capacitor charging oscillator. An external capacitor allows for maximum flexibility in choosing the associated external components for the RC5033. The oscillator frequency con be set from less than 200KHz to over 1MHz depending on the application requirements.

PERSONAL COMPUTERS

Design Procedure and Applications Information

Simple Step-Down Converter

Figure 4 shows a step-down DC-to-DC Converter with no feedback controller. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5033 in Figure 1. In Figure 5, the basic operation begins by closing the switch, S1. When S1 is closed the input voltage VB is impressed across the inductor L1. The current flowing in the inductor is given by the following equation: IL=(VB- Vo)Ton/L; where Ton is the time duration for S1 to be closed. When S1 is open, the diode will conduct the inductor current and the output current will be delivered to the load according to the equation: IL=Vo(T – Ton)/L; where T- Ton is the time duration for S1 to be off. By solving these two equations we can arrive at the basic relationship for the output voltage of a step-down converter: Vo= VB(Ton/T).

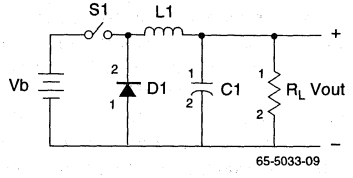


Figure 5. Simple Buck DC-DC Converter

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-to-DC converter application. The critical parameters are inductance (L), max DC current (Imax), and the coil resistance (Rl). The inductor core material is a critical factor in determining the amount of current that the inductor will be able to handle. As with all engineering designs there are trade- offs for various types of inductor core materials. In general, Ferrites are popular because of their low cost, low EMI, and high frequency (>500kHz) characteristics. Molypermalloy powder (MPP) materials have good saturation characteristics and low EMI with low hysteresis losses; however they tend to be expensive and are more efficiently utilized at frequencies below 400kHz. DC winding resistance is another critical parameter. In general, the DC resistance should be kept as low as possible. The power loss in the DC resistance will degrade the efficiency of the converter by the relationship: Power Loss = (Io)2*Rl.

The value of the inductor is a function of the switching frequency (Ton) and the maximum inductor current. The max inductor current can be calculated from the relationship:

$$I_{MAX} = \frac{2I_L}{F_O T_{ON}\left(\frac{V_{IN} - V_{OUT}}{V_{OUT} - V_D}\right) + 1}$$

Where: Fo is the desired clock frequency
Ton is the max on time of the M1 FET
Vd is the forward voltage of the schottky diode D1

Then the inductor value can be calculated with the relationship:

$$L = \frac{V_{IN} - V_{DSON}}{I_{MAX}}(T_{ON})$$

Where: Vdson is the voltage across the drain-source of the M1 FET when switched on.
(this can be calculated by RDSon * Imax)

Current-Sense Resistor

The current sense resistor will carry all of the peak current of the inductor. This current will be more than the designed for load current. The RC5033 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds 100mV. When this happens the output voltage will temporarily go out of regulation. As the voltage across the resistor becomes larger, the top-side FET will turn off more and more until the current limit value is reached and then the RC5033 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is advisable. Thus the resistor should be set by the relationship:

R = 100 mV/ Ipeak

Where: Ipeak = Imax * 1.33

Since the value of the sense resistor is generally in the miliohm region, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFB and VFB pins of the RC5033 should be Kelvin connected to the pads of the current-sense resistor as shown in the sample layout Figure 5. To minimize the influence of noise the two traces should be run next to each other and the pins should be bypassed with a .1uF to GND as close to the device pins as possible.

Filter Capacitors

Good ripple performance and transient response are functions of the filter capacitors. Since the 5V input for a PC motherboard can be located several inches away from the DC-to-DC converter, input capacitance can play an important role in the load transient response of the RC5033. In general, the higher the input capacitance, the more charge storage is available for improving the current transfer through the top-side FET. A good rule of thumb is that for each watt of output power that you wish to deliver, there should be around 10uF of input capacitance. Low "ESR" capacitors are best suited for this application and can have an influence on the converter's efficiency. The input capacitor should be placed as close to the drain of the top-side FET as possible to reduce the effect of ringing that can be caused by large trace lengths.

The ESR rating of a capacitor is a difficult number to pin down. ESR or Equivalent Series Resistance, is defined at the resonant impedance of that capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for it to have an associated resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained with the following equation: ESR = Pd/2pfC. Where Pd is the capacitor's dissipation factor and f is the frequency of measure and C is the capacitance in farads.

With this in mind, calculating the output capacitance correctly is crucial to the performance of the DC-to-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and the transient load response. The calculation uses the following equation:

$$C(\mu F) = \frac{T_{ON}\left(\frac{(V_{IN} - V_{OUT})I_{MAX}}{V_{OUT}} + I_L\right)}{V_r}$$

Where: Vr is the desired output ripple voltage

Schottky Diode Selection

The application circuit diagram shows two schottky diodes, DS1 and DS2. DS1 is used in parallel of M2 in order to prevent the lossy body diode in the FET from turning on. DS2 serves a dual purpose. As it is configured, it allows the VCCQP supply pin of the RC5033 to be bootstrapped up to

9V by using the bootstrap capacitor C2. When the lower FET M2 is turned on, one side of the capacitor C2 is connected to GND while the other side of the cap is being charged up through D2 to a voltage that is Vin - Vd. When the lower FET turns off and the upper one turns on, the voltage that is supplied to the VCCQP pin is 2Vin - Vd. The voltage then that is applied to the gate of the FET is VCCQP - Vsat, typically around 9V. It is important in the selection of DS1 and DS2 that they have a low forward voltage drop as this directly affects the regulator efficiency. The other job that DS2 performs is that of bootstrapping VCCQP during startup. It is possible to cause the output stage to latchup if the VCCQP supply is brought up before the other VCC supplies of the RC5033. It is therefore advisable that DS2 be connected even in applications that do not utilize the bootstrapping technique for VCCQP. An alternate application could tie the VCCQP supply pin to the +12V power supply in the PC, thus eliminating the need for C2 and forcing the Rdson of M1 even lower by increasing its Vgs.

MOSFET Switches

The MOSFET switches in the RC5033 applications circuit are N-channel "logic-level" FETs. This means that they will be fully on with a Vgs of 4V. Many manufacturers make logic-level FETs and the trick is to choose the one with the lowest RDSon at the given Imax current level. The value of RDSon directly enters into the efficiency equation as a power loss. Also influencing the efficiency is the gate charge of the FET and the clock frequency of the RC5033. At higher clocking rates the amount of charge needed to be delivered to the FET is going to lower the overall efficiency. In higher current applications, the upper FET can be paralleled to provide greater current capability; however, the lower FET doesn't necessarily have to be doubled since it is on only a fraction of the time that the upper FET is on.

PCB Layout and Grounding

As is the case with most analog circuitry, good layout practices are necessary to achieve the optimum in the overall performance of the DC-to-DC converter. In general, it is always a good practice to have a tight layout that attempts to minimize short low inductance wiring to the RC5033.

The use of multilayer PCB is recommended. In particular, it is recommended to have a continuos ground plane beneath the circuit, 2oz copper would be preferred in high current applications. As was stated previously, the current-sense resistor, R1, should be located as close to the RC5033 as possible and the IFB and VFB traces should be Kelvin connected to the pads of R1. To minimize switching losses and noise, place M1, M2, L and DS2 as close together as possible. Also try to keep the HIDRV and LODRV gate drive signal traces as short as possible. It is recommended that the noisy switching part of the circuit be kept away from the low current pins on the chip such as IFB, VFB, ADJ3, ADJ1, and CEXT. Keep the 0.1uF bypass capacitors as close to the chip pins as possible. All of the ground pins should be connected to the ground plane directly under the chip. A sample layout is provided in Figure 6.

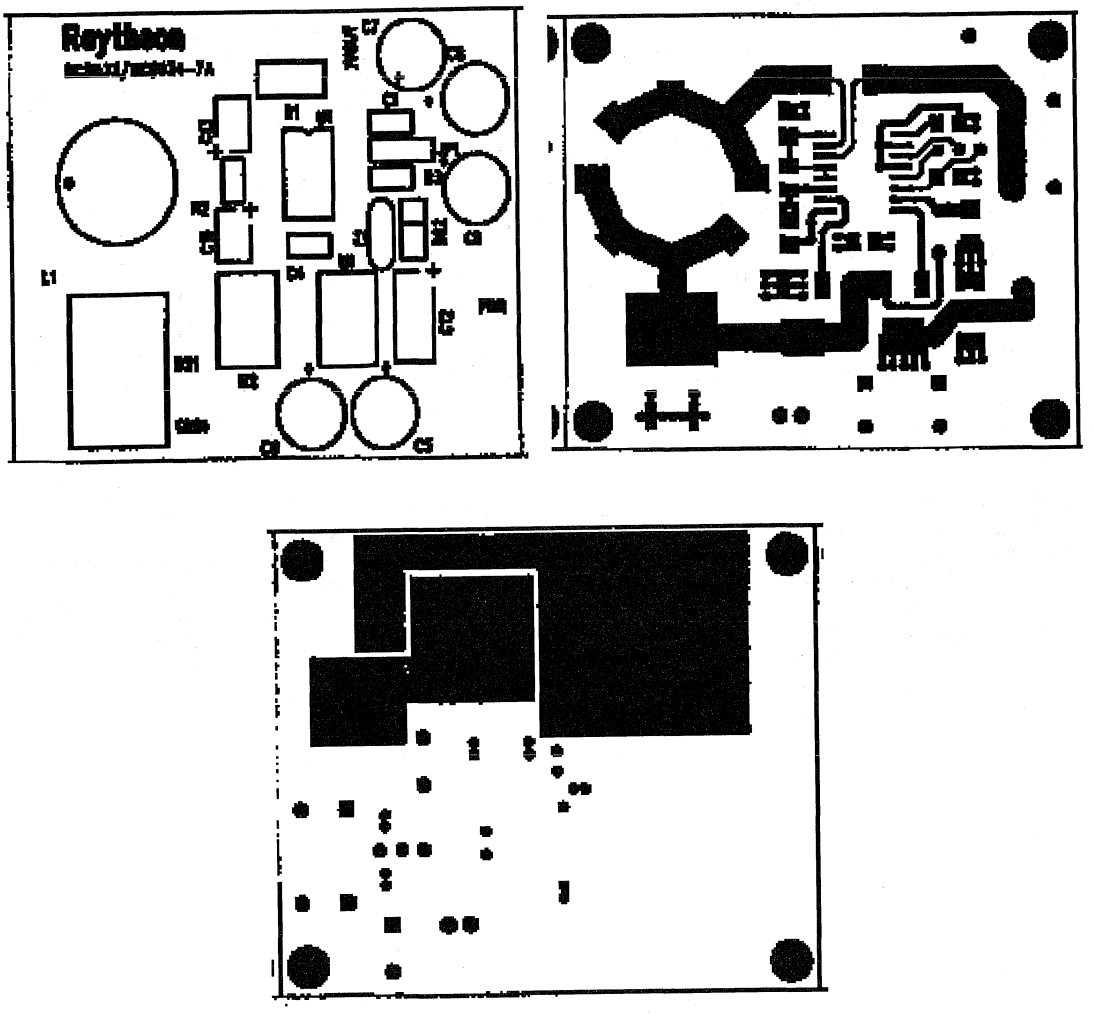


Figure 6. Sample PCB Layout

Ordering Information

Product Number	Package	θJA
RC5033M	16 SOIC	85°C/W

RC5034

High Accuracy Synchronous DC-DC Converter

Features

- Pentium™ VREF; 2% accuracy
- >85% Efficiency
- 350uA quiescent current in shutdown
- Fast transient response
- Soft control power-up
- Over-Voltage Protection
- Factory trimmed low TC reference voltage
- Adjustable oscillator frequency
- Drives N-Channel MOSFETs; to 1 MHz
- 16 pin SOIC package

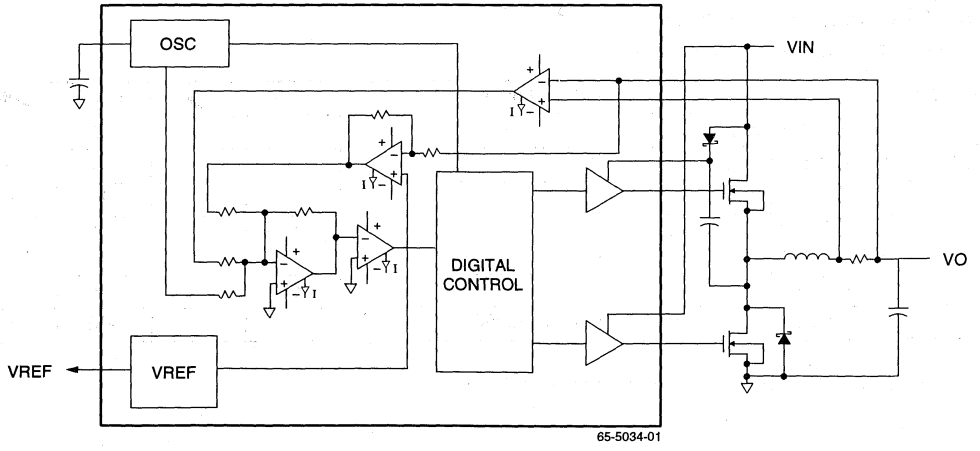
Applications

- 3.3V power supply for Pentium™ based CPUs requiring 2% VRE specification motherboards

Description

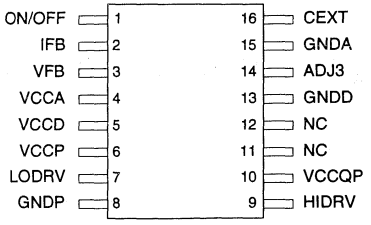
The RC5034 is a synchronous mode DC-DC controller IC dedicated to providing a 5V to 3.52V conversion for Pentium™ CPUs that require the 2% VRE voltage specification. It can be configured in both the synchronous and non-synchronous modes and with the proper applications circuitry can be used to deliver load current greater than 10 Amps. The RC5034 is designed to operate in a standard PWM control mode under heavy load conditions and as a PFM controller in light load conditions. Its highly accurate low TC reference eliminates the need for precision external components in order to achieve tight tolerance voltage regulation. An integrated Over-Voltage protection function constantly monitors the output voltage and shuts down the power to the CPU in the event of a out-of-tolerance voltage situation, thereby protecting the CPU. The programmable oscillator can operate from 200KHz to greater than 1MHz to provide for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs.

Block Diagram



65-5034-01

Pin Assignments



65-5034-02

Pin Definitions

Pin Name	Pin Number	Pin Function Description
On/Off	1	A low level on this pin will power down; tie to VCCD if not used.
IFB	2	Current Feedback Input.
VFB	3	Voltage Feedback Input.
VCCA	4	Analog VCC.
VCCD	5	Digital VCC.
VCCP	6	VCC for synchronous FET output drivers.
LODRV	7	Synchronous FET driver output.
GNDP	8	Power ground for high current drivers.
HIDRV	9	High side FET driver output.
VCCQP	10	VCC for High side FET output driver
NC	11, 12	No Connections leave open
GNDD	13	Digital ground.
ADJ3	14	VREF
GNDA	15	Analog ground.
CEXT	16	External capacitor for setting oscillator frequency.

Preliminary Information

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
V_{CCP}	Low Driver Supply				13	V
V_{CCQP}	High Driver Supply				13	V
T_J	Junction Temperature				175	°C
T_A	Ambient Operating Temperature		0		70	°C
T_S	Storage Temperature		-65		150	°C
T_L	Lead Soldering Temperature	(10 seconds)			300	°C

Note:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5	7	V
V_{CCP}	Low Driver Supply		4.5	5	7	V
V_{CCQP}	High Driver Supply		9		13	V
V_{IH}	Input Voltage, Logic HIGH		2			V
V_{IL}	Input Voltage, Logic LOW				0.8	V

DC Electrical Characteristics

(V_{CC} = 5V, fosc = 650 KHz, and T_A = +25°C unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Units
V_O	Output Voltage	T_A = 0–70°C	3.45	3.52	3.6	V
I_O	Output Current	See Figure 1 for application		5		A
Vref Acc	Reference Acc			.15	1	%
VTC	Output Voltage TC			-40		ppm
LDR	Load Regulation	0.5 to 7A		0.25		%Vo
LIR	Line Regulation	V_{CC} = ±5%		0.1		%Vo
V_R	Output Voltage Ripple			15		mV
Cum Acc	Cumulative Accuracy[2]	T_A = 0–70°C		1	2.1	%
Eff	Efficiency	Synchronous mode > 2A	85	88		%
Iodr	Output Driver I	Open Loop	0.5	0.7		A
Pd	Power Dissipation			0.1	0.2	W

Notes:

1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.
2. Output Voltage accuracy, Tempco, load regulation, ripple, and transient performance determine the Cumulative Accuracy.

AC Electrical Characteristics[1]

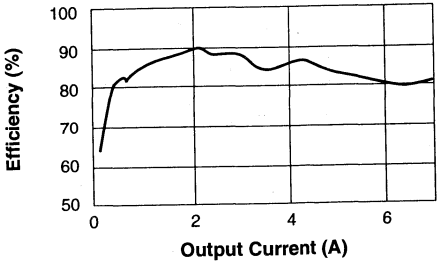
(V_{CC} = 5V, fosc = 650 KHz, and T_A = +25°C unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Units
Tr	Response Time	Il=0.5A to 5.5A		10		µs
Fosc	Oscillator Range		0.2		1.2	MHz
Osc Acc	Fosc Accuracy			10		%
Dtc	Max Duty Cycle	PWM mode	90	95		%
Dtcm	Min Duty Cycle	PFM mode			100	ns
Imax	Imax Threshold			30		mV
Iscp	Short Circuit Prot			80		mV
Ovp	Over Voltage Prot			20		%Vo
Trimax	Response to Imax			15	30	ns
Tssp	Soft start response			10		µs

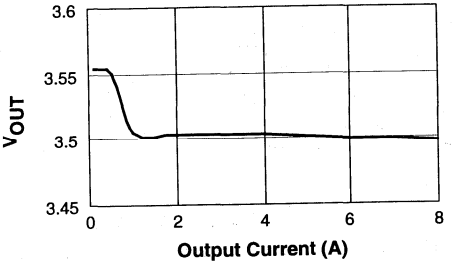
Preliminary Information

Typical Operating Characteristics[1]

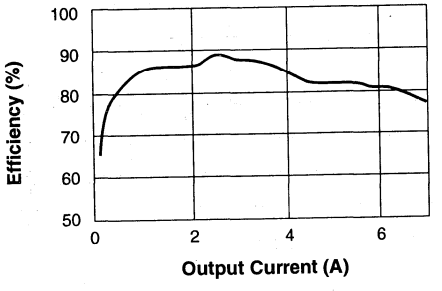
Efficiency vs Output Current (F_{OSC} = 400 KHz)



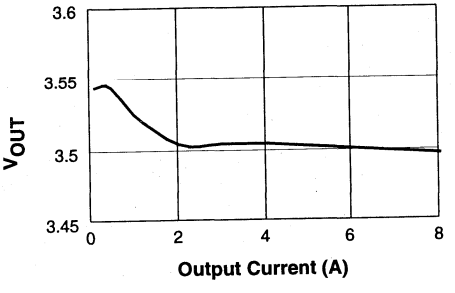
Load Regulation (F_{OSC} = 300 KHz)



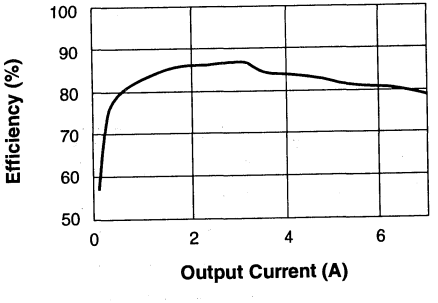
Efficiency vs Output Current (F_{OSC} = 650 KHz)



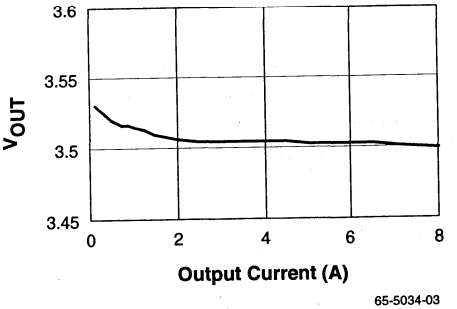
Load Regulation (F_{OSC} = 650 KHz)



Efficiency vs Output Current (F_{OSC} = 1 MHz)



Load Regulation (F_{OSC} = 1 MHz)



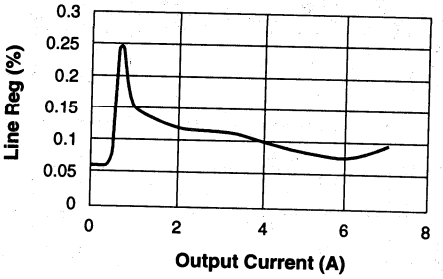
65-5034-03

Note:

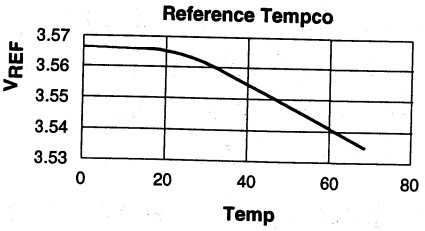
1. Data taken with circuit of Figure 1.

Typical Operating Characteristics (continued)

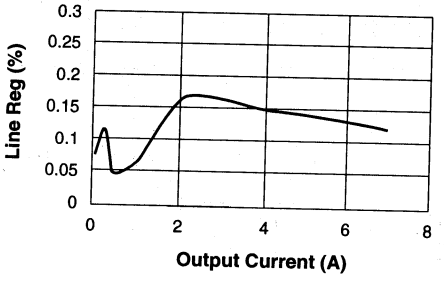
Line Regulation vs. Output Load (F_{OSC} = 400 KHz)



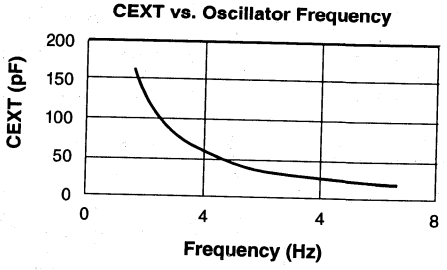
Reference Tempco



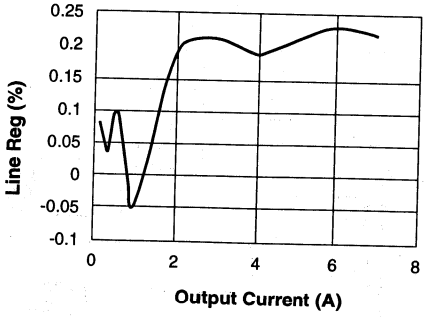
Line Regulation vs. Output Load (F_{OSC} = 650 KHz)



CEXT vs. Oscillator Frequency



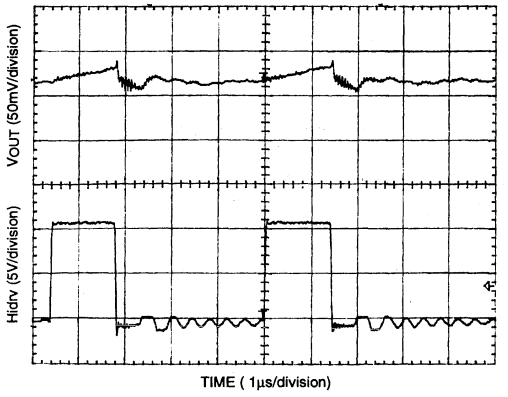
Line Regulation vs. Output Load (F_{OSC} = 1 MHz)



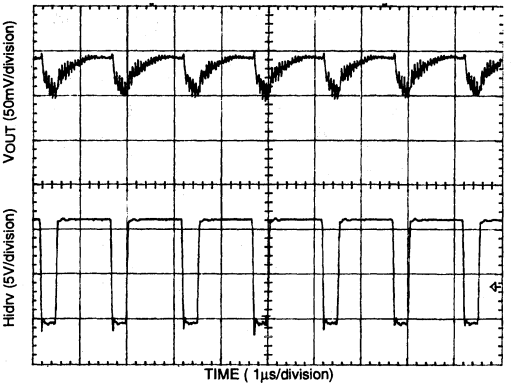
65-5034-04

PERSONAL COMPUTERS

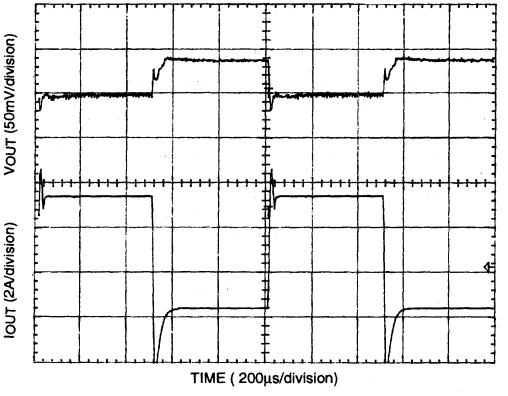
Typical Operating Characteristics (continued)



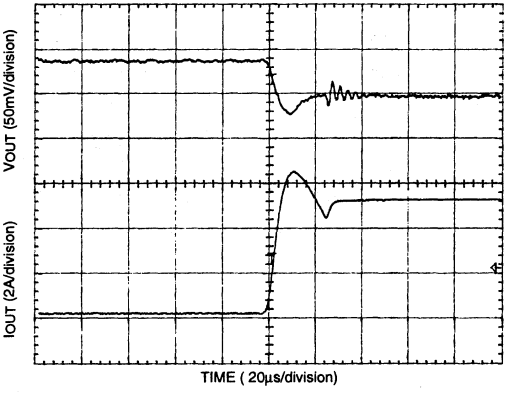
AC Ripple response .2A Load



AC Ripple response 5A Load



Transient Response .2A to 5A Load



Transient Response Magnified

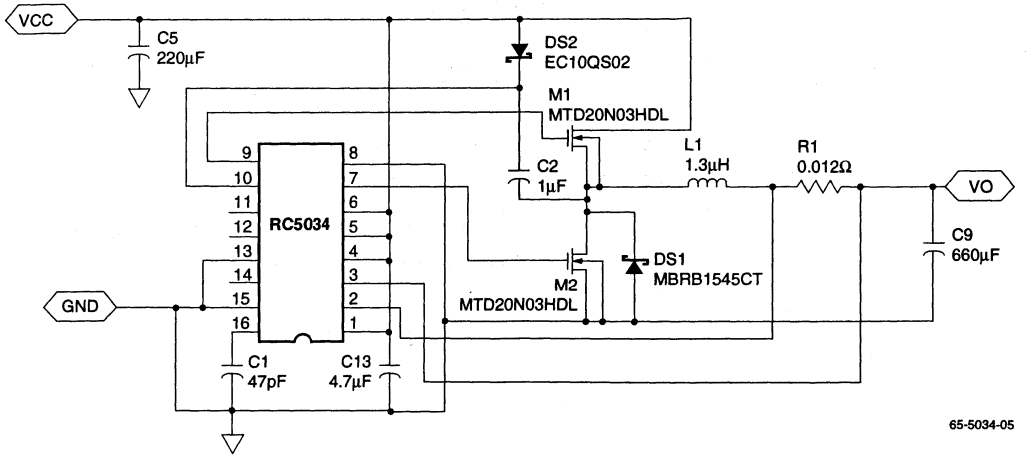


Figure 1. Synchronous 7A Schematic

Preliminary Information

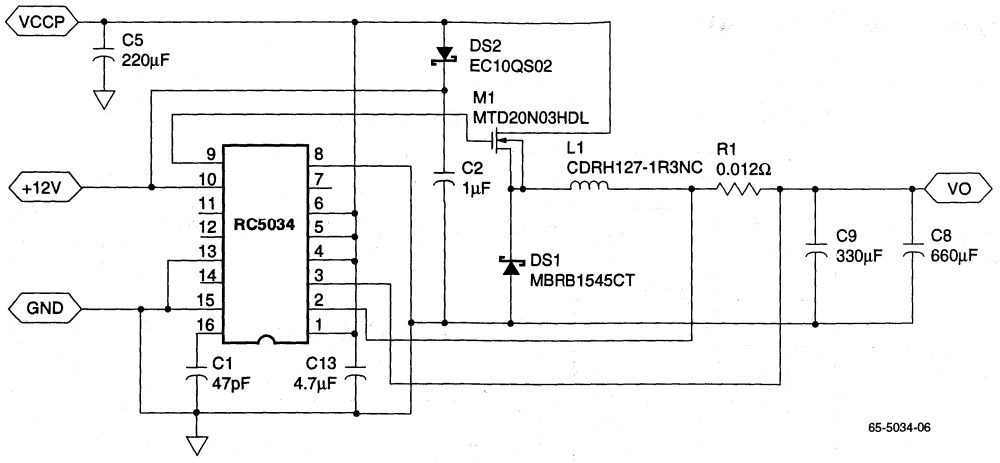


Figure 2. Non-Synchronous 7A Circuit

RC5034 Standard Application Circuit Bill of Materials			
Ref Designator	**Quantity**	**Part No.**	**Manufacturer**
L1	1	1.3 µH CDRH127-1R3NC	Sumida
M1,M2	2	MTD20N03HDL	Motorola
DS1	1	MBRB1545CT	Motorola
DS2	1	EC10QS02L	Nihon
R1	1	.012Ω LRC-2512	IRC
C5	1	220 µF OS-CON 10SA220M	Sanyo
C9	2	330 µF OS-CON 10SA330M	Sanyo
C2	1	1uF	Monolithic ceramic Cap
C1	1	47pF	SMD Cap
C4	2	0.1uF	SMD Cap
C13	1	4.7uF	SMD Cap

Table 1. Components for RC5034

RC5034 Alternate Suppliers of Components			
Ref Designator	Quantity	Alternate Part No.	Alternate Manufacturer
L1	1	1.3 µH PE-53680	Pulse Engineering
M1,M2	2	2SK1388	Fuji
		IRLZ44N	International Rectifier
		Si4410DY	Temic (Siliconix)
DS1	1	C10T02QL	Nihon
		SR1620C	Rectron
DS2	1	MBRS140T3	Motorola
R1	1	.012Ω WSL-2512	DALE

Table 2. Alternate Components Selection

Applications Discussion

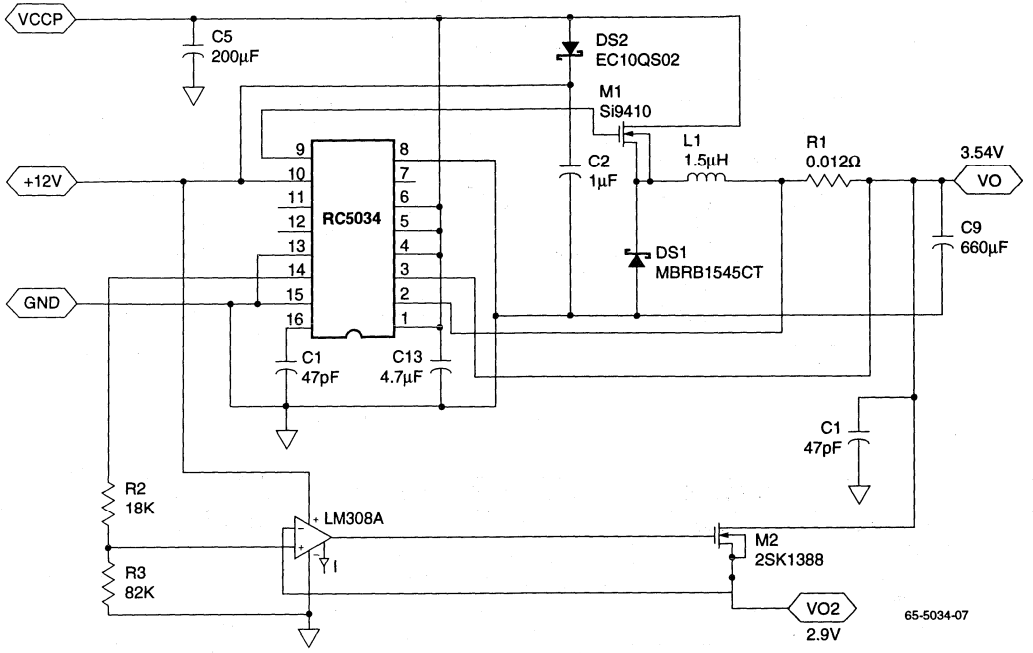


Figure 3. Dual Regulator Applications Circuit

Dual Power Supply Application

In some CPU power applications there may be a need for a split voltage converter. The circuit in Figure 3 addresses this need with only minimal component count. The basic RC5034 non-synchronous DC-DC converter is augmented with an op-amp, a power MOSFET, and some 1% resistors to provide a dual power supply with one voltage set to 3.5V and the other, slaved off of the 3.5V, set to 2.9V. In this configuration, the RC5034 converts the 5V to 3.5V with high efficiency. By using the op-amp, power FET, and the resistors, a low-dropout linear regulator is realized that can be run off of the 3.5V. The 2.9V linear regulator has a relatively high efficiency just due to the fact that the ratio of 2.9V/3.5V is close to 88%. The power FET is a low Rdson n-channel MOSFET, and thus it is reasonably inexpensive. The opamp can be a garden variety, though the input bias current and output slew rate need to be considered to optimize accuracy and transient response. The overall efficiency of this power supply system will very much depend upon the percentage of power used on each power output. Overall, the efficiency of this system will be lower than if both supplies were implemented as switchers; however, the added savings of the part count reduction may more than compensate for the overall lower efficiency.

Standard Application Circuit

The circuit shown in Figure 1 along with its components and values has been designed as representative of the typical application involving the RC5034 for a Pentium™ CPU. Use of the standard application circuit will deliver the performance curves shown under the Typical Operating Characteristics section of the data sheet. Many users will want to develop their own DC-DC converter solution that is uniquely tailored to a specific application requirement. In that case, the users should review the detailed information in the Design Procedure and Applications Information section of the data sheet.

Detailed Description

The RC5034 is a programmable voltage synchronous controller. When designed around the appropriate external components, it can be configured to deliver more than 10A of output current. During heavy loading conditions the RC5034 functions as a current-mode PWM step down regulator. Under light loading conditions, the regulator functions in the PFM or pulse skipping mode, thereby increasing its efficiency under light loads.

Main Control Loop

The main control loop of the regulator (see Block Diagram) contains two main blocks, the analog control block and the digital control block. The analog control block consists of signal conditioning amplifiers that feed into a set of fast comparators which provide the inputs to the digital control block. The signal conditioning block takes inputs from the IFB(current feedback) and VFB(voltage feedback) pins and then sets up two controlling signal paths. The voltage control path gains up the VFB signal and presents that signal to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents that signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator and the output is then presented to a comparator. This comparator provides the main PWM control signal to the digital control block.

There are three other comparators in the analog control block. The first two control the thresholds of where the RC5034 goes into its pulse skipping mode during light loads and the second controls the point at which the max current comparator disables the output drive signal to the upper power MOSFET. The third comparator determines when the synchronous mode bottom side power MOSFET will be enabled and disabled.

The digital controller section is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV and LODRV output pins that will in turn control the external power MOSFETs. This digital section was designed in high speed schottky transistor logic which allows the RC5034 to clock up to speeds greater then 1MHz. This section is responsible for providing the break-before-make timing that ensures that both external FETs will not be on at the same time.

High Current Output Drivers

The RC5034 contains two identical high current output drivers. These drivers contain high speed bipolar transistors configured in a push-pull configuration. Each output driver is capable of pumping out 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for added switching noise immunity. The HIDRV driver has a power supply, VCCQP, which can be either derived from an external voltage source or can be boot-strapped from a flying-capacitor as is shown in Figure 1. In the boot-strapped mode, C2 is alternately charged from VCC via the schottky diode DS2 and then boosted up when M1 is turned on. This provides a VCCQP voltage equal to 2*VCC - Vds(DS2); or about 9.5V with VCC=5V. This voltage is sufficient to provide the 9V gate drive to the external MOSFET that will be needed for achieving a low Rdson. Since the low side synchronous FET is referenced to ground, there is no need to boost the gate drive voltage and its VCCP power pin can just be tied to VCC.

Internal Reference

The reference in the RC5034 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. For a guaranteed stable operation under all loading conditions, a 0.1µF capacitor is recommended on the VREF output pin.

Over -Voltage Protection

The RC5034 provides a constant monitor of the output voltage for over-voltage protection. Should the voltage at the VFB pin exceed 20% of the selected program voltage, then an overvoltage condition will be assumed to exist and the RC5034 will shut down the output drive signals to the power FETs.

Oscillator

The RC5034 oscillator is designed as a fixed current capacitor charging oscillator. An external capacitor allows for maximum flexibility in choosing the associated external components for the RC5034. The oscillator frequency can be set from less than 200KHz to over 1MHz depending on the application requirements.

Design Procedure and Applications Information

Simple Step-Down Converter

Figure 4 shows a step-down DC-to-DC Converter with no feedback controller. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5034 in Figure 1. In Figure 4, the basic operation begins by closing the switch, S1. When S1 is closed the input voltage VB is impressed across the inductor L1. The current flowing in the inductor is given by the following equation: IL=(VB- Vo)Ton/L; where Ton is the time duration for S1 to be closed. When S1 is open, the diode will conduct the inductor current and the output current will be delivered to the load according to the equation: IL=Vo(T – Ton)/L; where T- Ton is the time duration for S1 to be off. By solving these two equations we can arrive at the basic relationship for the output voltage of a step-down converter: Vo=VB(Ton/T).

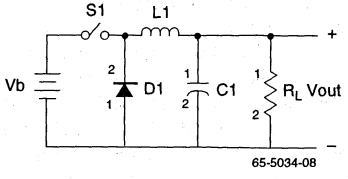


Figure 4. Simple Buck DC-DC Converter

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-to-DC converter application. The critical parameters are inductance (L), max DC current (Imax), and the coil resistance (Rl). The inductor core material is a critical factor in determining the amount of current that the inductor will be able to handle. As with all engineering designs there are trade- offs for various types of inductor core materials. In general, Ferrites are popular because of their low cost, low EMI, and high frequency (>500kHz) characteristics. Molypermalloy powder (MPP) materials have good saturation characteristics and low EMI with low hysteresis losses; however they tend to be expensive and are more efficiently utilized at frequencies below 400kHz. DC winding resistance is another critical parameter. In general, the DC resistance should be kept as low as possible. The power loss in the DC resistance will degrade the efficiency of the converter by the relationship: Power Loss = (Io)2*Rl.

The value of the inductor is a function of the switching frequency (Ton) and the maximum inductor current. The max inductor current can be calculated from the relationship:

$$I_{MAX} = \frac{2I_L}{F_O T_{ON}\left(\frac{V_{IN} - V_{OUT}}{V_{OUT} - V_D}\right) + 1}$$

Where: Fo is the desired clock frequency
Ton is the max on time of the M1 FET
Vd is the forward voltage of the schottky diode D1

Then the inductor value can be calculated with the relationship:

$$L = \frac{V_{IN} - V_{DSON}}{I_{MAX}}(T_{ON})$$

Where: Vdson is the voltage across the drain-source of the M1 FET when switched on.
(this can be calculated by RDSon * Imax)

Current-Sense Resistor

The current sense resistor will carry all of the peak current of the inductor. This current will be more than the designed for load current. The RC5034 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds 100mV. When this happens the output voltage will temporarily go out of regulation. As the voltage across the resistor becomes larger, the top-side FET will turn off more and more until the current limit value is reached and then the RC5034 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is advisable. Thus the resistor should be set by the relationship:

R = 100 mV/ Ipeak

Where: Ipeak = Imax * 1.33

Since the value of the sense resistor is generally in the miliohm region, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFB and VFB pins of the RC5034 should be Kelvin connected to the pads of the current-sense resistor as shown in the sample layout Figure 5. To minimize the influence of noise the two traces should be run next to each other and the pins should be bypassed with a .1uF to GND as close to the device pins as possible.

Filter Capacitors

Good ripple performance and transient response are functions of the filter capacitors. Since the 5V input for a PC motherboard can be located several inches away from the DC-to-DC converter, input capacitance can play an important role in the load transient response of the RC5034. In general, the higher the input capacitance, the more charge storage is available for improving the current transfer through the top-side FET. A good rule of thumb is that for each watt of output power that you wish to deliver, there should be around 10uF of input capacitance. Low "ESR" capacitors are best suited for this application and can have an influence on the converter's efficiency. The input capacitor should be placed as close to the drain of the top-side FET as possible to reduce the effect of ringing that can be caused by large trace lengths.

The ESR rating of a capacitor is a difficult number to pin down. ESR or Equivalent Series Resistance, is defined at the resonant impedance of that capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for it to have an associated resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained with the following equation: ESR = Pd/2pfC. Where Pd is the capacitor's dissipation factor and f is the frequency of measure and C is the capacitance in farads.

With this in mind, calculating the output capacitance correctly is crucial to the performance of the DC-to-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and the transient load response. The calculation uses the following equation:

$$C(\mu F) = \frac{T_{ON}\left(\frac{(V_{IN} - V_{OUT})I_{MAX}}{V_{OUT}} + I_L\right)}{V_r}$$

Where: Vr is the desired output ripple voltage

Schottky Diode Selection

The application circuit diagram shows two schottky diodes, DS1 and DS2. DS1 is used in parallel of M2 in order to prevent the lossy body diode in the FET from turning on. DS2 serves a dual purpose. As it is configured, it allows the VCCQP supply pin of the RC5034 to be bootstrapped up to 9V by using the bootstrap capacitor C2. When the lower FET

M2 is turned on, one side of the capacitor C2 is connected to GND while the other side of the cap is being charged up through D2 to a voltage that is Vin - Vd. When the lower FET turns off and the upper one turns on, the voltage that is supplied to the VCCQP pin is 2Vin - Vd. The voltage then that is applied to the gate of the FET is VCCQP - Vsat, typically around 9V. It is important in the selection of DS1 and DS2 that they have a low forward voltage drop as this directly affects the regulator efficiency. The other job that DS2 performs is that of bootstrapping VCCQP during startup. It is possible to cause the output stage to latchup if the VCCQP supply is brought up before the other VCC supplies of the RC5034. It is therefore advisable that DS2 be connected even in applications that do not utilize the bootstrapping technique for VCCQP. An alternate application could tie the VCCQP supply pin to the +12V power supply in the PC, thus eliminating the need for C2 and forcing the Rdson of M1 even lower by increasing its Vgs.

MOSFET Switches

The MOSFET switches in the RC5034 applications circuit are N-channel "logic-level" FETs. This means that they will be fully on with a Vgs of 4V. Many manufacturers make logic-level FETs and the trick is to choose the one with the lowest RDSon at the given Imax current level. The value of RDSon directly enters into the efficiency equation as a power loss. Also influencing the efficiency is the gate charge of the FET and the clock frequency of the RC5034. At higher clocking rates the amount of charge needed to be delivered to the FET is going to lower the overall efficiency. In higher current applications, the upper FET can be paralleled to provide greater current capability; however, the lower FET doesn't necessarily have to be doubled since it is on only a fraction of the time that the upper FET is on.

PCB Layout and Grounding

As is the case with most analog circuitry, good layout practices are necessary to achieve the optimum in the overall performance of the DC-to-DC converter. In general, it is always a good practice to have a tight layout that attempts to minimize short low inductance wiring to the RC5034.

The use of multilayer PCB is recommended. In particular, it is recommended to have a continuos ground plane beneath the circuit, 2oz copper would be preferred in high current applications. As was stated previously, the current-sense resistor, R1, should be located as close to the RC5034 as possible and the IFB and VFB traces should be Kelvin connected to the pads of R1. To minimize switching losses and noise, place M1, M2, L and DS2 as close together as possible. Also try to keep the HIDRV and LODRV gate drive signal traces as short as possible. It is recommended that the noisy switching part of the circuit be kept away from the low current pins on the chip such as IFB, VFB, ADJ3, ADJ1, and CEXT. Keep the 0.1uF bypass capacitors as close to the chip pins as possible. All of the ground pins should be connected to the ground plane directly under the chip. A sample layout is provided in Figure 5.

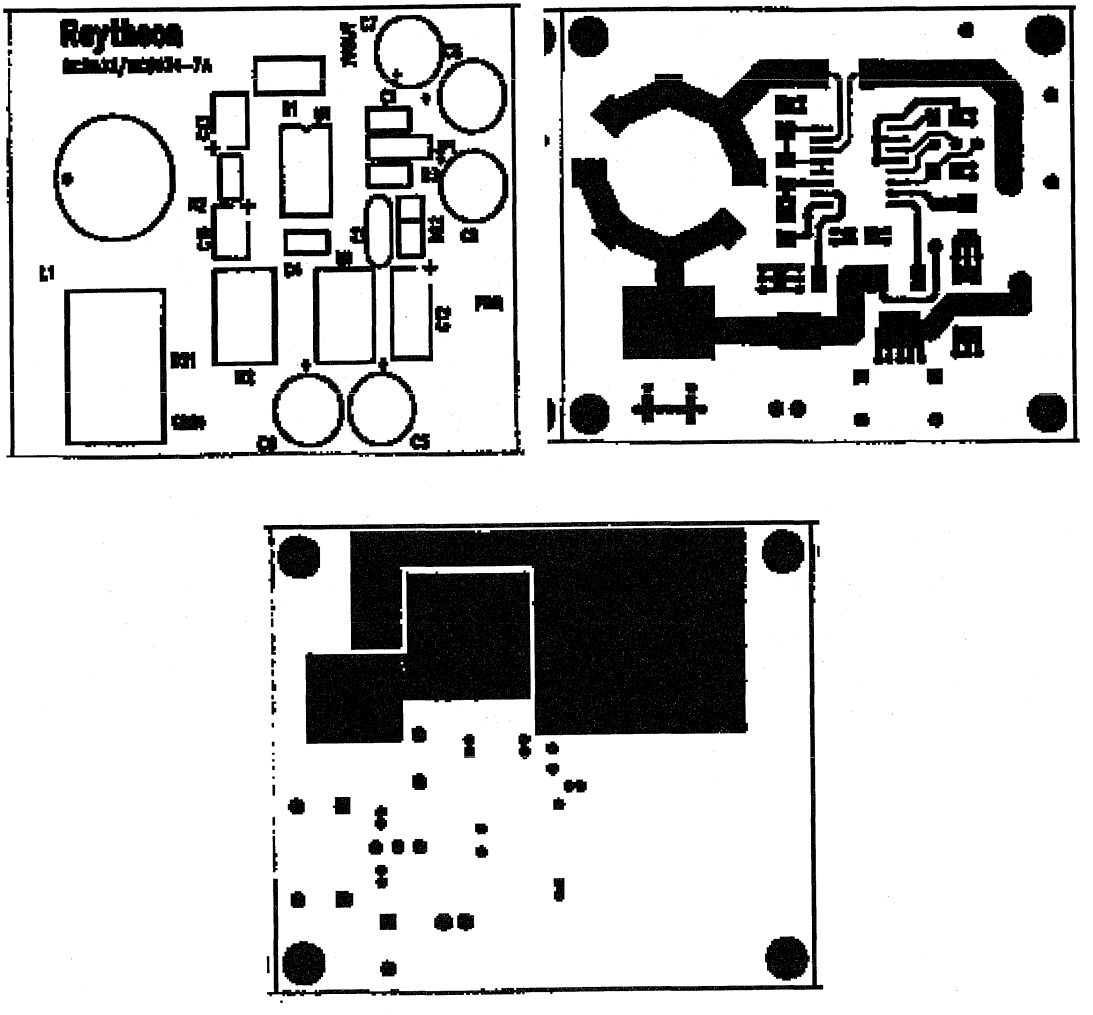


Figure 5. Sample PCB Layout

Ordering Information

Product Number	Package	θJA
RC5034M	16 SOIC	85°C/W

RC5040

Programmable Synchronous DC-DC Converter

Features

- 85% efficiency
- 350uA quiescent current in shutdown
- 4 Bit DAC for voltage selection
- On-board Power Good function
- Over-Voltage Protection
- Output voltage range from 2V to 3.5V
- Factory trimmed zero TC reference voltage
- Adjustable oscillator frequency to 1MHz
- Drives N-Channel MOSFETs
- 20 pin SOIC package
- Meets Intel VRM specification

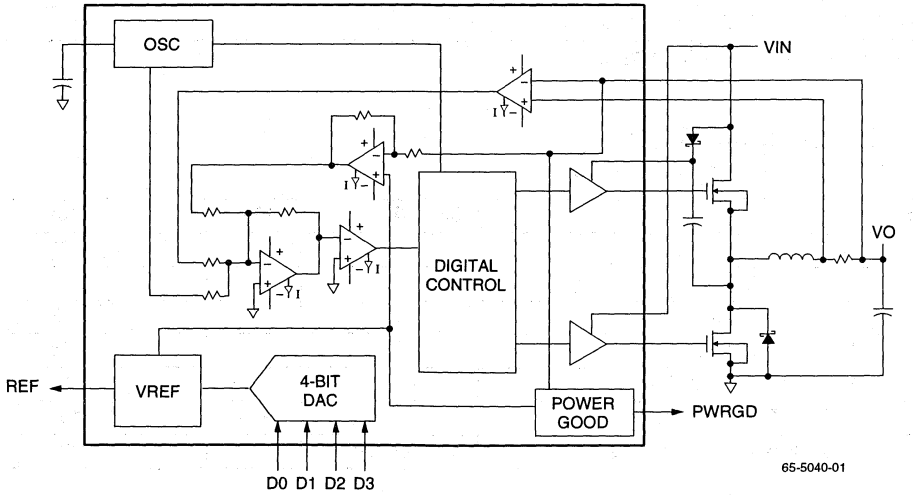
Applications

- Programmable power supply for Pentium Pro™ based CPU motherboards
- VRM module for Pentium Pro™ CPU
- Programmable power supply

Description

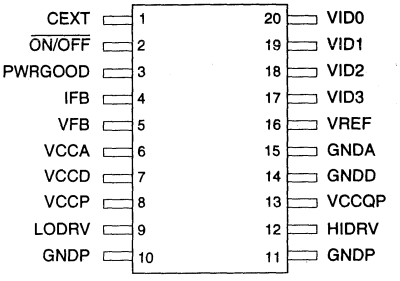
The RC5040 is a synchronous mode DC-DC controller IC dedicated to providing a 5V programmable conversion (2.1V to 3.5V) for Pentium Pro™ CPU power. It can be configured in both the synchronous and non-synchronous modes and with the proper applications circuitry can be used to deliver load current greater than 12 Amps. The RC5040 is designed to operate in a standard PWM control mode under heavy load conditions and as a PFM controller in light load conditions. Its highly accurate zero TC reference eliminates the need for precision external components in order to achieve tight tolerance voltage regulation. Through the use of the on-board DAC, the RC5040 can generate accurate output voltages from 2.1V up to 3.5V in 0.1V increments. An integrated Power Good function constantly monitors the output voltage and produces a low-going interrupt signal to the Pentium Pro CPU in the event of a out-of-tolerance voltage situation, thereby protecting the CPU. The programmable oscillator can operate from 200KHz to greater than 1MHz to provide for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs.

Block Diagram



Rev. 0.9.8

Pin Assignments



Preliminary Information

Pin Definitions

Pin Name	Pin Number	Pin Function Description
CEXT	1	External Capacitor for setting oscillator frequency
On/Off	2	A low level on this pin will power down; tie to VCCD if not used
Pwrgood	3	A 3.0V logic level indicated power is within limits
IFB	4	Current Feedback Input
VFB	5	Voltage Feedback Input
VCCA	6	Analog VCC
VCCD	7	Digital VCC
VCCP	8	VCC for synchronous FET output driver
LODRV	9	Synchronous FET driver output
GNDP	10, 11	Power ground for high current drivers
HIDRV	12	High side FET driver output
VCCQP	13	VCC for High side FET output driver
GNDD	14	Digital ground
GNDA	15	Analog ground
VREF	16	Reference voltage output
VID3-VID0	17-20	Voltage identification code input

Note: 0 = Processor pin connected to VSS. 1 = Open.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage				13	V
V_{CCP}	Driver Voltage				13	V
V_{CCQP}	High FET Driver Supply				13	V
T_J	Junction Temperature				175	°C
T_A	Ambient Operating Temperature		0		70	°C
T_S	Storage Temperature		-65		150	°C
T_L	Lead Soldering Temperature	10 seconds			300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5	7	V
V_{CCP}	Drivers Supply Voltage		4.5	5	12	V
V_{IH}	Input Voltage, Logic HIGH		2			V
V_{IL}	Input Voltage, Logic LOW				0.8	V

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	See Voltage Identification Code Table, T_A = 0–70°C	2.1		3.5	V
Output Current			10		A
Set Point Accuracy	I_{LOAD} = 1A includes ripple		0.25	1.5	%
Output Voltage Tempco			40		ppm/°C
Load Regulation	I_{load} = 0.5 to 10A		1		%Vo
Line Regulation	Input Voltage = 4.75 to 5.25V, I_{load} = 10A (See Figure 1)		0.14		%Vo
Output Voltage Ripple			30		mV
Cumulative Accuracy[1]	T_A = 0–70°C		2	5	%
Efficiency	I_{load} = 10A	80	85		%
Power Dissipation			0.1	0.2	W
Output Current Driver		0.5	0.7		A

Notes:

1. Output Voltage Accuracy, Tempco, Load Regulation, Line Regulation, Ripple, &Transient Performance determine the Cumulative Accuracy.

P6 Pins							
VID3	VID2	VID1	VID0	VDC	Set Point +Ripple[1] (±mV)	Total Room Temperature Accuracy[2] (±mV)	Total System Accuracy[3] (±mV)
1	1	1	1	No CPU	-	-	-
1	1	1	0	2.1	32	74	105
1	1	0	1	2.2	33	77	110
1	1	0	0	2.3	35	81	115
1	0	1	1	2.4	36	84	120
1	0	1	0	2.5	37	88	125
1	0	0	1	2.6	39	91	130
1	0	0	0	2.7	41	95	135
0	1	1	1	2.8	42	98	140
0	1	1	0	2.9	44	102	145
0	1	0	1	3.0	45	105	150
0	1	0	0	3.1	47	109	155
0	0	1	1	3.2	48	112	160

P6 Pins				VDC	Set Point +Ripple[1] (±mV)	Total Room Temperature Accuracy[2] (±mV)	Total System Accuracy[3] (±mV)
VID3	VID2	VID1	VID0				
0	0	1	0	3.3	50	116	165
0	0	0	1	3.4	51	119	170
0	0	0	0	3.5	53	123	175

Notes:
1. Includes initial accuracy plus ripple. (±mV).
2. Includes set point accuracy + line reg + load reg + transient (±mV).
3. Includes temperature effects to total accuracy (±mV).

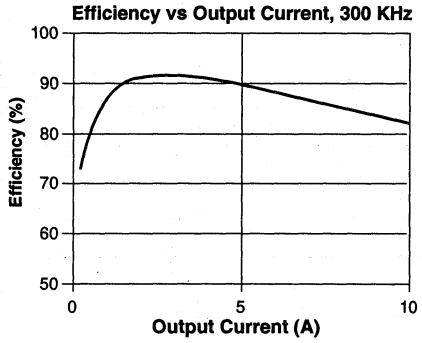
AC Electrical Characteristics[1]

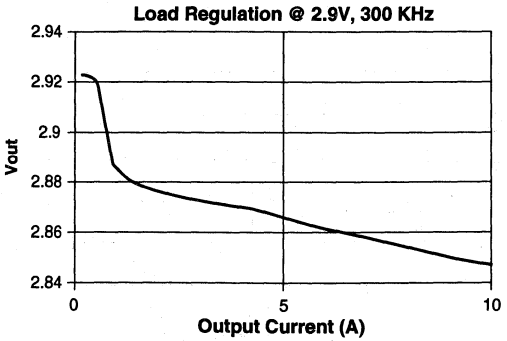
T_A = +25°C unless otherwise noted). Refer to Figure 1.

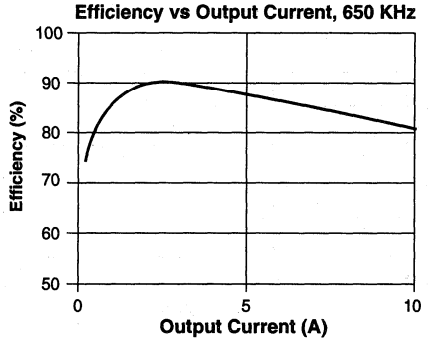
Parameter	Min	Typ	Max	Units
Response Time Sleep-to-Full Load		10		µs
Oscillator Frequency Range	.2		1.2	MHz
Oscillator Frequency Precision		10		%
Maximum Duty Cycle in PWM Mode	90	95		%
Minimum Duty Cycle in PFM Mode			100	ns
IMAX Circuit Detection (Comparator Threshold)		30		mV
Short Circuit Protection/Coil Saturation Detection		80		mV
Response Time to IMAX and Short Circuit Protection		15	30	ns
Soft Start during Power-Up and Power-Down		10		µs

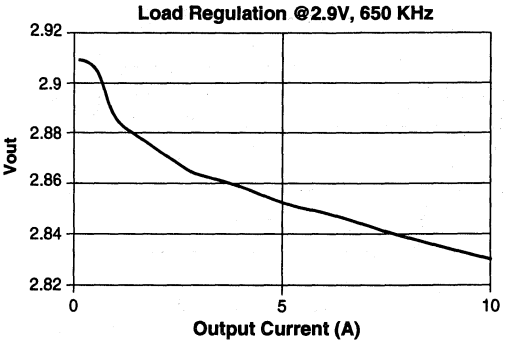
Notes:
1. Guaranteed by design, not tested 100%.

Typical Operating Characteristics





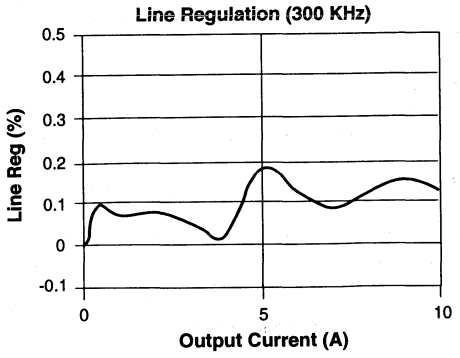


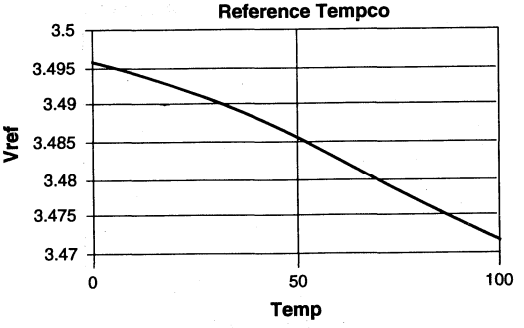


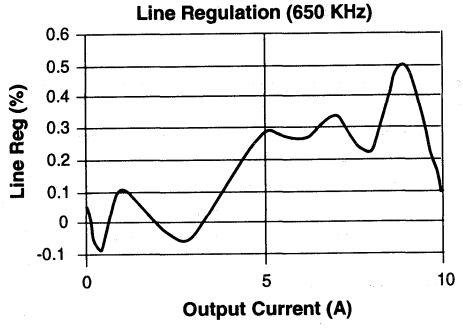
65-5040-02

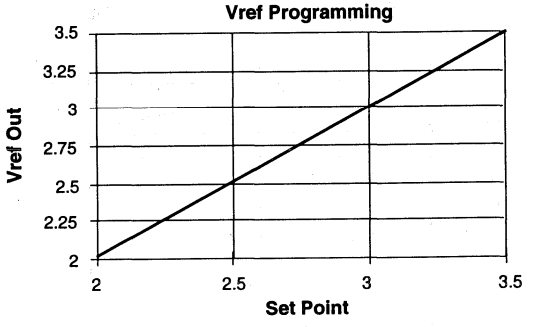
PERSONAL COMPUTERS

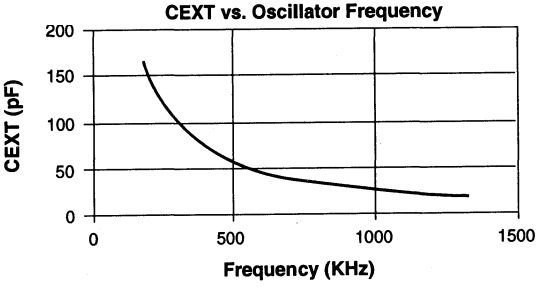
Typical Operating Characteristics (continued)







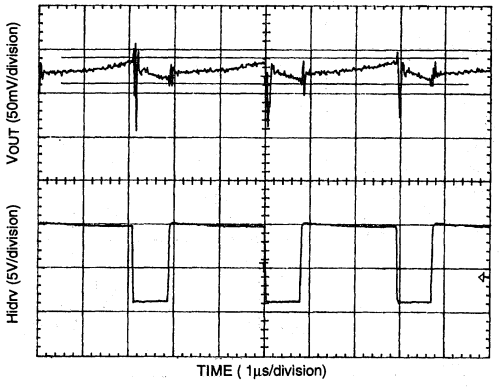




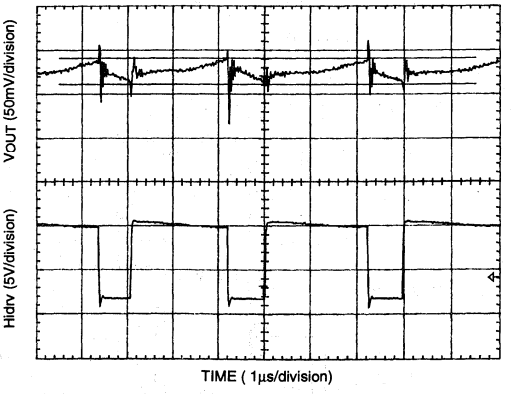
65-5040-03

Preliminary Information

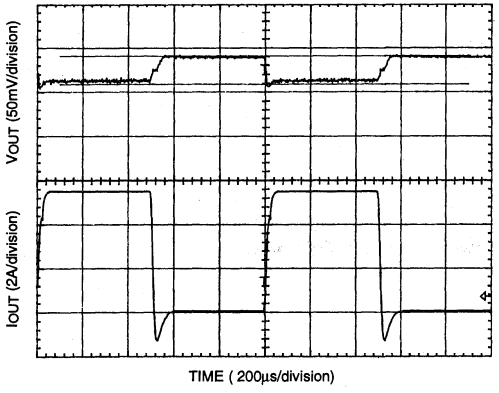
Typical Operating Characteristics (continued)



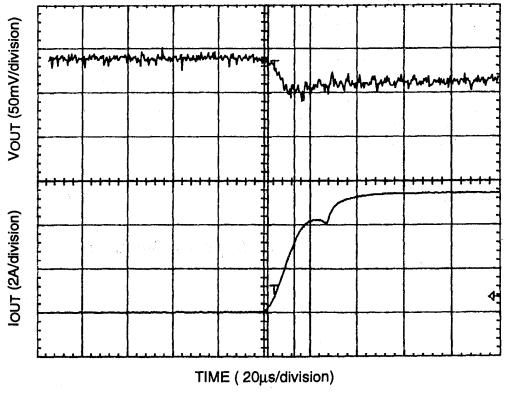
AC Ripple response 2A Load



AC Ripple response 10A Load



Transient Response .2A to 6A Load



Transient Response Magnified

PERSONAL COMPUTERS

Test Circuits

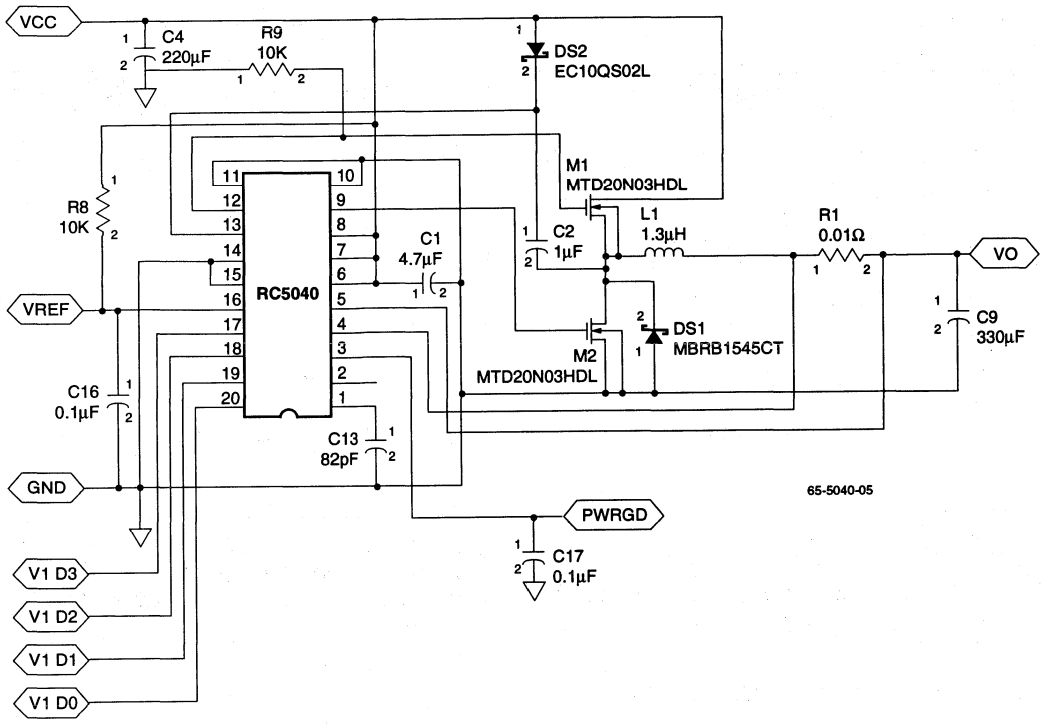


Figure 1. Synchronous DC-DC Conversion Test Configuration

Preliminary Information

Test Circuits (continued)

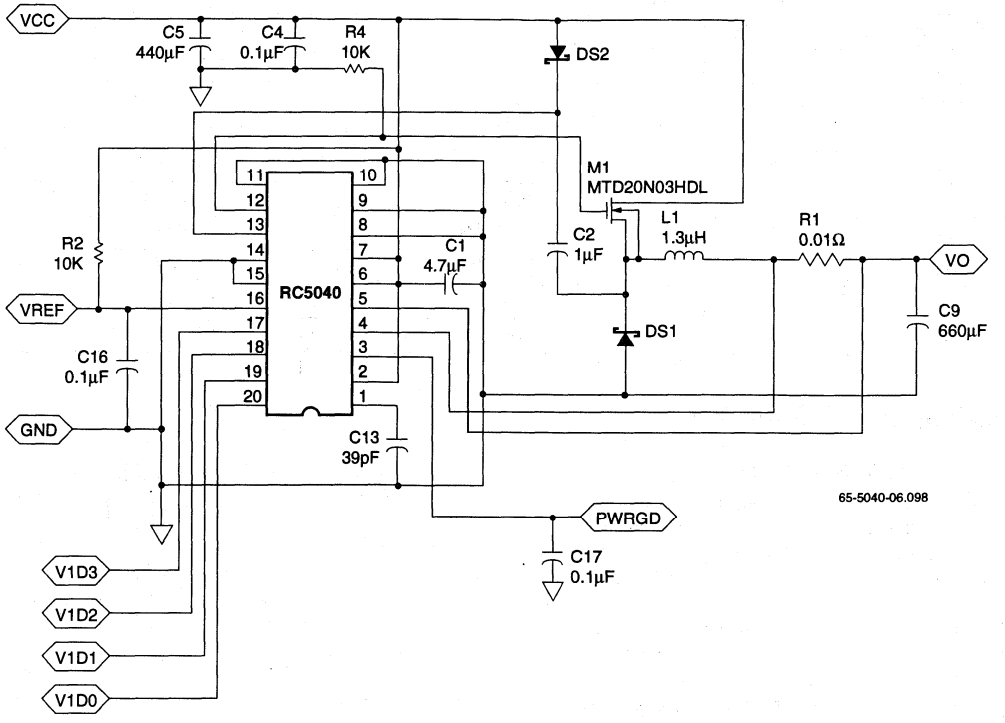


Figure 2. Non-Synchronous DC-DC Conversion Test Configuration

Table 1. Components for RC5040

RC5040 Standard ApplicationCircuit Bill of Materials			
Ref Designator	**Quantity**	**Part No.**	**Manufacturer**
L1	1	1.3µH CDRH127-1R3NC	Sumida
M1,M2	2	MTD20N03HDL	Motorola
DS1	1	MBRB1545CT	Motorola
DS2	1	EC10QS02L	Nihon
R1	1	.01n LRC-2512	IRC
C4	1	220µF OS-CON 10SA220M	Sanyo
C9	1	330µF OS-CON 10SA330M	Sanyo
C2	1	1uF	Monolithic ceramic Cap
C13	1	82pF	SMD Cap
C16,C17	2	0.1uF	SMD Cap
R8,R9	2	10K	SMD Resistor
C1	1	4.7µF	SMD Cap

Table 2. Alternate Component Selection

RC5040 Alternate Suppliers of Components			
Ref Designator	**Quantity**	**Alternate Part No.**	**Alternate Manufacturer**
L1	1	PE-53680	Pulse Engineering
M1,M2	2	2SK1388	Fuji
		IRLZ44N	International Rectifier
DS1	1	C10T02QL	Nihon
		SR1620C	Rectron
DS2	1	MBRS140T3	Motorola
R1	1	WSL-2512	DALE
D1	1	6.2V Zener	Motorola
R3	1	100Ω	SMD Resistor

Applications Discussion

Standard Application Circuit

The circuit shown in Figure 1 along with its components and values has been designed as representative of the typical application involving the RC5040 for a Pentium Pro™ CPU. Use of the circuit in Figure 1 will deliver the performance curves shown under the Typical Operating Characteristics section of the data sheet. Many users will want to develop their own DC-DC converter solution that is uniquely taylored to a specific application requirement. In that case, the users should review the detailed information in the Design Procedure and Applications Information section of the data sheet.

Detailed Description

The RC5040 is a programmable voltage synchronous controller. When designed around the appropriate external components, it can be configured to deliver more than 12A of output current. During heavy loading conditions the RC5040 functions as a current-mode PWM step down regulator. Under light loading conditions, the regulator functions in the PFM or pulse skipping mode, thereby increasing its effi-cency unde light loads.

Main Control Loop

The main control loop of the regulator (see Block Diagram) contains two main blocks, the analog control block and the digital control block. The analog control block consists of signal conditioning amplifiers that feed into a set of fast comparators which provide the inputs to the digital control block. The signal conditioning block takes inputs from the IFB(current feedback) and VFB(voltage feedback) pins and then sets up two controlling signal paths. The voltage control path gains up the VFB signal and presents that signal to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents that signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator and the output is then presented to a comparator. This comparator provides the main PWM control signal to the digital control block.

There are three other comparators in the analog control block. The first two control the thresholds of where the RC5040 goes into its pulse skipping mode during light loads and the second controls the point at which the max current comparator disables the output drive signal to the upper power MOSFET. The third comparator determines when the synchronous mode bottom side power MOSFET will be enabled and disabled.

The digital controller section is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV and LODRV output pins that will in turn control the external power MOSFETs. This digital section was designed in high speed schottky transistor logic which allows the RC5040 to clock up to speeds greater then 1MHz. This section is responsible for providing the break-before-make timing that ensures that both external FETs will not be on at the same time.

High Current Output Drivers

The RC5040 contains two identical high current output drivers. These drivers contain high speed bipolar transistors configured in a push-pull configuration. Each output driver is capable of pumping out 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for added switching noise immunity. The HIDRV driver has a power supply, VCCQP, which can be either derived from an external voltage source or can be boot-strapped from a flying-capacitor as is shown in Figure 1. In the boot-strapped mode, C2 is alternately charged from VCC via the schottky diode DS2 and then boosted up when M1 is turned on. This provides a VCCQP voltage equal to 2*VCC - Vds(DS2); or about 9.5V with VCC=5V. This voltage is sufficient to provide the 9V gate drive to the

external MOSFET that will be needed for achieving a low Rdson. Since the low side synchronous FET is referenced to ground, there is no need to boost the gate drive voltage and its VCCP power pin can just be tied to VCC.

Internal Reference

The reference in the RC5040 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. Added into the reference is the output from a 4-bit DAC. The DAC is provided in accordance with the Pentium Pro ™ specification that requires the DC-DC converter to be able to respond to a VID programming code. This code will change the reference voltage from 2.0V up to 3.5V in 100mV increments. For a guarenteed stable operation under all loading conditions, a 10K pull-up resistor is recommended along with a 0.1µF capacitor on the VREF output pin.

Power Good

The RC5040 Power Good function is designed in accordance with the Pentium Pro ™ DC-DC converter specification and provides a constant voltage monitor on the VFB pin. The circuit takes the VFB signal and compares it to the VREF voltage and then will provide a low going interrupt signal to the CPU should the power supply voltage exceed ±7% of its nominal set value. The Power Good flag provides no other control function to the RC5040.

Over-Voltage Protection

The RC5040 provides a constant monitor of the output voltage for over-voltage protection. Should the voltage at the VFB pin exceed 20% of the selected program voltage, then an overvoltage condition will be assumed to exist and the RC5040 will shut down the output drive signals to the power FETs.

Oscillator

The RC5040 oscillator is designed as a fixed current capacitor charging oscillator. An external capacitor allows for maximum flexibility in choosing the associated external components for the RC5040. The oscillator frequency con be set from less than 200KHz to over 1MHz depending on the application requirements.

Design Procedure and Applications Information

Simple Step-Down Converter

Figure 3 shows a step-down DC-to-DC Converter with no feedback controller. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5040 in Figure 1. In Figure 3, the basic operation begins by closing the switch, S1. When S1 is closed the input voltage VB is impressed across the inductor L1.
The current flowing in the inductor is given by the following equation: IL=(VB- Vo)Ton/L; where Ton is the time duration for S1 to be closed. When S1 is open, the diode will conduct the inductor current and the output current will be delivered to the load according to the equation: IL=Vo(T – Ton)/L; where T- Ton is the time duration for S1 to be off. By solving these two equations we can arrive at the basic relationship for the output voltage of a step-down converter: Vo= VB(Ton/T).

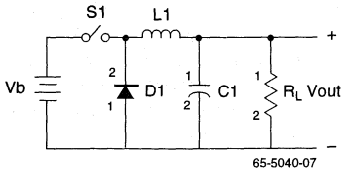


Figure 3. Simple Buck DC-DC Converter

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-to-DC converter application. The critical parameters are inductance (L), max DC current (Imax), and the coil resistance (Rl). The inductor core material is a critical factor in determining the amount of current that the inductor will be able to handle. As with all engineering designs there are trade- offs for various types of inductor core materials. In general, Ferrites are popular because of their low cost, low EMI, and high frequency (>500kHz) characteristics. Molypermalloy powder (MPP) materials have good saturation characteristics and low EMI with low hysteresis losses; however they tend to be expensive and are more efficiently utilized at frequencies below 400kHz. DC winding resistance is another critical parameter. In general, the DC resistance should be kept as low as possible. The power loss in the DC resistance will degrade the efficiency of the converter by the relationship: Power Loss = (Io)2*Rl.

The value of the inductor is a function of the switching frequency (Ton) and the maximum inductor current. The max inductor current can be calculated from the relationship:

$$I_{MAX} = \frac{2I_L}{F_O T_{ON}\left(\frac{V_{IN} - V_{OUT}}{V_{OUT} - V_D}\right) + 1}$$

Where : Fo is the desired clock frequency
Ton is the max on time of the M1 FET
Vd is the forward voltage of the schottky diode D1

Then the inductor value can be calculated with the relationship:

$$L = \frac{V_{IN} - V_{DSON}}{I_{MAX}}(T_{ON})$$

Where : Vdson is the voltage across the drain-source of the M1 FET when switched on.
(this can be calculated by RDSon * Imax)

Current-Sense Resistor

The current sense resistor will carry all of the peak current of the inductor. This current will be more than the designed for

PERSONAL COMPUTERS

load current. The RC5040 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds 100mV. When this happens the output voltage will temporarily go out of regulation. As the voltage across the resistor becomes larger, the top-side FET will turn off more and more until the current limit value is reached and then the RC5040 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is advisable. Thus the resistor should be set by the relationship:

R = 100 mV/Ipeak

Where : Ipeak = Imax * 1.33

Since the value of the sense resistor is generally in the milliohm region, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFB and VFB pins of the RC5040 should be Kelvin connected to the pads of the current-sense resistor as shown in the sample layout Figure 4. To minimize the influence of noise the two traces should be run next to each other and the pins should be bypassed with a .1uF to GND as close to the device pins as possible.

Filter Capacitors

Good ripple performance and transient response are functions of the filter capacitors. Since the 5V input for a PC motherboard can be located several inches away from the DC-to-DC converter, input capacitance can play an important role in the load transient response of the RC5040. In general, the higher the input capacitance, the more charge storage is available for improving the current transfer through the top-side FET. A good rule of thumb is that for each watt of output power that you wish to deliver, there should be around 10uF of input capacitance. Low "ESR" capacitors are best suited for this application and can have an influence on the converter's efficiency. The input capacitor should be placed as close to the drain of the top-side FET as possible to reduce the effect of ringing that can be caused by large trace lengths.

The ESR rating of a capacitor is a difficult number to pin down. ESR or Equivalent Series Resistance, is defined at the resonant impedance of that capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for it to have an associated resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained with the following equation: ESR = Pd/2pfC. Where Pd is the capacitor's dissipation factor and f is the frequency of measure and C is the capacitance in farads.

With this in mind, calculating the output capacitance correctly is crucial to the performance of the DC-to-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and the transient load response. The calculation uses the following equation:

$$C(\mu F) = \frac{T_{ON}\left(\frac{(V_{IN} - V_{OUT})\, I_{MAX}}{V_{OUT}} + I_L\right)}{V_r}$$

Where: Vr is the desired output ripple voltage

Schottky Diode Selection

The application circuit diagram shows two schottky diodes, DS1 and DS2. DS1 is used in parallel of M2 in order to prevent the lossy body diode in the FET from turning on. DS2 serves a dual purpose. As it is configured, it allows the VCCQP supply pin of the RC5040 to be bootstrapped up to 9V by using the bootstrap capacitor C2. When the lower FET M2 is turned on, one side of the capacitor C2 is connected to GND while the other side of the cap is being charged up through D2 to a voltage that is Vin - Vd. When the lower FET turns off and the upper one turns on, the voltage that is supplied to the VCCQP pin is 2Vin - Vd. The voltage then that is applied to the gate of the FET is VCCQP - Vsat, typically around 9V. It is important in the selection of DS1 and DS2 that they have a low forward voltage drop as this directly affects the regulator efficiency. The other job that DS2 performs is that of bootstrapping VCCQP during startup. It is possible to cause the output stage to latchup if the VCCQP supply is brought up before the other VCC supplies of the RC5040. It is therefore advisable that DS2 be connected even in applications that do not utilize the bootstrapping technique for VCCQP. An alternate application could tie the VCCQP supply pin to the +12V power supply in the PC, thus eliminating the need for C2 and forcing the Rdson of M1 even lower by increasing its Vgs.

MOSFET Switches

The MOSFET switches in the RC5040 applications circuit are N-channel "logic-level" FETs. This means that they will be fully on with a Vgs of 4V. Many manufacturers make logic-level FETs and the trick is to choose the one with the lowest RDSon at the given Imax current level. The value of RDSon directly enters into the efficiency equation as a power loss. Also influencing the efficiency is the gate charge of the FET and the clock frequency of the RC5040. At higher clocking rates the amount of charge needed to be delivered to the FET is going to lower the overall efficiency. In higher current applications, the upper FET can be paralleled to provide greater current capability; however, the lower FET doesn't necessarily have to be doubled since it is on only a fraction of the time that the upper FET is on.

PCB Layout and Grounding

As is the case with most analog circuitry, good layout practices are necessary to achieve the optimum in the overall performance of the DC-to-DC converter. In general, it is always a good practice to have a tight layout that attempts to minimize short low inductance wiring to the RC5040.

The use of multilayer PCB is recommended. In particular, it is recommended to have a continuos ground plane beneath the circuit, 2oz copper would be preferred in high current applications. As was stated previously, the current-sense resistor, R1, should be located as close to the RC5040 as possible and the IFB and VFB traces should be Kelvin connected to the pads of R1. To minimize switching losses and noise, place M1, M2, L and DS2 as close together as possible. Also try to keep the HIDRV and LODRV gate drive signal traces as short as possible. It is recommended that the noisy switching part of the circuit be kept away from the low current pins on the chip such as IFB, VFB, VREF, and CEXT. Keep the 0.1uF bypass capacitors as close to the chip pins as possible. All of the ground pins should be connected to the ground plane directly under the chip. A sample layout is provided in Figure 4.

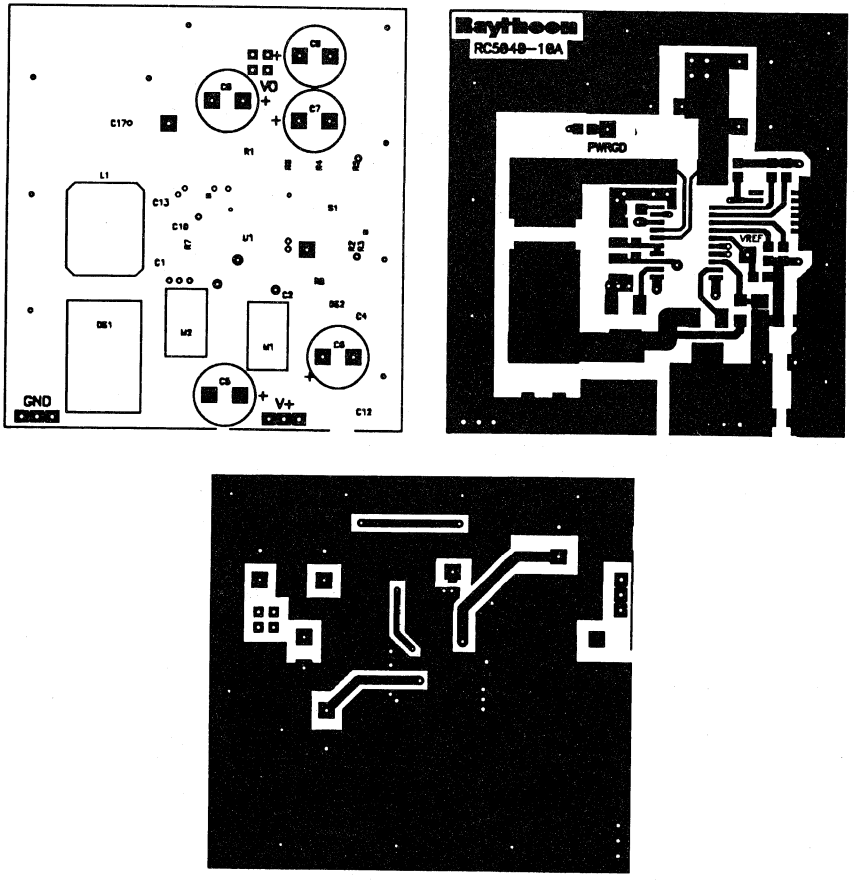


Figure 4. Sample PCB Layout

Ordering Information

Product Number	Package	θJA
RC5040M	20 pin SOIC	80°C/W

RC5042

Programmable DC-DC Converter

Features

- 85% efficiency
- 350µA quiescent current in shutdown
- 4 Bit DAC for voltage selection
- On-board Power Good function
- Over-Voltage Protection
- Output voltage range from 2.1V to 3.5V
- Factory trimmed zero TC reference voltage
- Adjustable oscillator frequency to 1MHz
- Drives N-Channel MOSFETs
- 16 pin SOIC package
- Meets Intel VRM specification

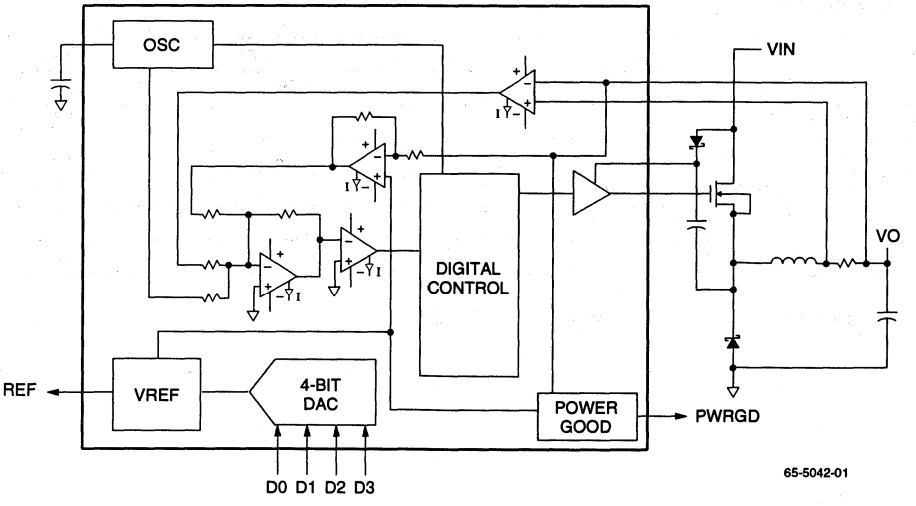
Applications

- Programmable power supply for Pentium Pro™ based CPU motherboards
- VRM module for Pentium Pro™ CPU
- Programmable power supply

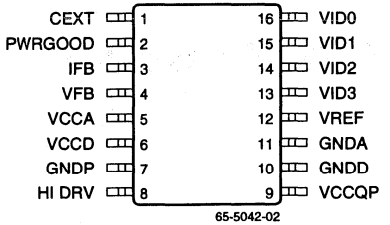
Description

The RC5042 is a non-synchronous DC-DC controller IC dedicated to providing a 5V programmable conversion (2.1V to 3.5V) for Pentium Pro™ CPU power. The RC5042 with the proper applications circuitry can be used to deliver load current greater than 12 Amps. The RC5042 is designed to operate in a standard PWM control mode under heavy load conditions and as a PFM controller in light load conditions. Its highly accurate zero TC reference eliminates the need for precision external components in order to achieve tight tolerance voltage regulation. Through the use of the on-board DAC, the RC5042 can generate accurate output voltages from 2.1V up to 3.5V in 0.1V increments. An integrated Power Good function constantly monitors the output voltage and produces a low-going interrupt signal to the Pentium Pro CPU in the event of a out-of-tolerance voltage situation, thereby protecting the CPU. The programmable oscillator can operate from 200KHz to greater than 1MHz to provide for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs.

Block Diagram



Pin Assignments



65-5042-02

Pin Definitions

Pin Name	Pin Number	Pin Function Description
CEXT	1	External Capacitor for setting oscillator frequency
PWRGOOD	2	An open collector. Logic HIGH indicated power is within limits
IFB	3	Current Feedback Input
VFB	4	Voltage Feedback Input
VCCA	5	Analog VCC
VCCD	6	Digital VCC
GNDP	7	Power ground for high current drivers
HIDRV	8	High side FET driver output
VCCQP	9	VCC for High side FET output driver
GNDD	10	Digital ground
GNDA	11	Analog ground
VREF	12	Reference voltage output
VID3-VID0	13-16	Voltage identification code input

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage				13.2	V
V_{CCQP}	High FET Driver Supply				13.2	V
T_J	Junction Temperature				175	°C
T_A	Ambient Operating Temperature		0		70	°C
T_S	Storage Temperature		-65		150	°C
T_L	Lead Soldering Temperature	10 seconds			300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied.

Preliminary Information

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5	7	V
V_{CCQP}	Driver Supply Voltage		9	12	13.2	V
V_{IH}	Input Voltage, Logic HIGH		2			V
V_{IL}	Input Voltage, Logic LOW				0.8	V

DC Electrical Characteristics

(V_{CC} = 5V, V_{CCQP} = 12V, fosc = 650 KHz, and TA = +25°C unless otherwise noted. Refer to Figure 1.

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	See Voltage Identification Code Table, T_A = 0–70°C	2.1		3.5	V
Output Current			10		A
Set Point Accuracy	I_{LOAD} = 1A		0.25		%
Output Voltage Tempco			40		ppm/°C
Load Regulation	I_{load} = 0.5 to 10A		1		%Vo
Line Regulation	Input Voltage = 4.75 to 5.25V, I_{load} = 10A (See Figure 1)		0.14		%Vo
Output Voltage Ripple			30		mV
Cumulative Accuracy[1]	T_A = 25°C		2	3.5	%
Cumulative Accuracy[1]	T_A = 0–70°C		3	5	%
Efficiency	I_{load} = 10A	80	85		%
Power Dissipation			0.1	0.2	W
Output Current Driver		0.5	1.0		A

Notes:

1. Output Voltage Accuracy, Tempco, Load Regulation, Line Regulation, Ripple, &Transient Performance determine the Cumulative Accuracy.

AC Electrical Characteristics[1]

T_A = +25°C unless otherwise noted). Refer to Figure 1.

Parameter	Min	Typ	Max	Units
Response Time Sleep-to-Full Load		10		µs
Oscillator Frequency Range	.2		1.2	MHz
Oscillator Frequency Precision		10		%
Maximum Duty Cycle in PWM Mode	90	95		%
Minimum Duty Cycle in PFM Mode			100	ns
Short Circuit Detection Comparator Threshold	80	100		mV
Short Circuit Protection/Coil Saturation Detection, r_{sense} = 5mΩ		20		A
Short Circuit Current Foldback, r_{sense} = 5mΩ		14		A
Response Time to IMAX and Short Circuit Protection		15	30	ns
Soft Start during Power-Up and Power-Down		10		µs

Notes:

1. Guaranteed by characterization, not tested 100%.

Voltage Identification Codes

P6 Pins				VDC	Set Point (±mV)	Total Room Temperature Accuracy[1] (±mV)	Total System Accuracy[2] (±mV)
VID3	VID2	VID1	VID0				
1	1	1	1	No CPU	—	—	—
1	1	1	0	2.1	24	74	105
1	1	0	1	2.2	24	77	110
1	1	0	0	2.3	24	81	115
1	0	1	1	2.4	24	84	120
1	0	1	0	2.5	25	88	125
1	0	0	1	2.6	26	91	130
1	0	0	0	2.7	27	95	135
0	1	1	1	2.8	28	98	140
0	1	1	0	2.9	29	102	145
0	1	0	1	3.0	30	105	150
0	1	0	0	3.1	31	109	155
0	0	1	1	3.2	32	112	160
0	0	1	0	3.3	33	116	165
0	0	0	1	3.4	34	119	170
0	0	0	0	3.5	40	123	175

Notes:

1. Includes set point accuracy + line reg + load reg + transient (±mV).
2. Includes temperature effects to total accuracy (±mV).

Test Circuits

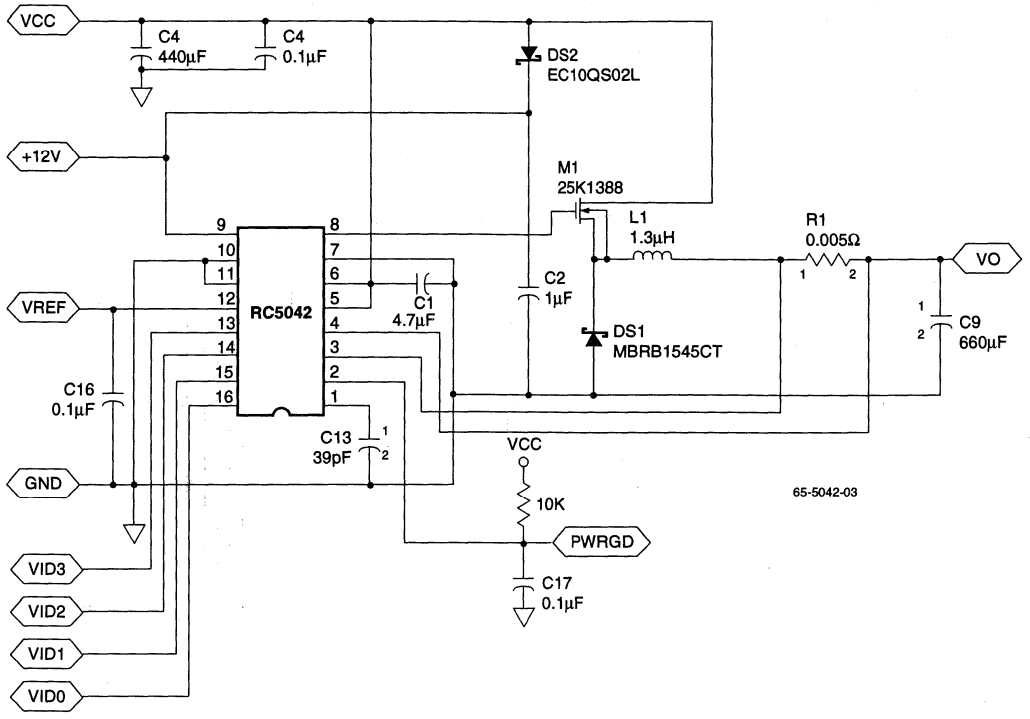


Figure 1. Standard Test or Application Schematic

Table 1. Components for RC5042

RC5042 Standard ApplicationCircuit Bill of Materials			
Ref Designator	**Quantity**	**Part No.**	**Manufacturer**
L1	1	CDRH127-1R3NC 1.3µH	Sumida
M1	2	25K1388	Fuji
DS1	1	MBRB1545CT	Motorola
DS2	1	EC10QS02L	Nihon
R1	1	LRC-2512 .005Ω	IRC
C4	2	OS-CON 10SA220M 220µF	Sanyo
C9	2	OS-CON 10SA330M 330µF	Sanyo
C1	1	1uF	Monolithic ceramic Cap
C13	1	39pF	SMD Cap
C16,C17	2	0.1uF	SMD Cap
R9	1	10K	SMD Resistor

PERSONAL COMPUTERS

Ordering Information

Product Number	Package	θJA
RC5042M	16 pin SOIC	80°C/W

RC5512

RAPPER™ Family – 4 Watt Stereo Sound Driver

Features

- Up to 4W/channel
- Drives 8Ω and 4Ω non-powered speakers
- NO-POP: during power-up/power-down and mute control
- Individual control pins to select mute and on/off for headphone, speaker, microphone, and regulator block
- Provides regulated 5V supply for sound codec, etc.
- Line output signal-to-noise ratio of 85dB
- Sleep mode supply current typically 10µA
- Microphone multiplexing
- Total harmonic distortion <0.1%
- Microphone amplifier with AGC 40dB dynamic range
- Internal Thermal Limiting Circuitry

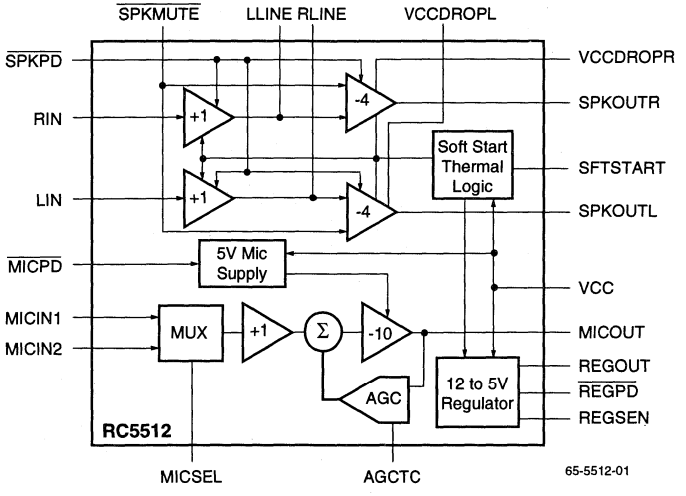
Applications

- Multimedia PC motherboards and add-in sound cards
- Portable multimedia personal computers
- Companion chip to Sigma-Delta Sound Codecs
- Sound Channel back-end in Set-top boxes

Description

The RC5512 can be used for driving key functions that are needed in all multimedia PCs and sound cards. These functions include directly powering speakers and headphone sets, providing a microphone pre-amplifier with AGC, and having a 12V to 5V regulator that can isolate the noise from the sound channel. Each function can be controlled individually, thus providing power saving features.

Block Diagram



Functional Description

The Rapper Stereo Sound Driver is an audio device that can be used on PC motherboards and add-in sound cards. It consists of stereo output drivers for headphone or speakers, a low noise microphone amplifier with AGC, and a regulator to provide a clean 5V supply. The RC5512 has two microphone inputs which are user selectable. Each section can be individually put into a shut-down mode and muted by pulling the appropriate pin low.

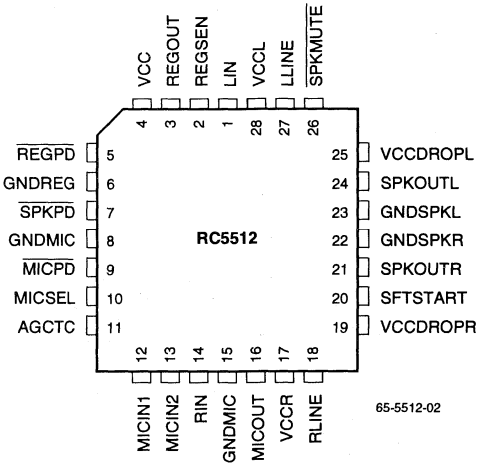
The output drivers can deliver up to 2 watts peak and 4 watts peak into 8Ω and 4Ω speakers, respectively, from a 12V source. The drivers use class AB amplifiers and maintain a low bias current. The power-down function is designed to save power and to turn on/off the driver without generating *popping* signals. To prevent popping signals, when the circuit is activated, a delay is provided to these output drivers. These drivers become active only after their outputs have settled. The time constant is user-defined through an external capacitor (C_{DELAY}) on the SFTSTART pin.

The microphone amplifier feeds into an AGC with a dynamic range of 40dB. An external capacitor is used to provide attack and decay features. Attack and decay times can be varied linearly by varying an external capacitor (C_{AD}) on the AGCTC pin. The attack and decay time ratio has been set for pleasant audio quality.

The 12 V to 5V voltage regulator can provide up to 20mA of current without external components. It can provide a noise-free regulated voltage supply to the other devices that complete the sound channel. Use of an external transistor can boost the regulator output to 150mA or higher with the appropriate thermal precautions. The line regulation of 50dB improves the cross talk and the power supply rejection ratio of all other audio blocks that are supplied by the 5V source.

The thermal limiting circuitry activates if the chip temperature typically exceeds 150°C.

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Description
LIN	1	Left Channel Input
REGSEN	2	Regulator Sense Point
REGOUT	3	Regulator 5V Output
VCC	4	12V Power Supply Input
$\overline{\text{REGPD}}$	5	Regulator Power-Down
GNDREG	6	Regulator Ground
$\overline{\text{SPKPD}}$	7	Speaker and Line Driver Power-Down
GNDMIC	8, 15	Microphone Ground
$\overline{\text{MICPD}}$	9	Microphone Power-Down
MICSEL	10	Microphone Output Select. LOW selects MICIN1, HIGH selects MICIN2
AGCTC	11	Attack and Decay Capacitor Pin
MICIN1	12	Microphone Input 1
MICIN2	13	Microphone Input 2
RIN	14	Right Channel Input
MICOUT	16	Microphone Output
VCCR	17	Right Speaker Supply
RLINE	18	Right Line Driver Output
VCCDROPR	19	Right Speaker Power Drop Supply
SFTSTART	20	Soft Start Timing Capacitor
SPKOUTR	21	Right Speaker Output
GNDSPKR	22	Right Speaker Ground
GNDSPKL	23	Left Speaker Ground
SPKOUTL	24	Left Speaker Output
VCCDROPL	25	Left Speaker Power Drop Supply
$\overline{\text{SPKMUTE}}$	26	Speaker Mute
LLINE	27	Left Line Driver Output
VCCL	28	Left Speaker Supply

Absolute Maximum Ratings[1]

(beyond which the device may be damaged)

Parameter		Min	Typ	Max	Units
VCC	Power supply voltage			13.2	V

Note:

1. Functional operation under any of these conditions is NOT implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
VCC VCCR VCCL	Power Supply		11.2	12	12.8	V
VCCDROPR VCCDROPL	Right and Left Power Drop Supplies	RDROP = 2Ω (See Figure 1)	11.2	12	12.8	V
V_{IH}	Input Voltage Logic High		2			V
V_{IL}	Input Voltage Logic Low				0.8	V
	Ambient Temperature		0		70	°C
T_C	Maximum Operation Die Temperature	Overthermal Protection		150		°C
I_{total}	Power Supply Current	No load		19	25	mA
I_{SD}	Shut-Down Current	$\overline{SPKPD}$, $\overline{MICPD}$, $\overline{REGPD} \leq 0.4V$		10	75	µA
ESD	ESD Threshold	Human Body Model	2000			V

Electrical Characteristics

VCC = 12V ± 6%, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
Line Driver		f = 1KHz,RL = 600Ω unless otherwise specified				
Zin	Input Impedance			10		KΩ
Av	Voltage Gain	V_{IN} = 0.5 Vrms	0.95	1.0	1.05	V/V
L&R Av	Left and Right Gain Matching	V_{OUT} = 4V_{P-P}		0.3		%
Vo	Output Voltage	RL = 600Ω		±4		V
THD	Total Harmonic Distortion	V_{OUT} = 4V_{P-P}		0.01		%
PSRR	Power Supply Rejection Ratio	f = 100Hz, ΔVcc = 0.85Vrms	80	86		dB
SNR	Signal-to-Noise Ratio	V_{IN} = 2.8Vrms		85		dB
Speaker Driver		f = 1KHz, RL = 8Ω unless otherwise specified				
Ispk	Speaker Driver and Line Driver Supply Current	V_{IN} = 0V		9		mA
Zin	Input Impedance		100			KΩ
Av	Voltage Gain	V_{IN} = 0.5 Vrms	-3.8	-4.0	-4.2	V/V
L&R Av	Left and Right Gain Matching	V_{OUT} = 4V_{P-P}		0.5		%
Vo	Output Voltage	RL = 4 Ω or 8Ω, VCC = 12V		±4		V_{pK}

Preliminary Information

Electrical Characteristics (continued)

VCC = 12V ± 6%, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
SNR	Signal-to-Noise Ratio	V_{IN} = 2.8Vrms		85		dB
Po	Power Output Per Channel Peak	RL = 4Ω, VCC = 12V		4		W
CS	Channel Separation L/R Input Referenced	V_{IN} = 0.5 Vrms	66			dB
XTALK	Cross Talk L/R to Mic Input Referenced	V_{IN} = 0.5 Vrms	90			dB
XTALK	Cross Talk L/R to Reg Input Referenced	V_{IN} = 0.5 Vrms	75			dB
THD	Total Harmonic Distortion	fo = 1KHz, Po = 50mW		0.1		%
Noise		20Hz - 20KHz, A-Weighted		4		µVrms
PSRR	Power Supply Rejection Ratio Input Referenced	f = 100Hz, ΔVCC = 1.6Vp-p	70	80		dB
Microphone Amplifier		f = 1KHz,RL = 10KΩ unless otherwise specified				
Imicamp	Microphone Amp Supply Current	V_{IN} = 0V, max gain		4		mA
Zin1	First Amp Input Impedance			4.5		KΩ
Av1	First Amp Gain			1		V/V
Av2	Second Amp Gain			-10		V/V
AGC	AGC Dynamic Range			40		dB
THD	Total Harmonic Distortion	Vin = 5mVP-P, AGC off		0.1		%
Noise		20Hz - 20KHz, A-Weighted		8		µVrms
XTALK	XTALK from other blocks at MICOUT	V_{IN} = 1Vrms at 1KHz	70			dB
PSRR	Input Referenced	f = 100Hz, ΔVCC = 1.6Vp-p	70			dB
Voltage Regulator						
Ireg	Voltage Regulator Supply Current			1.5		mA
Vreg	Regulator Voltage		4.75	5	5.25	V
Tc	Tempco			0.5		mV/°C
	Line Regulation			3		mV/V
	Load Regulation			2		mV/mA
Io	Output Current	Source		20		mA
		Source With External 2N2222		150		mA
		Sink		100		µA
Soft Start						
Delay	Anti-Pop Ramp-Up and Ramp-Down time	No Pop condition C_{DELAY} = 22µF on SFTSTART		2		sec

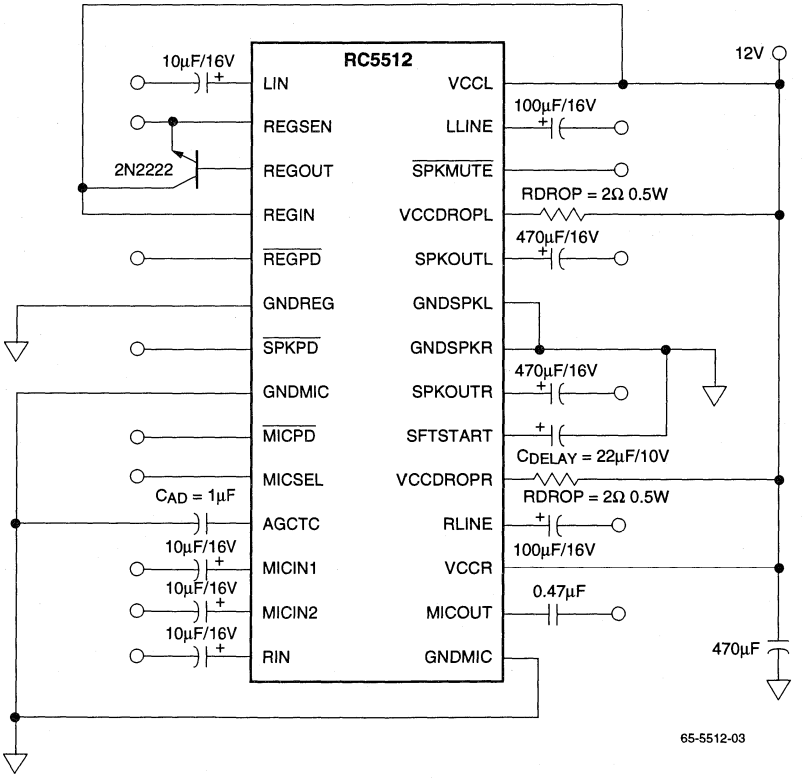
PERSONAL COMPUTERS

Power-Down Function Table

L = $V_{IL} \leq 0.8V$, H = $V_{IH} \geq 2.0V$, X = Don't Care

$\overline{SPKPD}$	$\overline{MICPD}$	$\overline{REGPD}$	$\overline{SPKMUTE}$	Function
L	L	L	X	Chip Disabled
H	H	H	H	All Sections Enabled
H	L	L	L	Line Driver Enabled, Regulator and Microphone Disabled, Speaker Muted
L	H	H	X	Line Driver and Speaker Disabled, Regulator and Microphone Enabled
H	L	H	H	Microphone Only Disabled
H	H	L	H	Regulator Only Disabled

Applications Discussion



Notes:

1. 4 Watt power represents the peak of the audio level and cannot be sustained without correct package thermal considerations. The average audio signal can be sustained by the RC5512 without extra thermal considerations.
2. To improve the thermal resistance of the PLCC 28 package, a heat sink can be used. One possible vendor is: AAVID, P/N CLC12059501.

Figure 1. Rapper™ RC5512, 4 Ohm Speaker, 4 Watt Application with External Pass Transistor for Voltage Regulator

Portable PC Application

Figure 2 shows an application of the RC5512 for portable PCs when a high current, regulated 12 volts is not available. Because the portable PC's battery voltage can exceed the VCC maximum specification of the RC5512, a low drop out linear regulator with power down has been included. The linear regualtor provides 12 volts of regulation even if the battery voltage exceeds 20 volts. In addition, the low drop out regulator allows good sound quality even when the battery voltage drops to 9 volts. The low power down current bias of the regulator minimizes the battery current drain when the RC5512 is in a sleep mode.

Alternatively, if a regulated 12 volt supply is available with a minimum current output of 300mA and sufficient by-pass capacitance, no additional regulation is required.

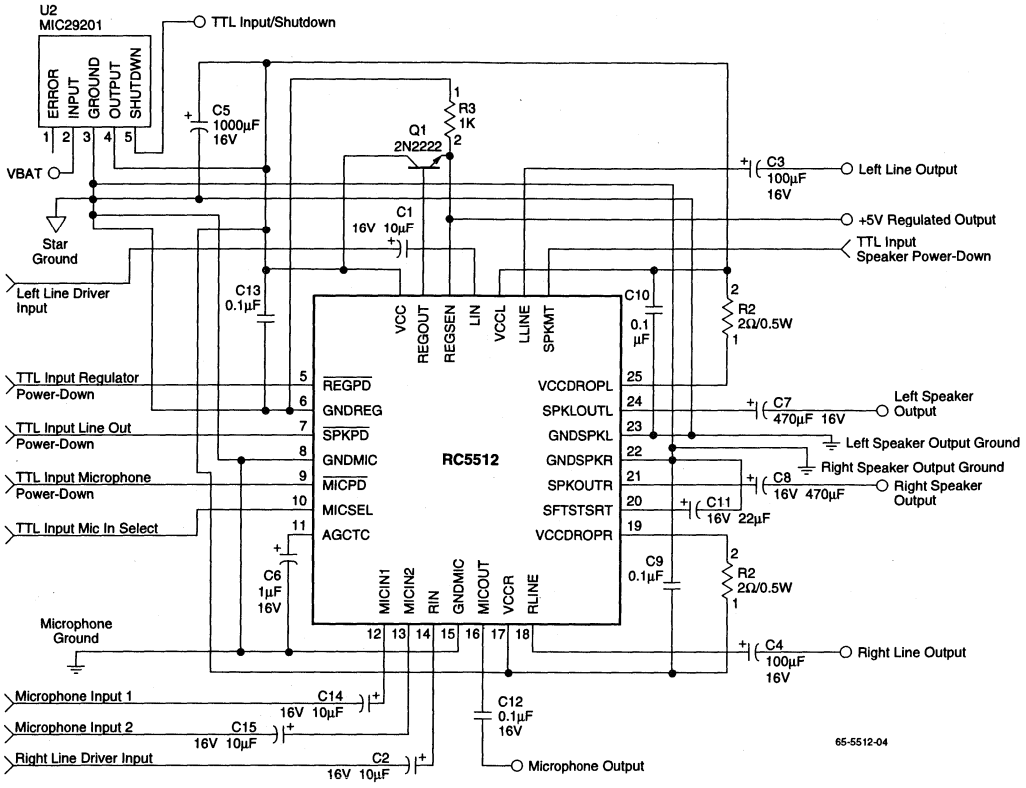


Figure 2. RC5512 Portable PC Application

Ordering Information

Product Number	Package
RC5512V	28 PLCC

RC5513

RAPPER™ Family – 4 Watt Stereo Sound Driver

Features

- Up to 4W/channel
- Drives 8Ω and 4Ω non-powered speakers
- NO-POP during power-up/power-down and mute
- Provides regulated 5V supply for sound codec, etc.
- Line Output signal to noise ratio of 85 dB
- Microphone amplifier and AGC dynamic range of 40dB
- Microphone multiplexing
- Internal thermal limiting circuitry
- 24 Lead SOIC package
- Total Harmonic Distortion < 0.1%

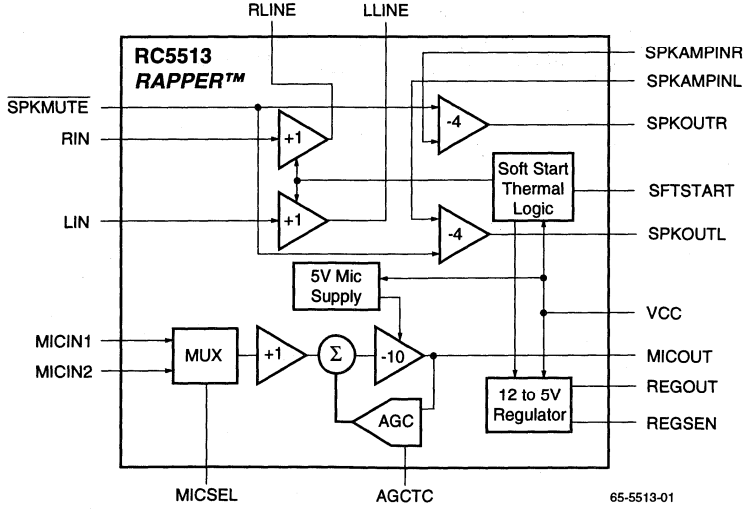
Applications

- Multimedia PC motherboards and add-in sound cards
- Companion chip to Sigma-Delta Sound Codecs
- Sound Channel back-end in Set-top boxes

Description

The Rapper is a stereo sound driver used for driving key functions that are needed in all multimedia PCs and sound cards. These functions include directly powering speakers and headphone sets, providing a microphone pre-amplifier with AGC, and having a 12V to 5V regulator that can isolate the noise from the sound channel.

Block Diagram



Functional Description

The Rapper Stereo Sound Driver is an audio device that can be used on PC motherboards and add-in sound cards. It consists of stereo output drivers for headphone or speakers, a low noise microphone amplifier with AGC, and a regulator to provide a clean 5V supply.

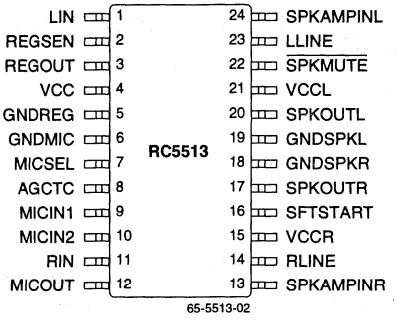
The output drivers can deliver up to 2 Watts peak and 4 Watts peak into 8Ω and 4Ω speakers, respectively, from a 12V source. The drivers use class AB amplifiers and maintain a low bias current. To help prevent popping signals a delay is provided to these output drivers to allow settling. The time constant is user-defined through an external capacitor (C_{DELAY}) on the SFTSTART pin.

The microphone amplifier feeds into an AGC with a dynamic range of 40dB. An external capacitor is used to provide attack and decay features. Attack and decay times can be varied linearly by varying an external capacitor (C_{AD}) on the AGCTC pin. The attack and decay time ratio has been set for pleasant audio quality.

The 12 V to 5V voltage regulator can provide up to 20mA of current without external components. It can provide a clean regulated voltage supply to the other devices that complete the sound channel. Use of an external transistor can boost the regulator output to 150mA or higher with the appropriate thermal precautions. The line regulation of 50dB improves the cross talk and the power supply rejection ratio of all other audio blocks that are supplied by the 5V source.

The thermal limiting circuitry activates if the chip temperature typically exceeds 150°C.

Pin Assignments



Preliminary Information

Pin Definitions

Pin Name	Pin Number	Pin Function Description
LIN	1	Left Channel Input
REGSEN	2	Regulator Sense Point
REGOUT	3	Regulator 5V Output
VCC	4	12V Power Supply Input
GNDREG	5	Regulator Ground
GNDMIC	6	Microphone Ground
MICSEL	7	MICOUT Select. LOW selects MICIN1, HIGH selects MICIN2
AGCTC	8	Attack and Decay Capacitor Pin
MICIN1	9	Microphone Input 1
MICIN2	10	Microphone Input 2
RIN	11	Right Channel Input
MICOUT	12	Microphone Output
SPKAMPINR	13	Right Channel Power Amplifier Input
RLINE	14	Right Line Driver Output
VCCR	15	Right Speaker Supply
SFTSTART	16	Soft Start Timing Capacitor
SPKOUTR	17	Right Speaker Output
GNDSPKR	18	Right Speaker Ground
GNDSPKL	19	Left Speaker Ground
SPKOUTL	20	Left Speaker Output
VCCL	21	Left Speaker Supply
$\overline{\text{SPKMUTE}}$	22	Speaker Mute
LLINE	23	Left Line Driver Output
SPKAMPINL	24	Left Channel Power Amplifier Input

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
VCC	Power supply voltage			13.2	V

Note:

1. Functional operation under any of these conditions is NOT implied. Performance is guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
VCC VCCR VCCL	Power Supply		11.2	12	12.8	V
V_{IH}	Input Voltage Logic High		2			V
V_{IL}	Input Voltage Logic Low				0.8	V
	Ambient Temperature		0		70	°C
T_C	Maximum Operation Die Temperature	Overthermal Protection		150		°C
I_{total}	Power Supply Current	No load		19	25	mA
ESD	ESD Threshold	Human Body Model	2000			V

Electrical Characteristics

V_{CC} = 12V ± 6%, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
Line Driver		f = 1KHz,RL = 600Ω unlees otherwise specified				
Zin	Input Impedance			10		KΩ
Av	Voltage Gain	Vin = 1 Vrms	0.95	1.0	1.05	V/V
L&R Av	Left and Right Gain Matching	Vout = $4V_{P-P}$		0.3		%
Vo	Output Voltage	RL = 600Ω		±4		V
THD	Total Harmonic Distortion	Vout = $4V_{P-P}$		0.01		%
PSRR	Power Supply Rejection Ratio	f = 100Hz, ΔVcc = 0.85Vrms	80	86		dB
SNR	Signal to Noise Ratio	Vin = 2.8V rms		85		dB
Speaker Driver		f = 1KHz, RL = 8Ω unless otherwise specified				
Ispk	Speaker Driver Supply Current	Vin = 0V		5		mA
Zin	Input Impedance		100			KΩ
Av	Voltage Gain	Vin = 0.5 Vrms	3.80	-4.0	-4.20	V/V
L&R Av	Left and Right Gain Matching	Vout = $4V_{P-P}$		0.5		%
Vo	Output Voltage	RL = 4Ω or 8Ω, VCC = 12V		±4		V
SNR	Signal to Noise Ratio	Input Referenced		85		dB
Po	Power Output Per Channel Peak	RL = 4Ω, VCC = 12V (See Figure 1)		4		W

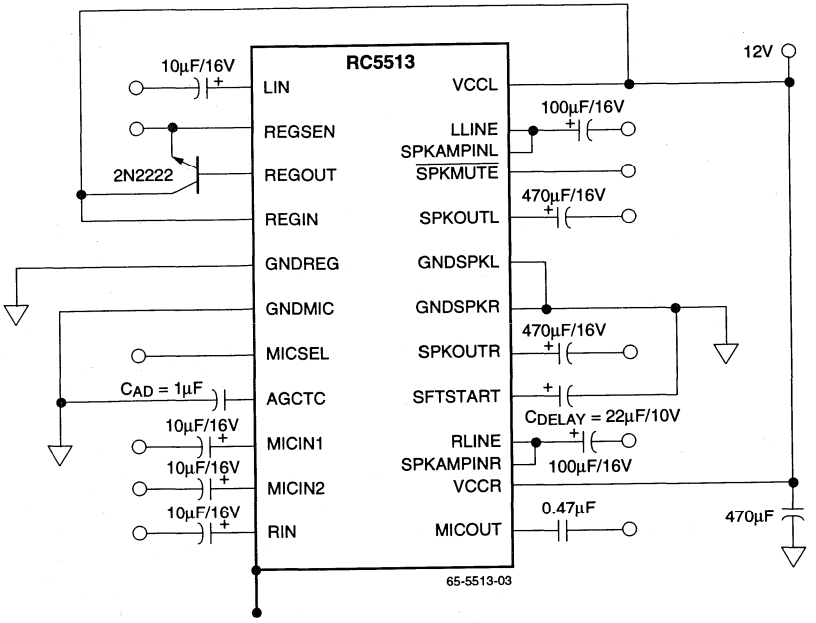
Preliminary Information

Electrical Characteristics (continued)

V_{CC} = 12V ± 6%, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
CS	Channel Separation L/R Input Referenced	Vin = 0.5 Vrms	66			dB
XTALK	Cross Talk L/R to Mic Input Referenced	Vin = 1 mVrms	90			dB
XTALK	Cross Talk L/R to Reg Input Referenced	Vin = 0.5 Vrms	75			dB
THD	Total Harmonic Distortion	fo = 1KHz, Po = 50mW		0.1		%
Noise		20Hz to 20kHz, A-Weighted		4		µVrms
PSRR	Power Supply Rejection Ratio Input Referenced	f = 100Hz, ΔVcc = 1.6Vp-p	70	80		dB
Microphone Amplifier		f = 1KHz,RL = 10KΩ unless otherwise specified				
Imicamp	Microphone Amp Supply Current	Vin = 0V, max gain		4		mA
Zin1	First Amp Input Impedance			4.5		KΩ
Av1	First Amp Gain			1		V/V
Av2	Second Amp Gain			-10		V/V
AGC	AGC Dynamic Range			40		dB
THD	Total Harmonic Distortion	Vin = 5mVP-P, AGC off		0.1		%
Noise		20Hz to 20kHz, A-Weighted		8		µVrms
XTALK	XTALK from other blocks at MICOUT	Vin = 1Vrms at 1KHz	70			dB
PSRR	Input Referenced	f = 100Hz, ΔVcc = 1.6Vp-p	70			dB
Voltage Regulator						
Ireg	Voltage Regulator Supply Current			1.5		mA
Vreg	Regulator Voltage		4.75	5	5.25	V
Tc	Tempco			0.5		mV/°C
	Line Regulation			3		mV/V
	Load Regulation			2		mV/mA
Io	Output Current	Source		20		mA
		Source With External 2N2222		150		mA
		Sink		100		µA
Soft Start						
Delay	Anti-Pop Ramp-Up and Ramp-Down time	No Pop condition C_{DELAY} = 22µF on SFTSTART		2		sec

Applications Discussion



Notes:

1. 4 watt power represents the peak of the audio level and cannot be sustained without correct package thermal considerations. The average audio signal can be sustained by the RC5513 without extra thermal considerations.
2. To improve the thermal resistance of the SOIC package a heat sink can be used.

Figure 1. Rapper™ RC5513, 4 Ohm Speaker, 4 Watt Application with External Pass Transistor for Voltage Regulator

Ordering Information

Product Number	Package
RC5513M	24 SOIC

Preliminary Information

TMC2360

Video Output Processor

VGA to NTSC/PAL

Features

- Single-package graphics to video conversion
- Multiple input formats
  - 640x480 50/60 Hz, 800x600 50 Hz
- Multiple output standards
  - NTSC, NTSC-EIA, PAL-B/G/H/I, PAL-M
- Composite and S-video output formats
- No external memory required
- Horizontal and vertical positioning inputs
- Configuration set by 11 switches
  - Microcontroller port optional
- Internal color bars
- 3-channel 8-bit input digitizer
- 3-channel 9-bit output D/A converters
- Accepts programming through H and V timing
  - VESA DPMS, filter modes, video standard
- Single +5V power supply

Applications

- VGA to video converter modules
- Computer video outputs
- Video games

PERSONAL COMPUTERS

Description

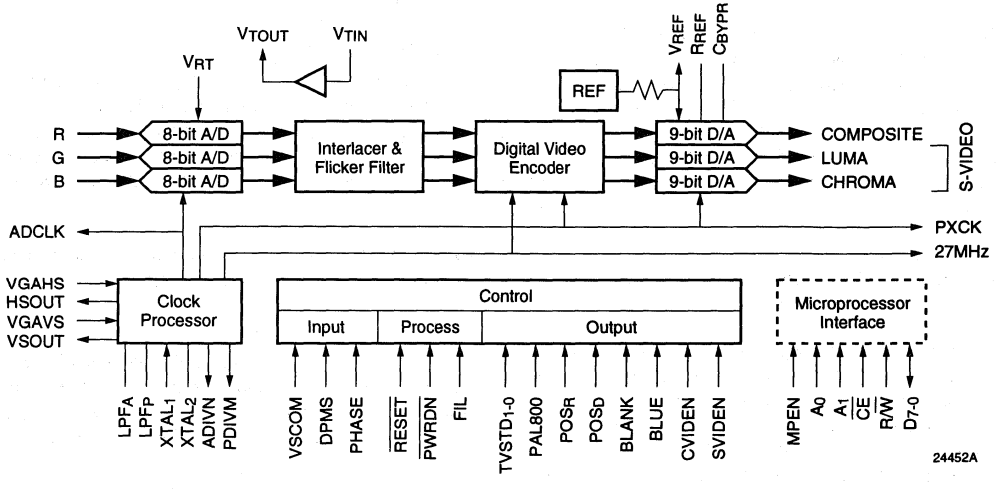
The TMC2360 converts RGB video and sync from a standard VGA source into broadcast-quality NTSC or PAL video. Composite and S-Video outputs are compliant with SMPTE-170M and CCIR-656 specifications. A fully-integrated 3-line adaptive flicker filter provides three selectable operating modes.

System implementation requires an absolute minimum of external components, with critical timing derived from a single 27 MHz crystal or an external clock reference.

All functions are directly controlled via package pins. Some functions, including video and filtering modes may be programmed through either a microcontroller port or VSYNC timing. VESA Display Power Management Signaling (DPMS) is supported.

Powered from a single +5V supply, the TMC2360 is available in an 80-lead Metric Quad Flat Pack (MQFP) and an 84-lead Plastic Leadless Chip Carrier (PLCC).

Block Diagram



Rev. 0.9.1

Functional Description

The TMC2360 is a VGA to Video converter capable of producing broadcast-quality signals conforming to NTSC and PAL standards using a single low-cost application circuit. Included is all of the active circuitry required to generate a television signal with outstanding image quality in a stand-alone application.

Incoming VGA source signals must be 2X the frame and 2X the line rate of the outgoing TV standard within a ±2% tolerance. Supported VGA formats are 640x480 at 60 Hz for NTSC and PAL-M, and 640x640 and 800x640 at 50 Hz for PAL B/G/H/I.

The TMC2360 is ideal for portable converter applications, as well as integration into notebook and palmtop computers and video games.

Input Section

Analog VGA signals are digitized by three 8-bit A/D converters, operating at rates of up to 36 Ms/s. The signal range is 0 to 700 mV established by the reference voltage, V_{RT}.

By connecting V_{TOUT} to V_{IN}, V_{RT} may be supplied by an on-chip voltage follower with an input, V_{TIN}, that may be varied from 0 to 2 volts to accommodate different input levels.

Clock Processor

Two phase-locked loops synthesize clocks from the VGA Horizontal Sync signal. One loop generates ADCLK, which is used internally as the A/D sample clock. A second PLL generates PXCK, which is used internally as the digital encoder clock.

Either internal or external phase-locked loops may be selected by programming pins A_1 and A_0. For internal loops, loop filters must be connected to LPF_A and LPF_P.

With external phase-locked loops, the internal divide by N and divide by M counters are still used. Only the phase detector, charge pump and VCO need be located in the external controller.

A stable timebase reference for subcarrier generation is derived from a 27 MHz crystal, or a TTL clock applied to pin $XTAL_1$.

To synchronize the video encoder, vertical timing is derived from VGAVS, the VGA vertical sync signal. VGAHS and VGAVS signals of either polarity are accepted.

VESA Display Power Management Signaling functions may be enabled with the DPMS pin. Using the DPMS protocol, operational commands may be communicated to the TMC2360 via VGAHS and VGAVS signals. DPMS STAND-BY or DPMS SUSPEND modes set the processor to sleep and blanks the screen. DPMS OFF sets the processor, A/Ds and D/As to sleep with a blanked screen.

Vertical Sync Communications may be enabled with the VSCOM pin to detect the number of VGAHS pulses during the VGAVS period. With VSCOM, the Flicker Filter mode and the Video Standard may be selected by commands communicated via the VGA sync signals.

Flicker Filter

Flicker may be traded off against vertical resolution with a three-line adaptive flicker filter. A single toggle pin (FIL) selects either High Filter, Medium Filter, or No Filter modes. A fourth mode, Color Bars, is useful for video setup and as a reference point for filter selection.

Video Encoder

Unless VSCOM is enabled, $TVSTD_{1-0}$ pins select the TV standard to be either NTSC, PAL or PAL-M.

Relative to the bezel framed by horizontal and vertical sync, the image may be moved right/left, and down/up by pulsing the POS_R and POS_D pins. BLANK suppreses the image, setting the screen either black or blue according to the state of the BLUE pin.

NTSC (SMPTE 170M) and PAL (CCIR 624) video signals are produced by three 9-bit D/A converters that can drive the 37.5Ω load of a double-terminated 75Ω line. Digital 2X oversampling minimizes sinX/X distortion, facilitating use of low-cost output filters.

Composite and S-Video D/As are independently enabled via CVIDEN and SVIDEN pins to minimize power dissipation.

Control Processor

TMC2360 setup and control is derived from external switches and push buttons. Schmitt trigger inputs reject external noise. Unused controls may be preset by hardwiring inputs to ground or V_{CC}.

Encoder Output Current

Output current is established by V_{REF} and an external resistor connected between R_{REF} and ground. An internal 1.235 volt reference is buffered from V_{REF} by a resistor, so V_{REF} may be overridden by an external voltage. Output current may be calibrated by resistor selection or setting a potentiometer attached to R_{REF}.

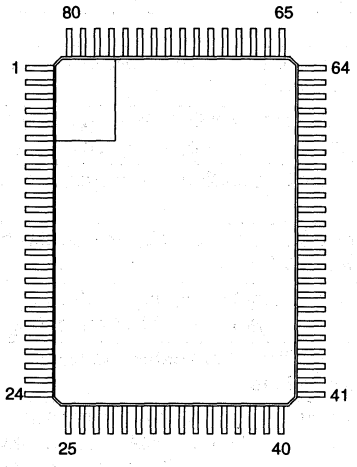
To minimize DAC noise, a bypass capacitor must be connected from C_{BYPR} to an adjacent V_{DDA} pin.

Microprocessor Port

Instead of utilizing control pin inputs, two operational modes, TV Standard and Flicker Filter, may be selected by writing to the VGA control register. Five registers may be read: address, VGA0, VGA1, Revision ID and Part ID.

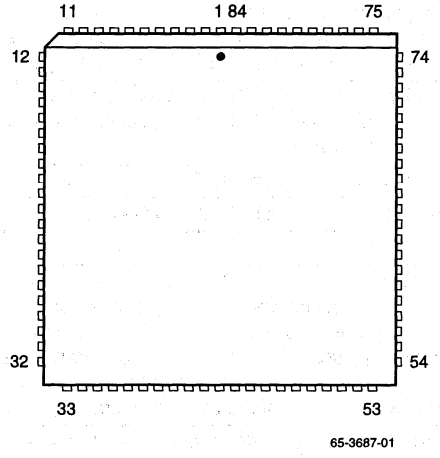
Pin Assignments

80-Lead MQFP (KL) Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AGND	21	D_4	41	PAL800	61	DGND
2	COMPOSITE	22	D_3	42	FIL	62	V_{DD}
3	R_{REF}	23	D_2	43	DPMS	63	AGND
4	V_{REF}	24	D_1	44	VSCOM	64	LPF_A
5	DGND	25	D_0	45	VGAVS	65	V_{DDPLLA}
6	PHASE	26	VSOUT	46	VGAHS	66	AGND
7	V_{DD}	27	HSOUT	47	POS_R	67	LPF_P
8	DGND	28	DGND	48	POS_D	68	V_{DDPLLP}
9	V_{DD}	29	V_{DD}	49	AGND	69	$XTAL_2$
10	DGND	30	MPEN	50	B	70	$XTAL_1$
11	27MHZ	31	A_1	51	V_{DDA}	71	$\overline{RESET}$
12	PXCK	32	A_0	52	V_{DDA}	72	$\overline{PWRDN}$
13	ADCLK	33	$R/\overline{W}$	53	G	73	SVIDEN
14	V_{DD}	34	$\overline{CE}$	54	AGND	74	CVIDEN
15	DGND	35	V_{DD}	55	V_{RT}	75	V_{DDA}
16	ADIVN	36	DGND	56	V_{TOUT}	76	V_{DDA}
17	PDIVM	37	BLUE	57	V_{TIN}	77	C_{BYPR}
18	D_7	38	BLANK	58	AGND	78	CHROMA
19	D_6	39	$TVSTD_1$	59	R	79	AGND
20	D_5	40	$TVSTD_0$	60	V_{DDA}	80	LUMA

84-Lead PLCC (R0) Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	$\overline{PWRDN}$	22	ADCLK	43	A_0	64	G
2	SVIDEN	23	V_{DD}	44	$R/\overline{W}$	65	AGND
3	CVIDEN	24	DGND	45	$\overline{CE}$	66	V_{RT}
4	V_{DDA}	25	ADIVN	46	V_{DD}	67	V_{TOUT}
5	V_{DDA}	26	PDIVM	47	DGND	68	V_{TIN}
6	C_{BYPR}	27	D_7	48	BLUE	69	AGND
7	CHROMA	28	D_6	49	BLANK	70	R
8	AGND	29	D_5	50	$TVSTD_1$	71	V_{DDA}
9	LUMA	30	D_4	51	$TVSTD_0$	72	DGND
10	AGND	31	D_3	52	PAL800	73	V_{DD}
11	COMPOSITE	32	DNC	53	FIL	74	DNC
12	R_{REF}	33	DNC	54	DPMS	75	DNC
13	V_{REF}	34	D_2	55	VSCOM	76	AGND
14	DGND	35	D_1	56	VGAVS	77	LPF_A
15	PHASE	36	D_0	57	VGAHS	78	V_{DDPLLA}
16	V_{DD}	37	VSOUT	58	POS_R	79	AGND
17	DGND	38	HSOUT	59	POS_D	80	LPF_P
18	V_{DD}	39	DGND	60	AGND	81	V_{DDPLLP}
19	DGND	40	V_{DD}	61	B	82	$XTAL_2$
20	27MHZ	41	MPEN	62	V_{DDA}	83	$XTAL_1$
21	PXCK	42	A_1	63	V_{DDA}	84	$\overline{RESET}$

PERSONAL COMPUTERS

Pin Descriptions

Pin Name	Pin Number MQFP	Pin Number PLCC	Type/ Value	Pin Function Description
Clocks				
ADCLK	13	22	TTL	**A/D Converter Clock Output.** Generated by an internal phase-locked loop slaved to VGAHS.
ADIVN	16	25	TTL	**Internal ADCLK divided by N Output.** Enabled by A_0 and A_1 pins according to Table 1 or by VGA Control Register 1.
LPF_A	64	77	—	**A/D PLL Loop Filter Connection.** An external RC network is connected here.
PXCK	12	21	TTL	**Encoder Clock Output.** Generated by an internal phase-locked loop slaved to VGAHS.
PDIVM	17	26	TTL	**Internal PXCK divided by M Output.** Enabled by A_0 and A_1 pins according to Table 1 or by VGA Control Register 1.
LPF_P	67	80	—	**Encoder PLL Loop Filter Connection.** An external RC network is connected here.
$XTAL_{1-2}$	70,69	83, 82	—	**Subcarrier Reference Crystal/Clock.** Connection terminals for an external 27 MHz crystal. Alternatively, the $XTAL_1$ pin may be used as an input from an external oscillator or clock. Subcarrier frequency accuracy is based on this clock.
27MHZ	11	20	TTL	**Subcarrier Reference Clock Output.** Buffered TTL output from 27MHz crystal oscillator/reference clock.
VGAHS	46	57	$CMOS_S$	**VGA Horizontal Sync.** Incoming VGA sync may be of either polarity (active LOW or active HIGH). VGAHS frequency must be within 2% of the nominal specified value. The VGAHS pin has a light pull-up and a Schmitt trigger.
VGAVS	45	56	$CMOS_S$	**VGA Vertical Sync.** Incoming VGA sync may be of either polarity (active LOW or active HIGH. The VGAVS pin has a light pull-up and a Schmitt trigger.
HSOUT	27	38	TTL	**Buffered Horizontal Sync Output.** Follows VGAHS.
VSOUT	26	37	TTL	**Buffered Verical Sync Output.** Follows VGAVS.
Global Controls				
$TVSTD_{1-0}$	39, 40	50, 51	$CMOS_P$	**Video Output Standard Select.** Preprogrammed into the TMC2360 are timing, subcarrier frequency and phase parameters corresponding to worldwide NTSC and PAL standards. $TVSTD_{1-0}$ select one of four sets of parameters to set up the encoder. Frame rate of the graphics source must be twice the frame rate of the selected video standard.
PAL800	41	52	$CMOS_P$	**Resolution select for PAL.** Sets number of samples per VGA line.
DPMS	43	54	$CMOS_P$	**Display Power Management Signaling Enable.** When HIGH, the operational state of the TMC2360 is controlled by the pulse activity on VGAHS and VGAVS. When LOW, the state of the TMC2360 is controlled only by input pins.
FIL	42	53	$CMOS_S$	**Flicker Filter Mode Select.** The adaptive flicker reduction filter may be configured for HIGH filtering, MEDIUM filtering, or NO filtering by pulsing this input HIGH. FIL defaults to HIGH-filter mode upon power-up. If VSCOM is HIGH, the filter mode will be selected by the pulsewidth of VGAVS, and FIL will be ignored. The FIL input is a Schmitt trigger.

Pin Descriptions (continued)

Pin Name	Pin Number MQFP	Pin Number PLCC	Type/ Value	Pin Function Description
VSCOM	44	55	CMOSP	**Vertical Sync Communications Enable.** When HIGH, vertical sync pulse width (VGAVS) will control the filter mode, and FIL will be ignored.
$\overline{\text{PWRDN}}$	72	1	CMOSP	**Power-Down Control.** When HIGH, the TMC2360 is fully operational and enabled. When LOW, the TMC2360 is configured for minimum power consumption. D/A converters and clocks are disabled. Previously established set-up conditions are retained and remain in effect when $\overline{\text{PWRDN}}$ goes HIGH.
$\overline{\text{RESET}}$	71	84	CMOSP	**Reset.** Initializes internal registers.
PHASE	6	15	CMOSP	**Sampling Phase Control.** Shifts the A/D sampling phase by 180°.
Encoder Controls				
CVIDEN	74	3	CMOSP	**Composite Video D/A Power Enable.** When HIGH, the COMPOSITE D/A converter is enabled. When LOW it is disabled to save power.
SVIDEN	73	2	CMOSP	**S-Video D/A Power Enable.** When HIGH, the CHROMA and LUMA D/A converters are enabled. When LOW, they are disabled to save power.
BLANK	38	49	CMOSP	**Blank Screen Generator.** When HIGH, the color selected by BLUE is displayed on the screen. When LOW, incoming video from the internal FIFO is encoded.
BLUE	37	48	CMOSP	**Blank Screen Color Selector.** When HIGH, the screen will be blanked to blue when BLANK is HIGH. When LOW, the screen will be blanked to black when BLANK is HIGH.
$\text{POS}_{R,D}$	47, 48	58, 59	CMOSS	**TV Image Position Controls.** Position controls shift the VGA image horizontally or vertically, revealing portions that are found near the edges or in the overscan areas. Default power-up position is the midpoint of the adjustment range. $\text{POS}_{D,R}$ inputs are Schmitt triggers.
A/D Converter Interface				
R, G, B	59, 53, 50	70, 64, 61	700 mV	**Analog RGB inputs.** Analog red, blue and green inputs to the A/D converters from incoming VGA signals. Nominal voltage range is 0.0 to +700 mV.
V_{TIN}	57	68	750 mV	**A/D Converter Reference Buffered Input.** Buffer is a voltage follower that may be connected to V_{RT}.
V_{TOUT}	56	67	750 mV	**A/D Converter Reference Buffered Output.** May be connected to V_{RT} to suppliy current to A/D converter reference resistors. In power down mode, V_{TOUT} drops to zero.
V_{RT}	55	66	750 mV	**A/D Converter Reference Input, Unbuffered.** Supplies current to A/D converter reference resistors. May be driven from V_{TOUT}. Voltage range is 0.5 to 2.0 volts.

Pin Descriptions (continued)

Pin Name	Pin Number MQFP	Pin Number PLCC	Type/ Value	Pin Function Description
Video Outputs				
COMPOSITE	2	11	1 V p-p	**NTSC/PAL Video Output, Composite Video.** NTSC/PAL baseband composite output can drive 1 Volt p-p video into a 37.5 Ohm load. Contains sync, subcarrier and active video information to drive monitors, projectors, VCRs, and other video devices.
LUMA	80	9	1 V p-p	**Luminance-only Video.** This analog monochrome video output can drive 1 Volt p-p video into a 37.5 Ohm load. Contains all sync and active video information necessary to drive black-and-white video devices.
CHROMA	78	7	1 V p-p	**Chrominance-only Video.** This analog output can drive a 37.5 Ohm load. CHROMA signal, when combined with LUMA comprises an S-Video signal suitable for driving monitors, projectors, VCRs, and other S-Video devices.
Voltage Reference				
V_{REF}	4	13	+1.23 V	**Voltage Reference Input/Output.** Output of an internal 1.23 Volt band-gap voltage reference. If unconnected, except for a 0.1F capacitor to ground for noise decoupling, the internal reference will be used for the three D/A converters. An externally generated voltage reference of +1.2 Volts applied to the V_{REF} pin will override the internal voltage reference and become the new reference for the D/A converters.
C_{BYPR}	77	6	0.1 µF	**Reference Bypass Capacitor.** An external 0.1F capacitor should be connected between C_{BYPR} and V_{DDA} to reduce noise on the internal reference circuitry.
R_{REF}	3	12	392Ω	**Current-setting Resistor.** A 392Ω resistor connected between the R_{REF} terminal and ground establishes the reference current for the three internal D/A converters. Resistor value determines the full-scale output current (and therefore the peak video level) of the D/A converters.
Microprocessor Interface				
MPEN	30	41	TTL	**Microprocessor port enable.** With MPEN = LOW, the port is disabled and control is via individual pins. With MPEN = HIGH, selected functions may be accessesd through the microprocessor port.
A_0	32	43	TTL	**External PXCK Phase-locked Loop Select/Address Bit.** Dual function pin. If MPEN = HIGH, A_0 is the microprocessor port address bit A0. If MPEN = LOW, A_0 configures the PXCK PLL inputs and outputs.
A_1	31	42	TTL	**External ADCLK Phase-locked Loop Select.** If MPEN = LOW, A1 configures the ADCLK PLL inputs and outputs.
$R/\overline{W}$	33	44	TTL	**Read/Write.** Read/Write selects the direction of the 8-bit data bus.
$\overline{CE}$	34	45	TTL	**Chip Enable.** When $\overline{CE}$ = H, D_{7-0} are high impedance. When $\overline{CE}$ = H, $R/\overline{W}$ sets D_{7-0} to either the read or write state.

Pin Descriptions (continued)

Pin Name	Pin Number MQFP	Pin Number PLCC	Type/ Value	Pin Function Description
D_{7-0}	18, 19, 20, 21, 22, 23, 24, 25	27, 28, 29, 30, 31, 34, 35, 36	TTL	**Data bits.** Data bus is high impedance unless $\overline{CE}$ = L and R/$\overline{W}$ = H.
Power and Ground				
V_{DD}	7, 9, 14, 29, 35, 62,	16, 18, 23, 40, 46, 73	+5.0 V	**Digital Power Supply.** Supplies +5V power to internal digital circuits.
V_{DDA}	51, 52, 60, 75, 76	4, 5, 62, 63, 71	+5.0 V	**Analog Power Supply.** Supples +5V power to internal analog circuits. V_{DD} and V_{DDA} must originate from the same source.
V_{DDPLLA}	65	78	+5.0 V	**A/D Phase Locked Loop +5V Power.** V_{DDPLLA} and V_{DD} must originate from the same source.
V_{DDPLLP}	68	81	+5.0 V	**Encoder Phase Locked Loop +5V Power.** V_{DDPLLP} and V_{DD} must originate from the same source.
DGND	5, 8, 10, 15 28, 36, 61	14, 17,19, 24, 39, 47, 72	0.0 V	**Digital Ground.** Ground point for internal digital circuits.
AGND	1, 49, 54, 58, 63, 66, 79	8, 10, 60, 65, 69, 76, 79	0.0 V	**Analog Ground.** Ground point for internal analog circuits. DGND and AGND should be connected to the same ground plane.
DNC	—	32, 33, 74, 75		Do Not Connect.

Notes:
$CMOS_P$ = CMOS with light pull-up
$CMOS_S$ = CMOS with Schmitt Trigger

Clocks

There are three internal clocks, ADCLK, PXCK, and 27MHz. ADCLK is the clock for the A/D converters with sampling on the edge selected by PHASE. PXCK is the encoder clock for sequencing data to the D/A converters at a 2X rate. 27MHz is the reference clock from which the chroma subcarrier data is synthesized.

ADCLK and PXCK clocks may be derived from internal or external phase-locked loops. Only an external controller containing the phase detector, charge pump, and VCO is needed for each loop. An internal divider programmed with the correct counts is included within the TMC2360.

Control of the internal/external PLL modes is either via the A_0 and A_1 pins (see Table 1) or through the VGA1 Control register, which can be programmed via the microprocessor port.

With control via A_0 and A_1 pins, outputs, PDIVM and ADIVN are high impedance unless either PLL is programmed to be external. A_0 and A_1 also control the direction of the ADCLK and PXCK clock pins. Each clock (ADCLK and PXCK) is an output in the internal mode and an output in the external mode.

Table 1. Internal/External Phase-locked loop selection (MPEN = L)

A_1	A_0	PLLA	PLLP	ADIVN	PDIVM	ADCLK	PXCK
0	0	Internal	Internal	High-Z	High-Z	Output	Output
0	1	Internal	External	1/N	1/M	Output	Input
1	0	External	Internal	1/N	1/M	Input	Output
1	1	External	External	1/N	1/M	Input	Input

A/D Clock (ADCLK)

ADCLK is the buffered analog-to-digital converter clock output which is derived from incoming VGA horizontal sync (VGAHS) by a phase-lock loop (PLL). Either an internal PLL or an external PLL controller may be selected by programming pin A1.

A/D Clock frequency is set by the PLL divide-by-N counter where N is the number of A/D samples between the horizontal sync pulses in each VGA line.

Pre-programmed values selected by the $TVSTD_{1-0}$ and PAL800 control inputs set N and the clock frequency as shown in Table 2.

Table 2. VGA A/D Clock

Television Standard	$TVSTD_{1-0}$	PAL800	ADCLK Freq. (MHz)	N
NTSC	0x	0	25.175	800
PAL640	10	0	25.250	808
PAL800	10	1	36.000	1152
PALM	11	0	25.175	800

For an internal loop, the recommended loop filter to be connected to the LPF_A pin is shown in Figure 1.

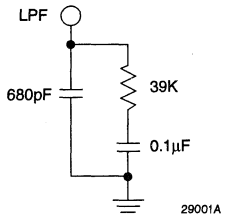


Figure 1. PLL Low Pass Filter

Pixel Clock (PXCK)

PXCK is the buffered video encoder clock output which is derived from the incoming VGA HSYNC signal by a second phase-lock loop. Either an internal PLL or an external PLL controller may be selected by programming pin A_0.

With the internal loop selected, Figure 1 shows the recommended loop filter, which should be connected to LPF_P.

Clock frequency is set by the PLL divide-by-M counter. M is the number of encoder samples between horizontal sync pulses. Because of 2X oversampling, the pixel rate is twice the TV square pixel rate. Table 3 shows the video output clock rates and M values.

Table 3. NTSC and PAL Pixel Clocks

Television Standard	Line Rate (kHz)	Pixel Rate (MHz)	M
NTSC	15.734	24.540	780
PAL	15.625	29.500	944
PALM	15.750	24.570	780

Reference Clock

Accuracy of the PAL/NTSC subcarrier depends on the 27 MHz reference signal applied to the $XTAL_1$. This signal may be derived from a clock connected directly to the $XTAL_1$ pin or a crystal and capacitors connected across $XTAL_{1-2}$ as shown in Figure 2.

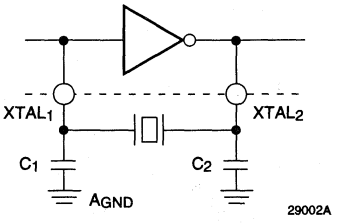


Figure 2. Crystal Oscillator Circuit

Capacitors C_1 and C_2, must be adjusted to trim the frequency within 20 ppm. C_1 and C_2 have the same value, with series capacitance equal to the load recommended for the crystal.

Typical crystal parameters are 50 ppm accuracy with a 20 pF load and ±80 ppm pullability.

Digitizing

A/D Reference

An on-chip voltage follower is included to supply current to the ADC reference V_{RT} from V_{TOUT}. A stable voltage source greater than the input peak amplitude should be connected to V_{TIN}.

Input Signal Conditioning

ADC performance can be optimized by driving the RGB video inputs with either a 75 ohm or a low impedance source.

Input Format Selection

One of four input VGA formats can be accepted by setting the $TVSTD_{1-0}$ and PAL800 inputs as shown in Table 4. Each VGA input option corresponds to a VGA active video area, frame rate and line rate with a corresponding TV output format.

Table 4. VGA Input Formats

$TVSTD_{1-0}$	PAL800	H x V Input Pixels	Frame Rate (Hz)	Line Rate (kHz)
0x	0	640 x 480	59.94	31.469
10	0	640 x 480	50	31.250
10	1	800 x 600	50	31.250
11	0	640 x 480	60	31.469

Sampling Phase Control

Conversion can be optimized by using the PHASE control to set the sampling points of the A/D clock to lie between the VGA pixel transitions. Figure 3 shows optimum sampling of VGA pixels on the rising edge of the ADCLK signal.

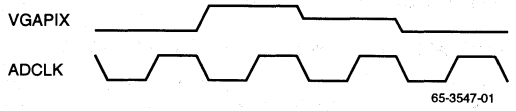


Figure 3. Sampling of VGA Pixels

PHASE selects the conversion edge of the ADCLK. If PHASE = LOW, the rising edge is selected. If PHASE = HIGH, the falling edge is selected.

Processing

Flicker Filter

Annoying artifacts can be eliminated by selecting one of three filter modes, which trade-off vertical resolution against flicker. Without the filter, one contrasting VGA line may be encoded into one field of the TV video, which will flicker at 30 Hz with NTSC and 25 Hz with PAL.

As shown in Table 5, if VSCOM = LOW, pulsing the FIL pin indexes the TMC2360 through a loop of three filter modes and a color bar pattern.

Table 5. FIL Filter Mode Select Sequence

FIL	Filter Mode
↓ ▲	HIGH (default)
↓	MEDIUM
↓	No filter
└	Color bars

Video Encoder

D/A Reference

Peak D/A converter current for the video outputs is set by a resistor connected to R_{REF}. For 1 volt video, with a 37.5 ohm load, the correct value of R_{REF} is 392 ohm. To trim the video output level, R_{REF} can be replaced with a potentiometer. (See the Applications Circuit, Figure 12).

Television Standard Selection

NTSC and PAL standards are preprogrammed into the TMC2360 to preset horizontal and vertical timing, subcarrier frequency, and chrominance phase. Frame rate of the VGA source must match the field rate of the selected video standard.

Depending upon the status of the Vertical Sync Communications (VSCOM) pin, the video output format may be selected by either the $TVSTD_{1-0}$ pins or by VSCOM codes.

Table 6 shows how the $TVSTD_{1-0}$ pins select the TV output format with VSCOM = LOW.

Table 6. TVSTD Control When Under Manual Control (VSCOM = 0)

$TVSTD_{1-0}$	Television Standard	Video Field Rate
00	NTSC	59.94 Hz
01	NTSC-EIA	59.94 Hz
10	PAL/B, G, I	50 Hz
11	PAL/M	60 Hz

If VCSOM = HIGH, Vertical Sync Communications are enabled. VSCOM is described under the Vertical Sync Command section below.

Image Positioning

POS_D and POS_R position controls change encoder timing relative to incoming PC video, shifting the viewed image either horizontally or vertically to reveal portions of the image located near the edges or in the overscan areas. At power-up, the default position is the midpoint of the adjustment range.

Each POS_D HIGH pulse moves the TV window down eight lines. At the lowest position (-64 lines) the direction reverses and the pulses move the image up in 8-line increments to the highest position (+64 lines). At this point the direction again reverses and the next sixteen pulses move the image down to the lowest position.

Each POS_R HIGH pulse moves the TV window eight pixels to the right. At the maximum right position (+64 pixels) the direction reverses and the next sixteen pulses move the window left to the maximum left position (-64 pixels). Direction again reverses and the next sixteen pulse move the image right.

Without a RESET, $POS_{D,R}$ controls will loop, causing the window to move down/up, right/left.

Blank and Blue

TV video can set to active (converted VGA source), blank or blue by the BLANK and BLUE inputs.

Table 7. Video Output for BLANK and BLUE inputs

BLANK	BLUE	Video
L	X	Video
H	L	Black
H	H	Blue

Power Management

D/A Power Control

Table 8 shows how the Composite and S-video ouputs are enabled by the CVIDEN and SVIDEN controls. If DPMS = LOW, the display will be blue if either or both VGAHS or VGAVS are inactive.

Table 8. Video Output Control

CVIDEN	SVIDEN	VGAHS & VGAVS	Compos-ite Video	S-Video
H	X	YES	Active	X
X	H	YES	X	Active
L	L	X	Blank	Blank
H	H	NO	Blue	Blue

Powerdown Mode

$\overline{\text{PWRDN}}$ eliminates current drain by the D/A converter, V_{TOUT} voltage follower and clock outputs. With $\overline{\text{PWRDN}}$ = HIGH, all outputs are enabled. If $\overline{\text{PWRDN}}$ = LOW, all outputs are disabled including the ADCLK, PXCK, V_{TOUT} and the D/A converters.

Software Control

Display Power Management Signaling (DPMS)

Display Power Management is compliant with VESA DPMS Proposal 1.0. With DPMS = HIGH, the operational state of the TMC2360 is controlled by the pulse activity on VGAHS and VGAVS.

Table 9 shows how the TMC2360 responds. "No Pulses" on VSYNC or HSYNC is declared on the second missing VSYNC or HSYNC pulse. Following an OFF state, detection of VGAHS and/or VGAVS restores either the Suspend, Standby, or On state.

Regardless of the state of DPMS, absence of VGAHS and/or VGAVS pulses will cause the TMC2360 processor to sleep. However, with DPMS = HIGH, in the Off state. the A/Ds, D/As, and clocks are also set to sleep.

Vertical Sync Communications (VSCOM)

VSCOM is a unique feature incorporated into the TMC2360. With VSCOM = HIGH, the TMC2360 interprets commands that are encoded within the VGA vertical sync period. TV Standard and Flicker Filter may be selected by commands from the PC sourcing the VGA signal.

During the vertical sync period, the number of horizontal sync pulses is counted. Table 10 shows how the selected Television Standard changes with the code set into the $TVSTD_{1\text{-}0}$ inputs and the number of horizontal syncs per vertical sync interval.

Table 11 shows how the Filter Mode is selected with VSCOM. Notice that if one standard, such as PAL800 is selected, then counts of 10, 11 and 12 enable selection of three filter modes.

Table 9. Display Power Management Signaling (DPMS) States

State	VGAHS	VGAVS	TMC2360 State
On	Pulses	Pulses	On, video active
Stand-by	No Pulses	Pulses	Stand-by, screen blanked (color set by BLUE)
Suspend	Pulses	No Pulses	Stand-by, screen blanked (color set by BLUE)
Off	No Pulses	No Pulses	Off, screen black (equivalent to $\overline{\text{PWRDN}}$, except A/D Clock and 27MHZ oscillator are active.)

Table 10. TVSTD Control When Under Software Control (VSCOM = 1)

$TVSTD_{1-0}$	Hsyncs per Vsync Interval	Television Standard	VGA Frame Rate
XX	10,11,12	PAL 800 (B, G, I)	50 Hz
X0	6,7,9	PAL 640 (B, G, I)	50 Hz
01	6,7,9	PAL-M	60 Hz
11	6,7,9	(reserved)	
0X	1-5,8,14,15	NTSC	60 Hz
10	1-5,8,14,15	NTSC-EIAJ	60 Hz
11	1-5,8,14,15	(reserved)	
XX	0,13	Blank (with prior standard)	50/60 Hz

Table 11. VSCOM Filter Command Interpretation (VSCOM=1)

HSYNCs per VSYNC Interval	Filter Mode
5, 9, 12	No Filter
4, 7, 11	2-line filter
1, 2, 3, 6, 8, 10, 14, 15	3-line filter
0, 13	Blank (with prior mode)

Microprocessor Interface

Table 12 shows the five registers that may be read after the Address Register has been loaded. Only the two VGA registers and the Address Register may be written. For microprocessor control, 40h must be written into VGA register 1. To disable control through VGA Register 0, 00h must be written into register 1. Bit assignments of VGA register 0 are listed in Table 13. Bit assignments of VGA register 1 are listed in Table 14.

For communications through the microprocessor port, set MPEN = HIGH. Read and write timing is shown in Figure 4 and Figure 5. To access a VGA register, write the address of the selected register into the lower four bits of the eight bit Address Register with A_0 = LOW. Then with A_0 = HIGH, read or write to the selected register.

Table 12. Microprocessor Addressable Registers

A1	A0	Address Register Value	Register
0	0	x	Address Register
0	1	x0	VGA Register 0
0	1	x1	VGA Register 1
0	1	x6	Revision ID (xxh)
0	1	x7	Part ID (0Fh)

Table 13. VGA Control Register 0 Bit Map

Bit #	Name	Function
7	—	0 (reserved)
6-5	FIL	0 0 No Filter
		0 1 2-line Filter
		1 x 3-line Filter
4-2	TVSTD	0 0 0 NTSC
		0 0 1 NTSC-EIA
		0 1 0 PALM
		0 1 1 PAL640
		1 x x PAL800
1-0	VIDEO	0 0 Black
		0 1 Ramp
		1 0 Color Bars
		1 1 Normal

Table 14. VGA Control Register 1 Bit Map

Bit #	Name	Function
7	—	0 (reserved)
6	MODE	0 Normal
		1 Bypass FIL and TVSTD Pins
5-3	—	0 (reserved)
2	DIVMN	0 (reserved)
		1 Enable ADIVN and PVIDM
1	EXTPLL	0 Disable external PXCK PLL
		1 Enable external PXCK PLL
0	EXTPLLA	0 Disable external ACLK PLL
		1 Enable external ACLK PLL

Video Formats

Incoming VGA Formats

Table 15 and Table 16 show expected VGA Video input formats.

Outgoing TV Formats

Table 17 shows the four different TV formats that may be selected as outputs by the TVSTD1-0 inputs.

Table 18 and Table 19 show the Horizontal and Vertical Timing for the NTSC and PAL formats.

Table 15. VGA Horizontal Timing Parameters

Television Standard	TVSTD1-0	PAL800	Line Rate (kHz)	Front Porch (pixels)	Horiz Sync (pixels)	Back Porch (pixels)	Active Video (pixels)
NTSC(-EIA)	0x	0	31.469	18	96	46	640
PAL/B, G, I	10	0	31.250	18	96	54	640
PAL/B, G, I	10	1	31.250	98	96	158	800
PAL/M	11	0	31.500	18	96	46	640

Table 16. VGA Vertical Timing Parameters

Television Standard	TVSTD1-0	PAL800	Frame Rate (Hz)	Line Rate (kHz)	Full Frame (lines)	Front Porch (lines)	Vert. Sync (lines)	Vsync + Back Porch (lines)	Active Video (lines)
NTSC(-EIA)	0x	x	59.94	31.469	525	13	2-16	32	480
PAL/B, G, I	10	0	50	31.250	625	61	2-16	84	480
PAL/B, G, I	10	1	50	31.250	625	1	2-16	24	600
PAL/M	11	x	60	31.469	525	13	2-16	32	480

Table 17. TVSTD Control When Under Manual Control (VSCOM = 0)

TVSTD1-0	Television Standard	Field Rate
00	NTSC	60 Hz
01	NTSC-EIA	60 Hz
10	PAL/B, G, I	50 Hz
11	PAL/M	60 Hz

Table 18. NTSC and PAL Horizontal Timing

Television Standard	Field Rate (Hz)	Lines per frame	Line Rate (kHz)	2x pix Rate (MHz)	fSC Freq. (MHz)	Front Porch pixels	Horiz Sync pixels	Back Porch pixels	Active Video pixels	Line H pixels
NTSC	59.94	525	15.734	24.546	3.579	18	58	58	646	780
PAL	50.00	625	15.625	29.500	4.433	18	70	82	774	944
PALM	60	525	15.734	25.570	3.576	18	58	58	646	780

Table 19. NTSC and PAL Vertical Timing

TV Std	Field Rate (Hz)	Lines per frame	Line Rate (kHz)	Front Porch (lines)	Vertical Sync (lines)	Back Porch (lines)	Active Video (lines)
NTSC	59.94	525	15.734	3-3.5	3	14-14.5	242.5
PAL	50.00	625	15.625	2.5	2.5	21	286.5
PALM	60.00	525	15.750	3	3	14	242.5

Timing Diagrams

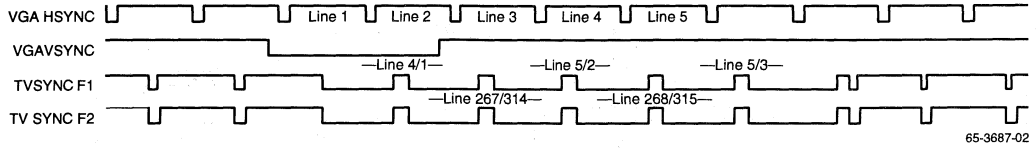


Figure 4. Nominal VGA-NTSC/PAL Vertical Sync Timing

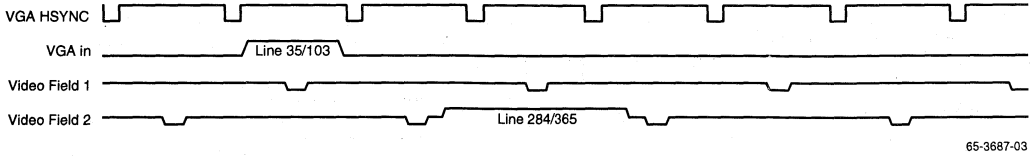


Figure 5. Nominal VGA640-NTSC/PAL, No Filter Timing

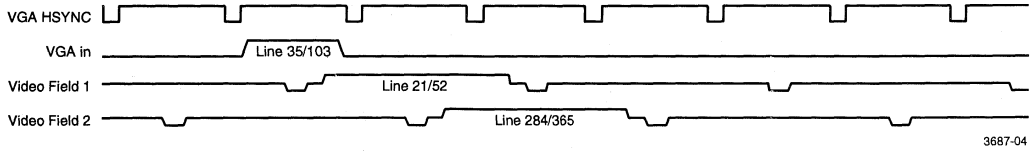


Figure 6. Nominal VGA-NTSC/PAL, Medium Filter Timing

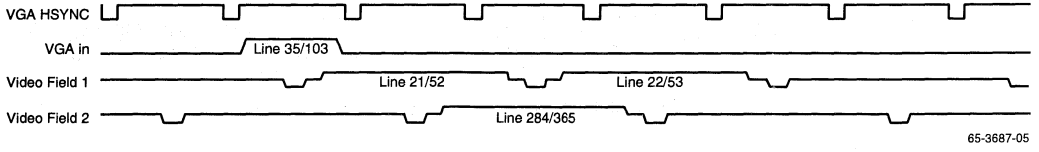


Figure 7. Nominal VGA-NTSC/PAL, High Filter Timing

Timing Diagrams (continued)

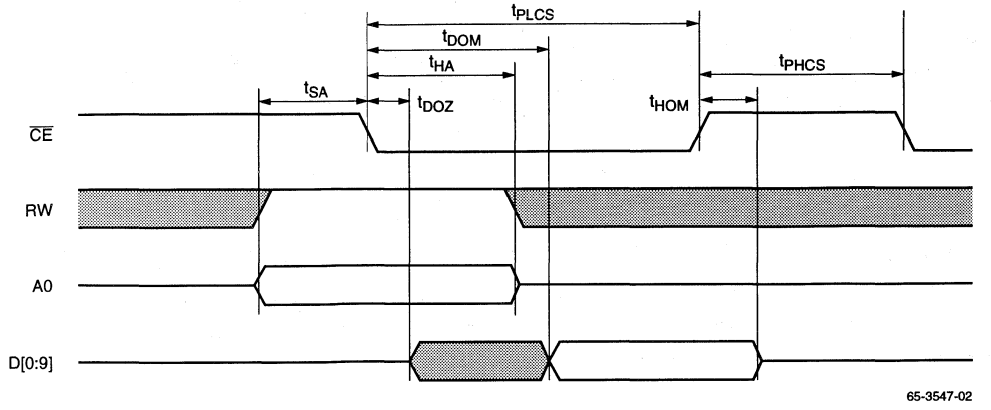


Figure 8. Microprocessor Read Timing

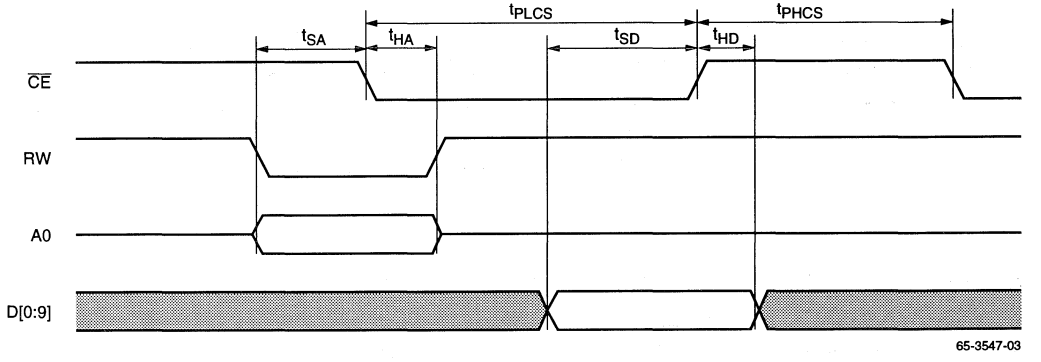


Figure 9. Microprocessor Write Timing

Preliminary Information

Equivalent Circuits

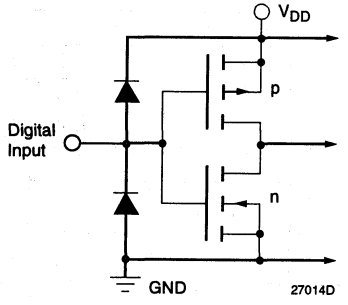


Figure 10. Equivalent Digital Input Circuit

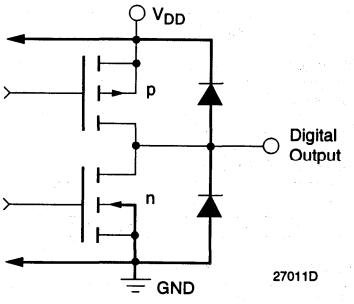


Figure 11. Equivalent Digital Output Circuit

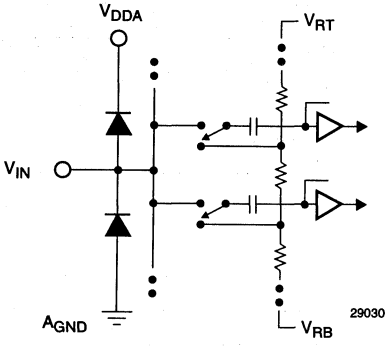


Figure 12. Equivalent A/D Input Circuit

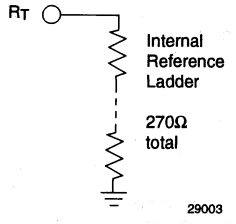


Figure 13. Equivalent A/D Reference Input Circuit

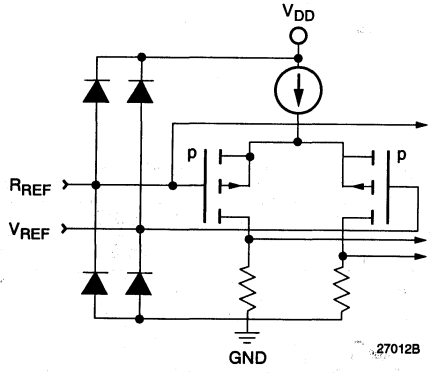


Figure 14. Equivalent D/A Reference Input Circuit

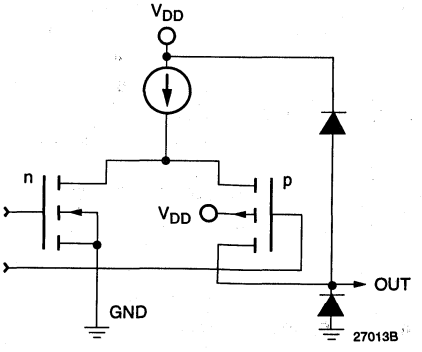


Figure 15. Equivalent D/A Output Circuit

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltages				
V_{DDA} (Measured to AGND)	-0.5		7.0	V
V_{DD} (Measured to DGND)	-0.5		7.0	V
V_{DDA} (Measured to VDD)	-0.5		0.5	V
AGND (Measured to DGND)	-0.5		0.5	V
Digital Inputs				
Applied Voltage (Measured to DGND)[2]	-0.5		V_{DD} + 0.5	V
Forced current [3, 4]	-10.0		10.0	mA
Analog Inputs				
Applied Voltage (Measured to AGND)[2]	-0.5		V_{DDA} + 0.5	V
Forced current [3, 4]	-10.0		10.0	mA
Digital Outputs				
Applied Voltage (Measured to DGND)[2]	-0.5		V_{DD} + 0.5	V
Forced current [3, 4]	-6.0		6.0	mA
Short circuit duration (single output in HIGH state to ground)			1	second
Temperature				
Operating, Ambient	-20		110	°C
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase soldering (1 minute)			220	°C
Storage	-65		150	°C
Electrostatic Discharge[5]			±150	V

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DD}	Digital Power Supply Voltage	4.75	5.0	5.25	V
V_{DDA}	Analog Power Supply Voltage	4.75	5.0	5.25	V
AGND	Analog Ground (Measured to D_{GND})	-0.1	0	0.1	V
V_{RT}	Reference Voltage, Top	0.5	0.75	2.0	V
V_{IN}	Analog Input Range	0		V_{RT}	V
V_{REF}	External Reference Voltage		1.235		V
I_{REF}	D/A Converter Reference Current (I_{REF} = V_{REF}/R_{REF}, flowing out of the R_{REF} pin)		3.15		mA
R_{REF}	Reference Resistor, V_{REF} = Nom		392		Ω
R_{OUT}	DAC Total Output Load Resistance		37.5		Ω

Operating Conditions (continued)

Parameter		Min	Nom	Max	Units
V_{IH}	Input Voltage, Logic HIGH	2.0			V
V_{IL}	Input Voltage, Logic LOW			0.8	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply Currents						
I_{DD}	Operating	CVIDEN = L, SVIDEN = H		250		mA
I_{DDS}	Standby	CVIDEN = L, SVIDEN = H		220		mA
I_{DDQ}	Power-Down	$\overline{PWRDN}$ = L		5		mA
I_{SDAC}	S-Video DACs	37.5 ohm load, I_{REF} = 3.15 mA		140		mA
I_{CDAC}	Composite Video DAC	37.5 ohm load, I_{REF} = 3.15 mA		70		mA
Digital Inputs and Outputs						
C_I	Input Capacitance			5	10	pF
C_O	Output Capacitance			10		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
V_{T+}	Schmitt Trigger Positive Threshold			3.0		V
V_{T-}	Schmitt Trigger Negative Threshold			0.8		V
V_{OH}	Output Voltage, HIGH	I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max			0.4	V
Analog Intputs						
C_{AI}	A/D Input Capacitance	ADCLK = LOW ADCLK = HIGH		4 12		pF pF
R_{IN}	A/D Input Resistance		500	1000		KΩ
I_{CB}	A/D Input Current				±1	µA
V_{RO}	Voltage Reference Output		0.988	1.235	1.482	V
Z_{RO}	V_{REF} Output Impedance			3		KΩ
Analog Outputs						
V_{OC}	Video Output Compliance		-0.4		2	V
R_{OUT}	Video Output Resistance			15		KΩ
C_{OUT}	Video Output Capacitance	C_{OUT} = 0 mA, Freq. = 1 MHz		15		pF
I_{OS}	Short-Circuit Current		-20		-80	mA

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
Clocks						
f_{XTAL}	Crystal/Reference Clock Frequency			27		MHz
f_{XTOL}	Crystal/Reference Clock Frequency Tolerance				±1350	Hz
t_{PWH}	Reference Clock Pulse Width, HIGH					ns
t_{PWL}	Reference Clock Pulse Width, LOW					ns
Syncs						
f_H	VGAHS Frequency	60 Hz Modes	30.840	31.469	32.100	KHz
		50Hz Modes	30.630	31.250	31.880	KHz
N_H	Lines per VGA frame	60 Hz Modes		525		
		50Hz Modes		625		
		Tolerance			±0	
t_{PWHS}	VGAHS Pulsewidth		2			µs
t_{VS-HS}	VGAVS to VGAHS Delay		0			ns
t_{DS}	Sync Delay (VGA Sync to Sync Out)					ns
Video Output						
t_{DOV}	Analog Output Delay (PXCK Out to Video Out)					ns
t_R	D/A Output Current Risetime (10% to 90%)			2		ns
t_F	D/A Output Current Falltime (90% to 10%)			2		ns
SKEW	D/A to D/A Skew				1	ns
Controls						
t_{PWH}	Control Input Pulse Width, HIGH			5		µs
t_{PWL}	Control Input Pulse Width, LOW			5		µs
Microprocessor Interface						
t_{PLCS}	$\overline{CS}$ Pulse Width, LOW		50			ns
t_{PHCS}	$\overline{CS}$ Pulse Width, HIGH		25			ns
t_{SA}	Address Setup Time		0			ns
t_{HA}	Address Hold Time		10			ns
t_{SD}	Data Setup Time		15			ns
t_{HD}	Data Hold Time		0			ns
t_{DOZ}	Output Delay, $\overline{CS}$ to low-Z		5			ns
t_{HOM}	Output Hold Time, $\overline{CS}$ to high-Z		5			ns
t_{DOM}	Output Delay, $\overline{CS}$ to Data Valid				30	ns

Preliminary Information

System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
A/D Converter Input						
E_{LI}	A/D Integral Linearity Error, Independent	V_{RT} = 2.0V		±0.3	±0.5	LSB
E_{LD}	A/D Differential Linearity Error	V_{RT} = 2.0V		±0.3	±0.5	LSB
E_{AP}	Aperture Error			30		ps
E_{OT}	Offset Voltage, Top	R_T – V_{IN} for most positive code transition	-5	-15	-25	mV
E_{OB}	Offset Voltage, Bottom	V_{IN} for most negative code transition	25	35	45	mV
D/A Converter Output						
RES	D/A Converter Resolution		9	9	9	Bits
dp	Differential Phase	PXCK = 27 MHz, 40 IRE Ramp			1.0	degree
dg	Differential Gain	PXCK = 27 MHz, 40 IRE Ramp			1.5	%
CNLP	Chroma Nonlinear Phase	NTC-7 Combination			±1.25	degree
CNLG	Chroma Nonlinear Gain	NTC-7 Combination			±1.0	%
CLIM	Chroma/Luma Intermodulation	NTC-7 Combination				IRE
CLGI	Chroma/Luma Gain inequality	NTC-7 Composite				%
CLDI	Chroma/Luma Delay inequality	NTC-7 Composite				ns
LNLD	Luma Nonlinear Distortion	NTC-7				IRE
FTWD	Field Time Waveform Distortion	NTC-7				IRE
LTWD	Line Time Waveform Distortion	NTC-7				IRE
LOTWD	Long Time Waveform Distortion, initial and peak overshoot	10% / 90% APL Bounce				IRE
LOTWD	Long Time Waveform Distortion, peak overshoot	after 5 seconds, 10% / 90% APL Bounce				IRE
LDCOFF	Line-by-Line DC Offset					IRE
DYNG	Dynamic Gain	NTC-7				IRE
NOISE	Noise Level[2]	100% unmod. ramp				dB rms
NOISE	Noise Level[3]	100% unmod. ramp				dB rms
CAMN	Chroma AM Noise	Red field				dB rms
CPMN	Chroma PM Noise	Red field				dB rms
SYRF	Sync Pulse Rise and Fall Time					ns
BERF	Burst envelope Rise and Fall Time					ns
PSRR	Power Supply Rejection Ratio	C_{BYP} = 0.1 µF, f = 1 KHz		0.5		%/ %V_{DD}

Notes:

1. Values shown in Typ column are typical for V_{DD} = V_{DDA} = +5V and T_A = 25°C.
2. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, with Tilt Null ON measured using VM700 "Measure Mode."
3. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, measured using VM700 "Auto Mode".

Application Notes

Grounding

Analog and digital circuits are separated within the TMC2360. To keep digital system noise from the A/D and D/A converters, it is recommended that power supply voltages (V_{DD} and V_{DDA}) originate from the same low-noise source, and that ground connections (DGND and AGND) be made to the analog ground plane. Power supply connections should be individually decoupled at each pin. Digital circuitry deriving input from the TMC2360 should be referred to the system digital ground plane.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions for layout:

1. Keep the critical analog traces as short as possible and as far as possible from all digital signals. Locate the TMC2360 near the board edge, close to the analog input/output connectors.

2. The power plane for the TMC2360 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC2360 is the same as that of the system's digital circuitry, power to the TMC2360 should be decoupled with ferrite beads and 0.1µF capacitors to reduce noise.

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They supply different circuits on the integrated circuit, each of which generate varying amounts and types of noise. For best results, use 0.1µF ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not be placed under the TMC2360, the voltage reference, or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC2360 and its related analog circuitry can have an adverse effect on performance.

The 27 MHz clock reference or crystal should be handled carefully. Jitter and noise on this clock will degrade performance. With an external clock, the line should be terminated to eliminate overshoot and ringing.

Locate phase locked loop components close to the relevant TMC2360 pins. Isolate these components from noise.

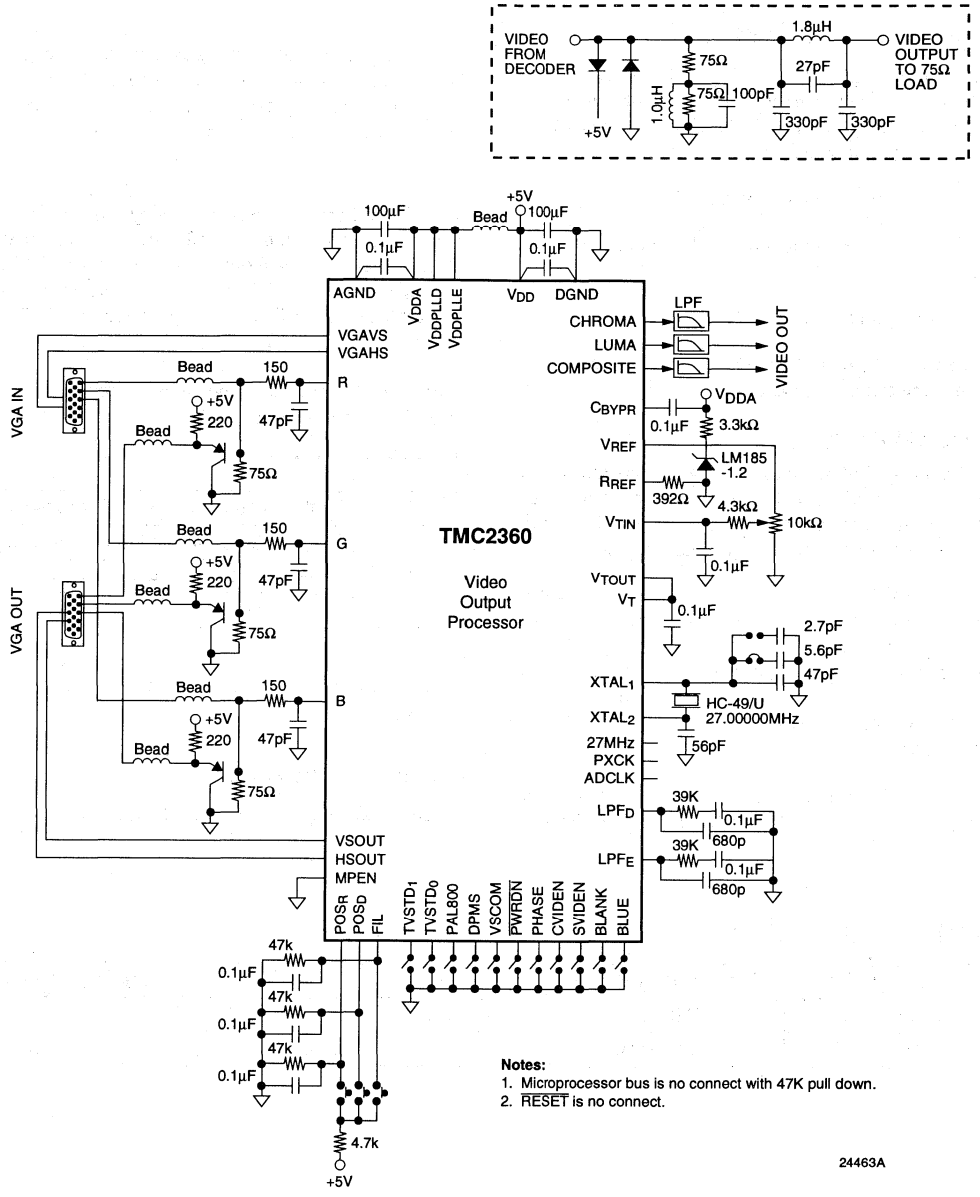


Figure 12. Typical application circuit with internal phase-locked loops

Suggested User Instructions

For a product incorporating the TMC2360, part of the documentation is expected to include operating instructions describing the functions of the TMC2360 user controls. A recommended text fragment follows:

Three external controls may be used to:

1) position the image within the boundaries of the TV screen.

2) control vertical resolution.

Each control is a button that can be momentarily depressed to execute one cycle of the selected function.

Position Controls

Position controls shift the viewed image horizontally or vertically to reveal portions of the image that are located near the edges or in the overscan areas. At power-up, the default position is the midpoint of the adjustment range.

Each time the VERTICAL POSITION button is depressed, the TV window moves down by eight lines. At the lowest position (-64 lines) the direction reverses and depressing the button moves the image up in 8-line increments to the highest position (+64 lines). At this point the direction again reverses and the next sixteen pulses move the image down to the lowest position.

When the HORIZONTAL POSITION button is depressed, the TV window moves eight pixels to the right. At the maximum right position (+64 pixels) the direction reverses and the next sixteen pulses move the window left to the maximum left position (-64 pixels). Direction again reverses and the next sixteen pulses move the image right.

Flicker Filter

Annoying artifacts can be eliminated by selecting one of three filter modes which trade-off vertical resolution against flicker. For example, without the filter, a single VGA line is encoded into only one field of the TV display. If there is high contrast between this line and adjacent lines, it will flicker at 30 Hz in NTSC or 25 Hz in PAL.

Depressing the FILTER button indexes through the filter functions shown in the table below:

FIL	Filter Mode
↓ ▲	Soft vertical resolution without flicker
↓	Medium vertical resolution, some flicker
↓	Sharp vertical resolution with flicker
└─┘	Color bars

The filter should be selected for best appearance on the TV screen. Optimal selection will depend on the image being encoded.

Related Products

- TMC2302 Image Manipulation Sequencer

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2360KLC	0°C to 70°C	Commercial	80 Lead MQFP	2360KLC
TMC2360R0C	0°C to 70°C	Commercial	84 Lead PLCC	2360R0C

Section 5 – Set Top Box

TMC22290

Multistandard Digital Video Encoder

Features

- All-digital video encoding
- Internal digital subcarrier synthesizer
- 8-bit parallel CCIR-601/CCIR-656/ANSI/SMPTE 125M input iormat
- CCIR-624/SMPTE-170M compliant output
- Switchable chrominance bandwidth
- Switchable pedestal with gain compensation
- Pre-programmed horizontal and vertical timing
- 13.5 Mpps pixel rate
- Synchronizes to incoming data stream
- Subcarrier phase and frequency values may be input through ancillary data packet in video stream
- Internal interpolation filters simplify output reconstruction filters
- 9-bit D/A converters for video reconstruction
- Supports NTSC and PAL standards
- Output encoding per Macrovision copy protection (Revision 6) available (TMC22291)
- Simultaneous S-Video (Y/C) output
- Controlled edge rates
- TAG (IEEE Std 1149.1-1990) test interface
- Single +5V power supply
- 44 lead PLCC package
- Parallel and serial control interface

Applications

- Settop Digital Cable Television Receivers
- Settop Digital Satellite Television Receivers
- Studio Parallel CCIR-601 to Analog Conversion

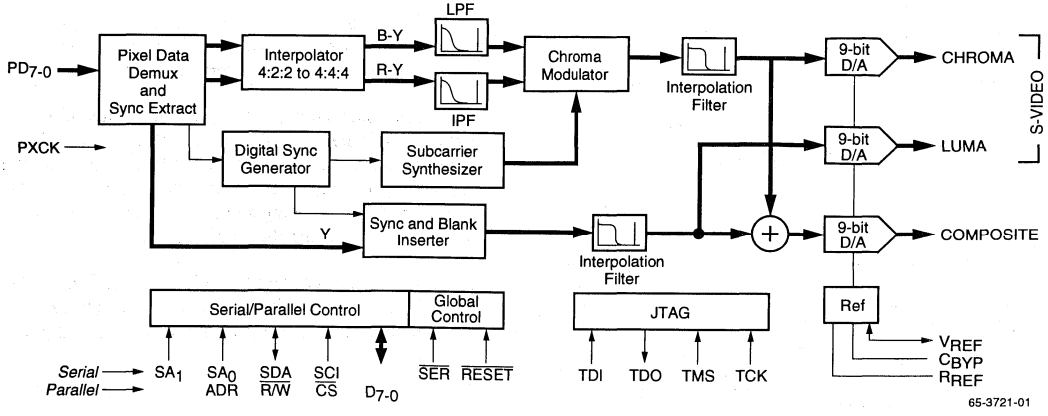
SET TOP BOX

Description

The TMC22290 video encoder converts digital component video (in 8-bit parallel CCIR-601/656 or ANSI/SMPTE 125M format) into a standard analog baseband television (NTSC, NTSC-EIA, all PAL standards) signal with a modulated color subcarrier. Both composite (single lead) and S-Video (separate chroma and luma) formats are active simultaneously at the three analog outputs. Each video output generates a standard video-level signal capable of driving a singly- or doubly-terminated 75 Ohm load.

The TMC22290 is fabricated in a submicron CMOS process and is packaged in a 44-lead PLCC. Performance is guaranteed over the full 0°C to 70°C operating temperature range.

Block Diagram



General Description

The TMC22290 is a fully-integrated digital video encoder with simultaneous composite and Y/C (S-Video) outputs. The TMC22290 video outputs are compatible with NTSC, NTSC-EIA, and all PAL television standards. No external component selection or tuning is required.

To prevent unauthorized video taping, the output data stream may be modified per the Macrovision copy protection system (Revision 6). This feature is available on the TMC22291 only to Macrovision licensees. Consult the factory for information.

The encoder accepts digital component video at the PD port in 8-bit parallel CCIR-601/656 format. It is demultiplexed into luminance and chrominance components. The chrominance components modulate a digitally synthesized subcarrier. The luminance and chrominance signals are separately interpolated to twice the input pixel rate and converted to analog levels by 9-bit D/A converters. They are also digitally combined and the resulting composite signal is output by a third 9-bit D/A converter.

The encoder operates from a single clock of 27 MHz, twice the system pixel rate. Programmable control registers allow the software control of subcarrier frequency and phase parameters. Incoming YC_BC_R422 digital video is interpolated to YC_BC_R444 format for encoding.

Internal control registers can be accessed over a standard 8-bit parallel microprocessor port or a 2-pin (clock and data) serial port.

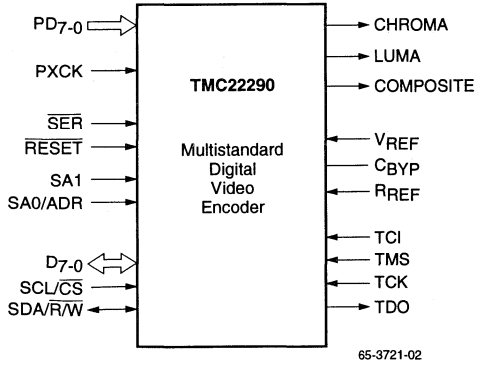


Figure 1. Logic Symbol

MSB						LSB
PD7			C_B (n)			PD0
PD7			Y (n)			PD0
PD7			C_R (n)			PD0
PD7			Y (n+1)			PD0

Samples C_B(n), Y(n), and C_R(n) are cosited.

Figure 2. Pixel Data Format

Sync Generator

The TMC22290 operates in a slave mode, extracting its horizontal and vertical sync timing and field information from the CCIR-656 EAV (End of Active Video) signal in the incoming data stream.

Horizontal and vertical synchronization pulses in the analog output are digitally generated by the TMC22290 with controlled rise and fall times on all sync edges, the beginning and end of active video, and the burst envelope.

Chroma Modulator

A digital subcarrier synthesizer drives a quadrature modulator, producing a digital chrominance signal. The chroma bandwidth may be programmed to 650kHz or 1.3 MHz. The relative phases of the burst and active video portions of the subcarrier can be adjusted with respect to the falling edge of horizontal sync. This sets the SCH phasing of the TMC22290. SCH phase adjustment can be accomplished through the parallel or serial ports as well as the ancillary data prior to each line of incoming video.

Interpolation Filters

Interpolation filters on the luminance and chrominance signals double the pixel rate in preparation for D/A conversion. This low-pass filtering and oversampling process greatly simplifies the output filter required after the D/A converters and dramatically reduces sin(x)/x distortion.

D/A Converters

The analog outputs of the TMC22290 are driven by three 9-bit D/A converters, operating at 27 MHz. The outputs drive standard video levels into 37 or 75 Ohm loads. An internal voltage reference is used to provide reference current for the D/A converters. For more accurate video levels, an external fixed or variable voltage reference source is accommodated. The video signal levels from the TMC22290 may be adjusted to overcome the insertion loss of analog low-pass output filters by varying R_{REF} or V_{REF}.

Parallel and Serial Microprocessor Interfaces

The parallel microprocessor interface employs 14 pins. These are shared with the serial interface, and a single pin, $\overline{SER}$, selects between the two interface modes.

In parallel interface mode, one address line is decoded for access to the internal control register and its pointer. Controls are reached by loading a desired address through the 8-bit D_{7-0} port, followed by the desired data (read or write) for that address. The control register address pointer auto-increments to address 20h and then remains there.

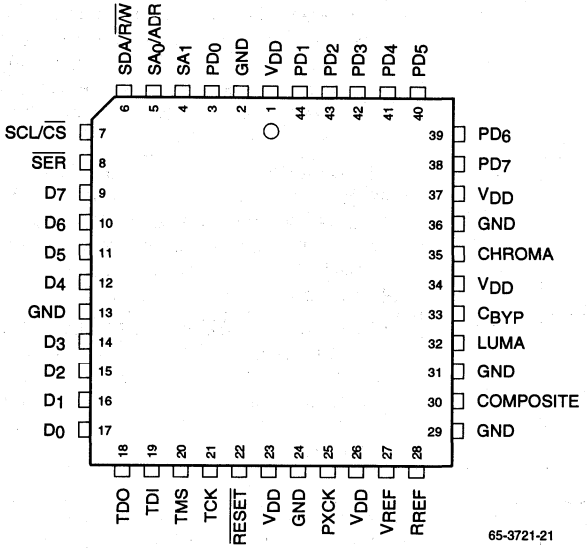
A 2-line serial interface is also provided on the TMC22290 for initialization and control. The same set of registers accessed by the parallel port is available to the serial port.

The $\overline{\text{RESET}}$ pin sets all internal state machines to their initialized conditions, disables the analog outputs, and places the encoder in a power-down mode. All register data are maintained while in power-down mode. At power-up. the encoder is automatically initialized in NTSC-M format.

JTAG Test Interface

The TMC22290 includes a standard 4-line JTAG (IEEE Std 1149.1-1990) test interface port, providing access to all digital input/output data pins. This is provided to facilitate component and board-level testing.

Pin Assignments



Pin Descriptions

Name	Pin Number	Value	Pin Function Description
Clock			
PXCK	25	TTL	**Pixel Clock Input.** This 27.0 MHz clock is internally divided by 2 to generate the internal pixel clock. PXCK drives the entire TMC22290, except the asynchronous microprocessor interface. All internal registers are strobed on the rising edge of PXCK.
Data Input			
PD_{7-0}	38-44, 3	TTL	**Pixel Data Inputs.** Video data enter the TMC22290 on PD_{7-0} (Figure 2).
µProc I/O			
$\overline{\text{RESET}}$	22	TTL	**Master Reset Input.** Bringing $\overline{\text{RESET}}$ LOW forces the internal state machines to their starting states, sets all control registers to their default values, and disables all outputs.
D_{7-0}	9-12, 14-17	TTL	**Data I/O Port.** Parallel control port. When $\overline{\text{SER}}$ is HIGH, all control parameters are loaded into and read back over this 8-bit port. When $\overline{\text{SER}}$ = LOW, D_0 serves as a composite sync output, D_1 outputs a burst flag during the back porch, D_{2-5} are General Purpose Outputs, and D_{6-7} are General Purpose Inputs.
SA_1	4	TTL	**Serial Address Select.** When $\overline{\text{SER}}$ is LOW, SA_1 in conjunction with SA_0 selects one-of-four addresses for the TMC22290.

Pin Descriptions (continued)

Name	Pin Number	Value	Pin Function Description
$\overline{SER}$	8	TTL	**Serial/Parallel Port Select.** When LOW, the 2-line serial interface is activated. Pins 5, 6, and 7 function as SA_0, SDA, and SCL respectively. When HIGH, the parallel interface port is active and pins 5, 6, and 7 function as ADR, $\overline{R/W}$, and $\overline{CS}$ respectively.
SA0/ADR	5	TTL	**Serial/Parallel Port Address.** When $\overline{SER}$ is LOW, SA_0 in conjunction with SA_1 selects one-of-four addresses for the TMC22290. When $\overline{SER}$ is HIGH, this control governs whether the parallel microprocessor interface selects a table address or reads/writes table contents. It also governs setting and verification of the TMC22290's internal operating modes, also over port D_{7-0}.
SDA/$\overline{R/W}$	6	R-Bus/TTL	**Serial Data/Read/Write Control.** When $\overline{SER}$ is LOW, SDA is the data line of the serial interface. When $\overline{SER}$ is HIGH, the pin is the read/write control for the parallel interface. When $\overline{R/W}$ and $\overline{CS}$ are LOW, the microprocessor can write to the control registers over D_{7-0}. When $\overline{R/W}$ is HIGH and $\overline{CS}$ is LOW, it can read the contents of any selected control register over D_{7-0}.
SCL/$\overline{CS}$	7	R-Bus/TTL	**Serial Clock/Chip Select.** When $\overline{SER}$ is LOW, SCL is the clock line of the serial interface. When $\overline{SER}$ is HIGH, the pin is the chip select control for the parallel interface. When $\overline{CS}$ is HIGH, the microprocessor interface port, D_{7-0}, is set to HIGH impedance and ignored. When $\overline{CS}$ is LOW, the microprocessor can read or write parameters over D_{7-0}.
Analog Outputs			
COMPOSITE	30	1.35 V P-P	**Composite NTSC/PAL Video.** Analog output of composite D/A converter, nominally 1.35 volt peak-to-peak into a doubly terminated 75 Ohm load.
LUMA	32	1.35 V P-P	**Luminance-only Video.** Analog output of luminance D/A converter, nominally 1.35 volt peak-to-peak into a doubly terminated 75 Ohm load.
CHROMA	35	1.35 V P-P	**Chrominance-only Video.** Analog output of chrominance D/A converter, nominally 1.35 volt peak-to-peak into a doubly terminated 75 Ohm load.
Reference			
V_{REF}	27	+1.23 V	**Voltage Reference Input.** External voltage reference input, internal voltage reference output, nominally 1.235 V.
C_{BYP}	33	0.1 µF	**Reference Bypass Capacitor.** Connection point for 0.1 mF decoupling capacitor.
R_{REF}	28	787W	**Current-setting Resistor.** Connection point for external current-setting resistor for D/A converters. The resistor is connected between R_{REF} and GND. Output video levels are inversely proportional to the value of R_{REF}.
JTAG I/O			
TDI	19	TTL	**Data Input Port.** Boundary scan data input port.
TMS	20	TTL	**Scan Select Input.** Boundary scan (HIGH) / normal operation (LOW) selector.
TCK	21	TTL	**Scan Clock Input.** Boundary scan clock.
TDO	18	TTL	**Data Output Port.** Boundary scan data output port.

Pin Descriptions (continued)

Name	Pin Number	Value	Pin Function Description
Power			
V_{DD}	1, 23, 26, 34, 37	+5 V	**Power Supply.** Positive power supply circuits.
GND	2, 13, 24, 29, 31, 36	0.0 V	**Ground.** Ground for analog circuits, 0 V.

Control Registers

The TMC22290 is initialized and controlled by a set of registers which determine the operating modes.

An external controller is employed to write and read the Control Registers through either the 8-bit parallel or 2-line serial interface port. The parallel port, D_{7-0}, is governed by pins $\overline{CS}$, $\overline{R/W}$, and ADR. The serial port is controlled by SDA and SCL.

Table 2. Control Register Map

Reg	Bit	Name	Function
TMC22290 Identification Registers			
00	7-0	PARTID2	(Read only = $7F_h$)
01	7-0	PARTID1	(Read only = $3A_h$)
02	7-0	PARTID0	(Read only = 95_h)
03	7-0	REVID	(Read only = Revision #)
Global Control Register			
04	7-6	reserved	
04	5	YCDELAY	Luma to chroma delay
04	4	RAMPEN	Modulated ramp enable
04	3	YCDIS	LUMA, CHROMA disable
04	2	COMPDIS	COMPOSITE disable
04	1-0	FORMAT	Television standard select
Video Output Control Register			
05	7	reserved	
05	6	$\overline{BURSTF}$	Burst flag disable
05	5	CHRBW	Chroma bandwidth select
05	4	SYNCDIS	Sync pulse disable
05	3	BURDIS	Color burst disable
05	2	LUMDIS	Luminance disable
05	1	CHRDIS	Chrominance disable
05	0	PEDEN	Pedestal enable
Horizontal Ancillary Data Control Register			
06	7-6	reserved	
06	5-3	FIELD	Field ID (Read only)
06	2	ANCFREN	Ancillary FREQ enable
06	1	ANCPHEN	Ancillary SCHPH enable
06	0	ANCTREN	Ancillary timing ref. enable
Ancillary Data ID Register			
07	7-0	ANCID	Ancillary identification
Subcarrier Frequency Register			
08	7-0	FREQ3	Subcarrier frequency MSB
09	7-0	FREQ2	Subcarrier freq. 2nd byte
0A	7-0	FREQ1	Subcarrier freq. 3rd byte
0B	7-0	FREQ0	Subcarrier frequency LSB
Subcarrier Phase Offset Register			
0C	7-0	SCHPHM	Subcarrier phase MSBs
0D	7-0	SCHPHL	Subcarrier phase LSBs
General Purpose Port (when $\overline{SER}$=LOW)			
0E	7	PORT7-6	General Purpose Inputs
0E	6	PORT5-2	General Purpose Outputs
0E	1	BURSTF	Burst Flag Output
0E	0	CSYNC	Composite Sync Output
Reserved Registers			
0F-FF	7-0	reserved	

Notes:

1. Functions are listed in the order of reading and writing.
2. For each register listed above, all bits not specified are reserved and should be set to zero to ensure proper operation.

Table 3. Power-Up Default Register Values

Reg	Dflt	Reg	Dflt	Reg	Dflt	Reg	Dflt
00	7F	04	00	08	43	0C	00
01	3A	05	00	09	E0	0D	00
02	95	06	00	0A	F8	0E	xx
03	xx	07	00	0B	3E		

SET TOP BOX

Control Register Definitions

TMC22290 Identification Registers (read only)

Reg	Bit	Name	Description
00	7-0	PARTID2	Reads back $7F_h$
01	7-0	PARTID1	Reads back $3A_h$
02	7-0	PARTID0	Reads back 95_h
03	7-0	REVID	Reads back a value corresponding to the revision letter of the silicon.

Global Control Register (04)

7	6	5	4	3	2	1	0
Reserved		YCDELAY	RAMPEN	YCDIS	COMPDIS	FORMAT	

Reg	Bit	Name	Description
04	7-6		Reserved.
04	5	YCDELAY	When HIGH, the luminance path within the TMC22290 is delayed by one PXCK period. The delay applies only to the LUMA output and may be used to compensate for group delay variation of external filters. When LOW, luminance and chrominance have the same latency. The COMPOSITE output always has equal luminance and chrominance latencies.
04	4	RAMPEN	When HIGH, the TMC22290 outputs a modulated ramp test signal. When LOW, incoming digital video is encoded.
04	3	YCDIS	When HIGH, the LUMA and CHROMA outputs are disabled, reducing power consumption. Set LOW for normal enabled operation.
04	2	COMPDIS	When HIGH, the COMPOSITE output is disabled. Set LOW for normal enabled operation.
04	1-0	FORMAT	Output video format select. Subcarrier frequency, pedestal level, and chrominance bandwidth are independently programmed. 0 0 NTSC 0 1 PAL-B,G,H,I,N 1 0 PAL-M 1 1 Reserved

Control Register Definitions (continued)

VIdeo Output Control Register (05)

7	6	5	4	3	2	1	0
Reserved		$\overline{\text{BURSTF}}$	CHRBW	SYNCDIS	BURDIS	CHRDIS	PEDEN

Reg	Bit	Name	Description
05	7		Reserved.
05	6	$\overline{\text{BURSTF}}$	When $\overline{\text{BURSTF}}$ is LOW, a clamp gate signal is produced on the D1 output and register 0E bit 1
05	5	CHRBW	When LOW, the chrominance bandwidth is ±650 kHz. When HIGH, the chrominance bandwidth is ±1.3 MHz.
05	4	SYNCDIS	When HIGH, horizontal and vertical sync pulses on the COMPOSITE video output are suppressed (blanking level). Color burst, active video, and the COMPSYNC output remain active. Set LOW for normal composite video operation.
05	3	BURDIS	When HIGH, color burst is suppressed (blanking level). Set LOW for normal operation.
05	2	LUMDIS	When HIGH, incoming Y values are forced to the black level. Color burst, CHROMA, and sync are not affected. Set LOW for normal operation.
05	1	CHRDIS	When HIGH, incoming color components CB and CR are suppressed enabling monochrome operation. Output color burst is not affected. Set LOW for normal color operation.
05	0	PEDEN	When LOW, black and blanking are the same level for ALL lines. When HIGH, a 7.5 IRE pedestal is inserted into the output video for NTSC and PAL-M lines 23-262 and 286-525 only. Chrominance and luminance gain factors are adjusted appropriately. PEDEN is valid for NTSC and PAL-M only and should be LOW for all other formats.

Horizontal Ancillary Data Control Register (06)

7	6	5	4	3	2	1	0
Reserved		FIELD			ANCFREN	ANCPHEN	ANCTREN

Reg	Bit	Name	Description
06	7-6		Reserved.
06	5-3	FIELD	Digital field identification. A read-only value of 000 corresponds to field 1 and 111 corresponds to field 8.
06	2	ANCFREN	When HIGH, the TMC22290 gets subcarrier frequency data (FREQ3-0) from incoming ancillary data (in accordance with FRV bit). When LOW, FREQ3-0 registers contain the subcarrier frequency data.
06	1	ANCPHEN	When HIGH, the TMC22290 gets subcarrier phase offset data (SCHPHL and SCHPHM) from incoming ancillary data (in accordance with PHV bit). When LOW, a default value of 0000h is used for subcarrier phase.
06	0	ANCTREN	When HIGH, the TMC22290 decodes incoming ancillary data to determine video timing (FIELD and SVF). When LOW, the ancillary timing reference data is ignored.

Control Register Definitions (continued)

Ancillary Data ID Register (07)

Reg	Bit	Name	Description
07	7-0	ANCID	Bits 7-1 determine the ancillary data identification. Bit 0 is an odd parity bit, but the TMC22090 does not check parity. The value in this register must match that of the incoming ancillary data.

Subcarrier Frequency Registers

Reg	Bit	Name	Description
08	7-0	FREQ3	Eight MSBs (bits 31-24) of the 32-bit subcarrier frequency value.
09	7-0	FREQ2	Bits 23-16 of the 32-bit subcarrier frequency value.
0A	7-0	FREQ1	Bits 15-8 of the 32-bit subcarrier frequency value.
0B	7-0	FREQ0	Eight LSBs (bits 7-0) of the 32-bit subcarrier frequency value.

Subcarrier Phase Offset Registers

Reg	Bit	Name	Description
0C	7-0	SCHPHM	Eight MSBs (bits 15-8) of the 16-bit subcarrier phase offset value. Values other than 00h may be used to adjust the SCH phase of the TMC22290.
0D	7-0	SCHPHL	Eight LSBs (bits 7-0) of the 16-bit subcarrier phase offset value. Values other than 00h may be used to adjust the SCH phase of the TMC22290.

General Purpose Port Register (0E)

7	6	5	4	3	2	1	0
PORT7	PORT6	PORT5	PORT4	PORT3	PORT2	BURSTF	CSYNC

Reg	Bit	Name	Description
0E	7-6	PORT7-6	$D_{7\text{-}6}$ input pins. When in serial control mode, these register read-only bits indicate the state present on data port pins D_7 and D_6.
0E	5-2	PORT5-2	$D_{5\text{-}2}$ output pins. When in serial control mode or when reading register 0E in parallel control mode, these register read/write bits drive data pins D_5-D_2 to the state contained in the respective register bits.
0E	1	BURSTF	D_1 output pin. Produces Burst Flag when in serial control mode, or when reading register 0E.
0E	0	CSYNC	D_0 output pin. Produces Composite Sync when in serial control mode, or when reading register 0E.

Reserved Registers

Reg	Bit	Name	Description
0F-FF	7-0		Reserved. May be left unwritten.

General Purpose Port

The TMC22290 provides a general purpose I/O port for system utility functions. Input, output, and sync functions are implemented. Register 0E is the General Purpose Register.

Full functionality is provided when the encoder is in Serial control mode ($\overline{SER}$ = LOW). Most of the functions are available in parallel interface mode ($\overline{SER}$ = HIGH).

General Purpose Input (serial mode only)

Bits 7 and 6 of Register 0E are general purpose inputs. When the encoder is in serial control mode, data bits D_7 and D_6 are connected to these register locations. When Register 0E is read, the states of bits 7 and 6 reflect the TTL levels present on D_7 and D_6, respectively, at the time of read command execution. Writing to these bits has no effect.

This function is not available when the encoder is in parallel control mode.

General Purpose Output

Register 0E read/write bits 5-2 are connected to pins $D_{5\text{-}2}$, respectively, when the encoder is in serial control mode. The output pins continually reflects the values most recently written into register 0E (1 = HIGH, 0 = LOW). Note that these pins are always driven outputs when the encoder is in serial control mode.

When register 0E is read, these pins report the values previously stored in the corresponding register bits, i.e., it acts as a read/write register. When the encoder is in parallel control mode, this reading produces the output bit values on the corresponding data pins, just as in the serial control mode. However, the values are only present when reading register 0E. The controller can command a continuous read on this register to produce continuous outputs from these pins.

Burst Flag and Composite Sync (output/ read-only)

Register 0E bit 1 is associated with the encoder burst flag. It is a 1 (HIGH) from just before the start of the colorburst to just after the end of the burst. It is a 0 (LOW) at all other times. It is internally delayed to match the internal encoder latency, and is synchronous with the LUMA and COMPOSITE D/A outputs.

Register 0E bit 0 reports the encoder composite sync. It is a 0 (LOW) during horizontal and vertical sync tips. It is a 1 (HIGH) at all other times.

These register bits may be read at any time over either the serial or parallel control port. As they are dynamic, their states will change as appropriate during a parallel port read. In fact, if the parallel control port is commanded to read register 0E continually, the pins associated with these bits behave as burst flag and composite sync timing outputs.

In serial control mode, these same data output pins ($D_{1\text{-}0}$) always act as a burst flag and composite sync TTL outputs, the conditions of the serial control notwithstanding. The states of the flags may be read over the serial port, but due to the low frequency of the serial interface, it may be difficult to get meaningful information.

Horizontal and Vertical Timing

Horizontal and vertical video timing in the TMC22290 is preprogrammed for line-locked systems with a 2x pixel clock of 27.0 MHz.

Table 5 and Table 6 show timing parameters for NTSC and PAL standards as well as the actual expected timing for the TMC22290. Exactly 712 pixels of active video are provided by the user for 525/60 standards, 708 pixels for 625/50 systems. The TMC22290 precisely controls the duration and activity of all other segments of the horizontal line and vertical field group.

The vertical field group comprises several different line types based upon the Horizontal line time.

H = (2 x SL) + (2 x SH) [Vertical sync pulses]

= (2 x EL) + (2 x EH) [Equalization pulses]

SMPTE 170M NTSC and Report 624 PAL video standards call for specific rise and fall times on critical portions of the video waveform. The chip does this automatically, requiring no user intervention. The TMC22290 digitally defines slopes compatible with SMPTE 170M NTSC or CCIR Report 624 PAL on all vital edges:

1. Sync leading and trailing edges.
2. Burst envelope.
3. Active video leading and trailing edges.
4. All vertical interval equalization pulse and sync edges.

Table 5. Horizontal Timing Standards and Actual Values for 60 fps Video Standards (μs)

Parameter		NTSC (SMPTE 170M)			PAL-M (CCIR 624)			TMC22290
		Min	Nom	Max	Min	Nom	Max	
Front porch	FP	1.4	1.5	1.6	1.27		2.22	1.48
Horiz. Sync	SY	4.6	4.7	4.8	4.6	4.7	4.8	4.74
Breezeway	BR	0.508	0.608	0.809	0.9	1.1	1.3	0.59 (NTSC) 1.04 (PAL-M)
Color Burst	BU	2.235	2.514	2.794	2.237	2.517	2.797	2.37
Color Back porch	CBP	0.998	1.378	1.857	0.503		2.363	1.63 (NTSC) 1.19 (PAL-M)
Blanking	BL	10.5	10.7	11.0	10.7	10.9	11.1	10.81
Active Video	VA	52.56	52.86	53.06	52.46	52.66	52.86	52.74
Line Time	H		63.556			63.556		63.56
Equalization HIGH	EH		29.5			29.5		29.41
Equalization LOW	EL		2.3			2.3		2.37
Sync HIGH	SH		4.7			4.7		4.74
Sync LOW	SL		27.1			27.1		27.04
Sync rise and fall times			140±20 ns			<250 ns		150

Table 6. Horizontal Timing Standards and Actual Values for 50 fps Video Standards (μs)

Parameter		PAL-B,G,H,I (CCIR 624)			PAL-N (CCIR 624)			TMC22290
		Min	Nom	Max	Min	Nom	Max	
Front porch	FP	1.2	1.5	1.8	1.2	1.5	1.8	1.41
Horiz. Sync	SY	4.5	4.7	4.9	4.5	4.7	4.9	4.74
Breezeway	BR	0.6	0.9	1.2	0.6	0.9	1.2	0.89
Color Burst	BU	2.030	2.255	2.481	2.233	2.513	2.792	2.37
Color Back porch	CBP		2.654			2.387		2.15
Blanking	BL	11.7	12.0	12.3	11.7	12.0	12.3	11.56
Active Video	VA	51.7	52.0	52.3	51.7	52.0	52.3	52.44
Line Time	H		64			64		64.0
Equalization HIGH	EH		29.65			29.65		29.63
Equalization LOW	EL		2.35			2.35		2.37
Sync HIGH	SH		4.7			4.7		4.74
Sync LOW	SL		27.3			27.3		27.26
Sync rise and fall times			250±50 ns			200±100 ns		240

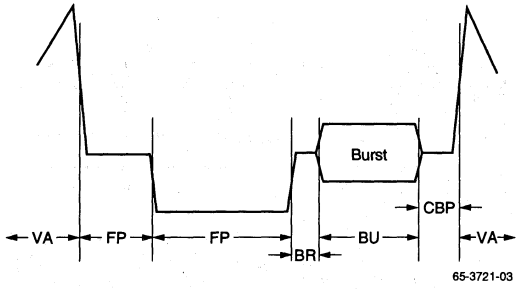


Figure 3. Horizontal Blanking Interval Timing

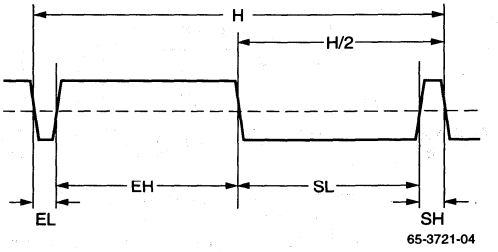


Figure 4. Vertical Sync and Equalization Pulse Detail

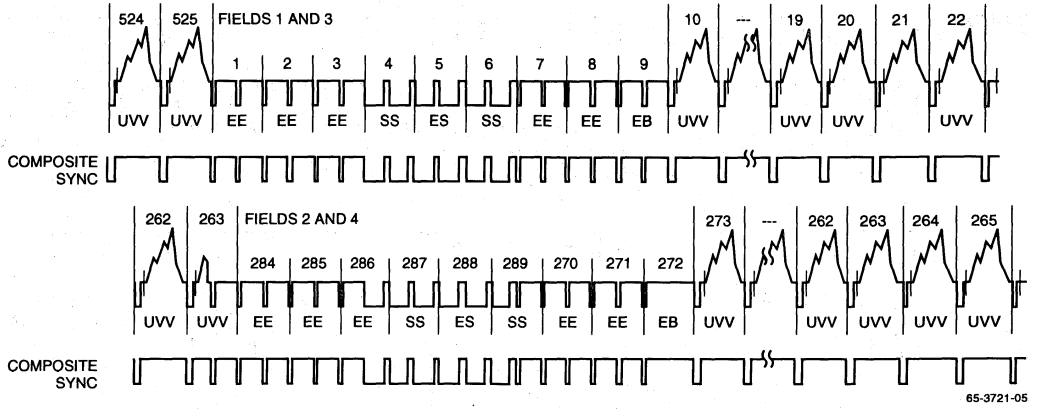


Figure 5. NTSC Vertical Interval

Table 7. NTSC Field/Line Sequence and Identification

Field 1 FID = 00		Field 2 FID = 01		Field 3 FID = 10		Field 4 FID = 11	
Line	ID	Line	ID	Line	ID	Line	ID
1	EE	264	EE	1	EE	264	EE
2	EE	265	EE	2	EE	265	EE
3	EE	266	ES	3	EE	266	ES
4	SS	267	SS	4	SS	267	SS
5	SS	268	SS	5	SS	268	SS
6	SS	269	SE	6	SS	269	SE
7	EE	270	EE	7	EE	270	EE
8	EE	271	EE	8	EE	271	EE
9	EE	272	EB	9	EE	272	EB
10	UVV	273	UVV	10	UVV	273	UVV
•••	•••	•••	•••	•••	•••	•••	•••
262	UVV	524	UVV	262	UVV	524	UVV
263	UVE	525	UVV	263	UVE	525	UVV

EE Equalization pulse
SS Vertical sync pulse
EB Equalization broad pulse
UVE Half-line video, half-line equalization pulse
SE Half-line vertical sync pulse, half-line equalization pulse
ES Half-line equalization pulse, half-line vertical sync pulse
UVV Active video

SET TOP BOX

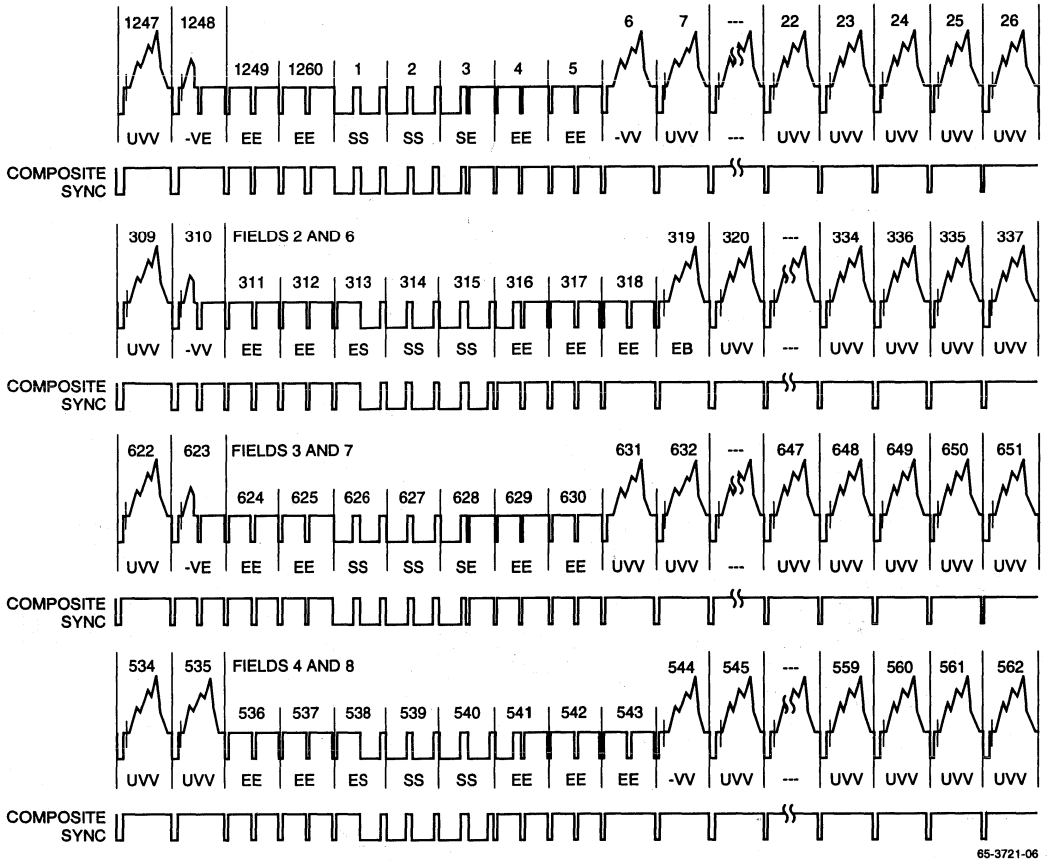


Figure 6. PAL-B, G, H, I, N Vertical Interval

Table 8. PAL-B, G, H, I, N Field/Line Sequence and Identification

Fields 1 and 5 FID = 000, 100		Fields 2 and 6 FID = 001, 101		Fields 4 and 8 FID = 011, 111		Fields 4 and 8 FID = 011, 111	
Line	**ID**	**Line**	**ID**	**Line**	**ID**	**Line**	**ID**
1	SS	313	ES	626	SS	938	ES
2	SS	314	SS	627	SS	939	SS
3	SE	315	SS	628	SE	940	SS
4	EE	316	EE	629	EE	941	EE
5	EE	317	EE	630	EE	942	EE
6	-VV	318	EV	631	UVV	943	EB
7	UVV	319	UVV	632	UVV	944	-VV
8	UVV	320	UVV	633	UVV	945	UVV
•••	•••	•••	•••	•••	•••	•••	•••
308	UVV	621	UVV	933	UVV	1246	UVV
309	UVV	622	-VV	934	UVV	1247	UVV
310	-VV	623	-VE	935	UVV	1248	-VE
311	EE	624	EE	936	EE	1249	EE
312	EE	625	EE	937	EE	1250	EE

EE Equalization pulse
SE Half-line vertical sync pulse, half-line equalization pulse
SS Vertical sync pulse
ES Half-line equalization pulse, half-line vertical sync pulse
EB Equalization broad pulse
UVV Active video
-VV Active video with color burst suppressed
-VE Half-line video, half-line equalization pulse, color burst suppressed

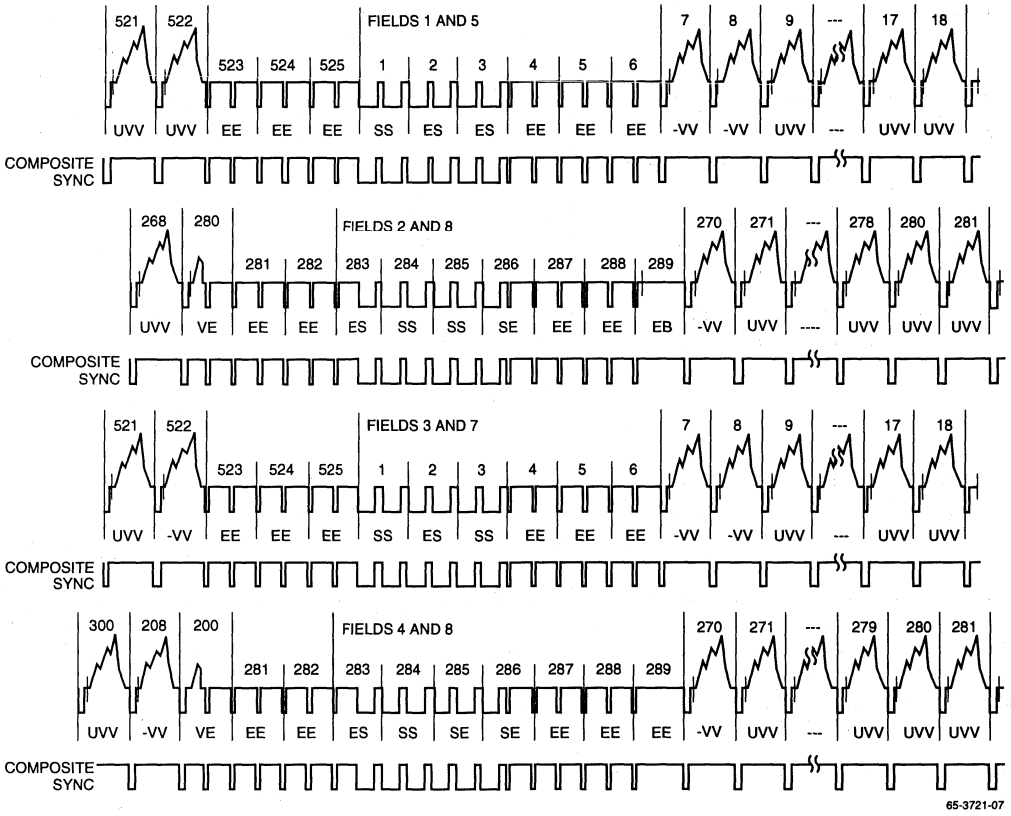


Figure 7. PAL-M Vertical Interval

Table 9. PAL-M Field/Line Sequence and Identification

Field 1 and 5 FID = 000, 100		Field 2 and 6 FID = 001, 101		Field 3 and 7 FID = 010, 110		Field 4 and 8 FID = 011, 111	
Line	ID	Line	ID	Line	ID	Line	ID
1	SS	263	ES	1	SS	263	ES
2	SS	264	SS	2	SS	264	SS
3	SS	265	SS	3	SS	265	SS
4	EE	266	SE	4	EE	266	SE
5	EE	267	EE	5	EE	267	EE
6	EE	268	EE	6	EE	268	EE
7	-VV	269	EB	7	-VV	269	EB
8	-VV	270	-VV	8	UVV	270	-VV
9	UVV	271	UVV	9	UVV	271	UVV
•••	•••	•••	•••	•••	•••	•••	•••
258	UVV	521	UVV	258	UVV	521	UVV
259	UVV	522	-VV	259	-VV	522	UVV
260	-VE	523	EE	260	-VE	523	EE
261	EE	524	EE	261	EE	524	EE
262	EE	525	EE	262	EE	525	EE

EE Equalization pulse
SS Vertical sync pulse
EB Equalization broad pulse
SE Half-line vertical sync pulse, half-line equalization pulse
ES Half-line equalization pulse, half-line vertical sync pulse
UVV Active video
-VV Active video with color burst suppressed
-VE Half-line video, half-line equalization pulse, color burst suppressed
UVV half-line black, half-line video

Subcarrier Generation and Synchronization

The color subcarrier is produced by an internal digital frequency synthesizer with programmable frequency and phase. The subcarrier synthesizer gets its frequency and phase values from the control registers or ancillary data packet.

The subcarrier is internally synchronized to establish and maintain a specific relationship between the leading edge of horizontal sync and color burst phase (SCH). In NTSC and PAL, SCH synchronization is performed every eight fields, on field 1 of the eight-field sequence. Proper subcarrier phase is maintained through the entire eight field set, including the 25 Hz offset in PAL-N,B,I systems

The subcarrier synthesizer seed value (stored in FREQ3, FREQ2, FREQ1, and FREQ0) depends upon the desired subcarrier frequency and the pixel rate:

$FREQ_{10}$ = (Subcarrier frequency / 13.5 MHz) x 2^{32}
= (Subcarrier cycles per line / pixels per line) x 2^{32}

Converting $FREQ_{10}$ to hexadecimal yields the values for the FREQ3, FREQ2, FREQ1, and FREQ0 registers.

SCH Phase Error Correction

SCH refers to the timing relationship between the 50% point of the leading edge of horizontal sync and the positive or negative zero-crossing of the color burst subcarrier reference. In PAL, SCH is defined for line 1 of field 1, but since there is no color burst on line 1, SCH is usually measured at line 7 of field 1. The need to specify SCH relative to a particular line in PAL is due to the 25 Hz offset of PAL subcarrier frequency. Since NTSC has no such 25 Hz offset, SCH applies to all lines.

Based upon the operating mode of the TMC22290, the subcarrier phase may be reset once every eight fields, on a line-by-line basis, or not at all (free run). The resetting of subcarrier phase is always synchronized with the 50% point of the falling edge of horizontal sync. When eight field reset is employed, the subcarrier is reset to the phase values found in Table 10.

Table 10. Subcarrier and Color Burst Reset Values

	NTSC	PAL-M	PAL-B,G,H,I,N
Digital field: Line number:	1 4	1 4	1 1
Subcarrier phase reset value:	180°	0°	0°
Resultant color burst phase:	0°	+135°	+135°

Note: Line numbering is in accordance with Figure 5, Figure 6, and Figure 7. Subcarrier and color burst phase are relative to the horizontal reference of the line specified above.

The SCHPH control register are used to compensate subcarrier phase for any group delay variation in external analog filters. This register adds a constant phase shift to the subcarrier. This phase offset is adjustable from 0° to 360° . An SCHPH value of 0000h equals 0° offset while an SCHPH value of 8000h is equal to 180°.

A 13-bit subcarrier phase value from the ancillary data packet will set the absolute phase of the subcarrier synthesizer on a line-by-line basis. If the phase values from the ancillary data are not used, the absolute phase of the synthesizer is set to zero. The SCHPH phase value is a phase offset added to subcarrier phase after the synthesizer.

Table 11. Standard Subcarrier Parameters

Standard	Horizontal Frequency (MHz)	Subcarrier Frequency (MHz)	FREQ Registers (hex)	PHASE Register (hex)	SCHPH Register (hex)
NTSC	15.734266	3.579545455	43E0F83E	0000	0000
PAL B,G,H,I	15.625000	4.43361875	54131596	0000	0000
PAL-M	15.734266	3.57561189	43CDDFC7	0000	0000
PAL-N	15.625000	3.58205625	43ED288D	0000	0000

Note: The PHASE Register is accessed via the ancillary data packet only.

Luminance Processing

During horizontal and vertical blanking, the luma processor generates blanking levels and properly timed and shaped sync and equalization pulses. During active video, it captures and rescales the incoming Y components and adds the results to the blank level to complete a proper monochrome television waveform, which is then upsampled 2:1 to drive the luma DAC and the composite adder.

For NTSC-EIA (5:2 white:sync, no black pedestal), the overall luma input-to-output transfer function for 0<Y<255 is:

luma out (IRE, relative to blank) =
(Y - 16) * 100/219

For NTSC and PAL-M (5:2, with 7.5 IRE pedestal), the equation becomes:

luma out (IRE, relative to blank) =
(Y - 16) * 92.5/219 + 7.5

For all common 625-line PAL standards (7:3, no pedestal), the equation becomes:

luma out (mV, relative to blank) =
(Y-16) * 700/219

Since Y=0 and Y=255 are reserved values in CCIR-601, a trap causes them to output black, i.e., 0mV or 0 IRE without pedestal, 7.5 IRE with pedestal.

Table 12. Luminance Input Codes

PD_{7-0} Input		Luma Level	NTSC, PAL-M Luma Level (IRE)		PAL-B, G, H, I, N Luma Level
Dec	Hex	(CCIR-601)	PEDEN = 0	PEDEN = 1	(mV)
255	FF	reserved	0	7.5	0
254	FE		108.7	108	761
235	EB	100% white	100	100	700
16	10	Black	0	7.5	0
1	01		-6.9	1.2	-48
0	00	reserved	0	7.5	0

Table 13. D/A Converter and Analog Levels

Video Level	NTSC, PAL-M		NTSC w/o Setup		PAL-B, G, H, I, N	
	D/A	IRE	D/A	IRE	D/A	mV
Maximum Output	511	137.2	511	137.2	511	977.5
100% white	405	100	405	100	400	700
Black	141	7.37	120	0	120	0
Blank	120	0	120	0	120	0
Sync	6	40	6	-40	0	-300
White-to-blank	285	100	285	100	280	700
White-to- sync	399	140	399	140	400	1000
Color burst	114	40	114	-40	120	300

Filtering Within the TMC22290

The TMC22290 incorporates internal digital filters to establish appropriate bandwidths and simplify external analog filter designs.

The chroma portion of the incoming digital video is band-limited to reduce edge effect and other distortions of the image compression process. Chrominance bandwidth is selected by CHRBW (control register 05, bit 5). When LOW, the chrominance passband attenuation is <3 dB ±650 kHz from f_{SC}. The stopband rejection is >20 dB outside f_{SC} ±2 MHz. When HIGH, the chrominance passband attenuation is <3 dB ±1.3 MHz from f_{SC}. The stopband rejection is >20 dB outside f_{SC} ±4 MHz.

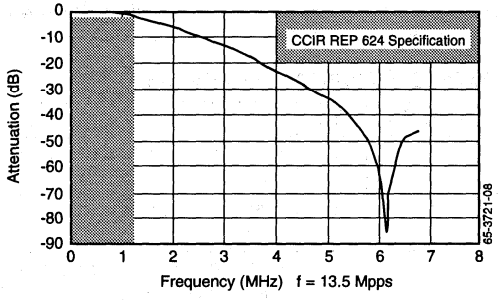


Figure 8. Color-Difference Low-Pass Filter Response

The Chroma Modulator output and the luminance data path are digitally filtered with sharp-cutoff low-pass interpolation filters. These filters ensure that aliased subcarrier, chrominance, and luminance frequencies are sufficiently suppressed in the frequency band above base-band video and below the pixel frequency ($f_S/4$ to 3 x $f_S/4$, where f_S is the PXCK frequency).

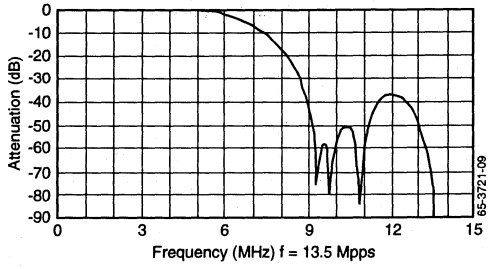


Figure 9. Chrominance and Luminance Interpolation Filter - Full Spectrum Response

Virtually all digital-to-analog reconstruction systems exhibit a high frequency roll-off as a result of the zero-order hold characteristic of classic D/A converters. This response is commonly referred to as a sin(x)/x response. It is a function of the sampling rate of the output D/A.

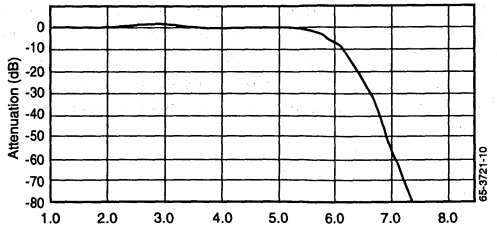


Figure 10. Chrominance and Luminance Interpolation Filter - Passband Detail

The TMC22290's digital interpolation filters convert the data stream to a sample rate of twice the pixel rate. This results in much less high frequency sin(x)/x rolloff and the output spectrum between $f_S/4$ and 3 x $f_S/4$ contains very little energy. Since there is so little signal energy in this frequency band, the demands placed on the output reconstruction filter

SET TOP BOX

are greatly reduced. The output filter needs to be flat to fS/4 and have good rejection at 3 x fS/4. The relaxed requirements greatly simplify the design of a filter with good phase response and low group delay distortion. A small amount of peaking may be used to compensate residual sin(x)/x rolloff.

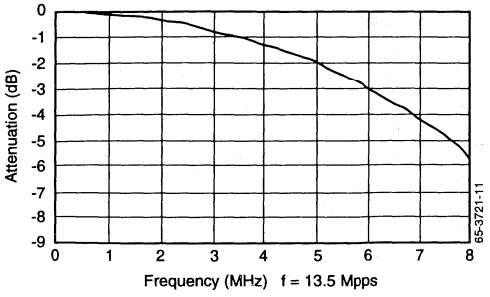


Figure 11. Sin(x)/x Response At 1x Pixel-Rate Conversion

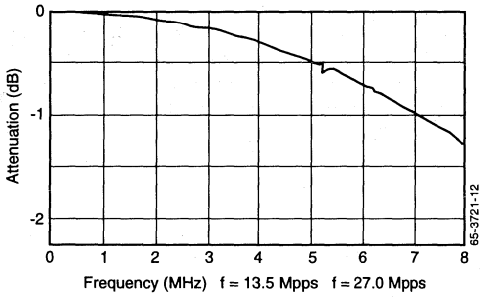


Figure 12. Sin(x)/x Response At 2X Pixel-Rate Conversion

Ancillary Data

The TMC22290 is designed to accept 15 words of ancillary data after the active video pixels at the end of each horizontal line. Ancillary data may occur once per line, once per field, once per eight fields, on random lines, or not al all. The TMC22290 does not assume ancillary data is present on a regular basis.

The first three words of ancillary data comprise the TRS signal (ANC2-0) which indicates the end of active video. Also known as the Ancillary Data Header, the TRS signal is a 00_h, FF_h, FF_h sequence. Except for the TRS words, ancillary data bit 0 (B_0, LSB) is odd parity for B_{7-1}.

The data type word (TT) is used to specify the ancillary data type. The TMC22290 compare this 7-bit value with the contents of the ANCID control register. If there is a match, the ancillary data will be processed. If there is no match, the TMC22290 ignores ancillary data.

The word count data (D_{11-0} in MM, LL) in the ancillary data packet is ignored. Ancillary data that matches the programmed Data Type is assumed to be 9 bytes long.

Ancillary phase data is used to program the MSBs of the PHASE register. ANCPHEN and PHV determine how ancillary phase data is used. When ancillary data is not present, the TMC22290 assumes PHV = LOW.

Table 14. ANCPHEN and PHV function

ANCPHEN	PHV	Description
0	x	Ignore ancillary phase data, set PHASE = 0
1	0	Ignore ancillary phase data, no change to PHASE
1	1	Load ancillary phase data into PHASE registers

Ancillary frequency data is used to program the 32-bits of the FREQ3-0 registers. ANCFREN and FRV determine how ancillary frequency data is used. When ancillary data is not present, the TMC22290 assumes FRV = LOW.

Table 15. ANCFREN and FRV function

ANCFREN	FRV	Description
0	x	Ignore ancillary frequency data
1	0	Ignore ancillary frequency data
1	1	Load ancillary frequency data into FREQ3-0 registers

Table 16. Ancillary Data Sequence

Word ID	Description	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
ANC2	Ancillary Data Header	0	0	0	0	0	0	0	0
ANC1	(Timing Reference	1	1	1	1	1	1	1	1
ANC0	Signal)	1	1	1	1	1	1	1	1
TT	Data Type	TT6	TT5	TT4	TT3	TT2	TT1	TT0	P
MM	Word	0	X	X	X	X	X	X	P
LL	Count	0	X	X	X	X	X	X	P
FIELD	Field ID / Synchronous Video Flag	x	x	x	$\overline{SVF}$	F2	F1	F0	P
	reserved	x	x	x	x	x	x	x	P
PH1	Subcarrier	PHV	PH_{12}	PH_{11}	PH_{10}	PH_9	PH_8	PH_7	P
PH0	Phase	PH_6	PH_5	PH_4	PH_3	PH_2	PH_1	PH_0	P
FR4		FRV	x	x	FR31	FR30	FR29	FR28	P
FR3	Subcarrier	FR_{27}	FR_{26}	FR_{25}	FR_{24}	FR_{23}	FR_{22}	FR_{21}	P
FR2		FR_{20}	FR_{19}	FR_{18}	FR_{17}	FR_{16}	FR_{15}	FR_{14}	P
FR1	Frequency	FR_{13}	FR_{12}	FR_{11}	FR_{10}	FR_9	FR_8	FR_7	P
FR0		FR_6	FR_5	FR_4	FR_3	FR_2	FR_1	FR_0	P

P = odd parity bit, x = reserved bit - set to 0

Table 17. Field Identification and Subcarrier Reset Modes

ANCTREN	$\overline{SVF}$	F_2	F_1	F_0	F (EAV)	Field ID / Subcarrier Reset Mode
Basic Mode						
0	x	x	x	x	0	odd field, reset subcarrier every 8 fields
0	x	x	x	x	1	even field
Genlocking Mode						
1	1	x	x	x	0	odd field, subcarrier free run
1	1	x	x	x	1	even field
Field Sequence Mode						
1	0	0	0	0	X	Field 1, reset subcarrier at field 1
1	0	0	0	1	X	Field 2
1	0	0	1	0	X	Field 3
1	0	0	1	1	X	Field 4
1	0	1	0	0	X	Field 5
1	0	1	0	1	X	Field 6
1	0	1	1	0	X	Field 7
1	0	1	1	1	X	Field 8

The F bit is part of the EAV timing reference code and tracks the F0 bit

Operating Modes

The field number bits (F_{2-0}) from the ancillary data packet FIELD word, are used to program the encoder's field counter depending upon the state of the synchronous video flag ($\overline{SVF}$) and the ANCTREN bit in the control register.

In the basic operating mode (ANCTREN = LOW), all timing is found in the F bit of EAV. F_{2-0} and $\overline{SVF}$ are ignored and the encoder subcarrier synthesizer is reset to the PHASE value every eight fields (when the field counter transitions from 111(field 8) to 000 (field 1).

In the basic mode, ANCFREN and ANCPHEN are typically set LOW, ignoring ancillary frequency and phase data. If ANCFREN and ANCPHEN are HIGH, the TMC22290 uses the incoming ancillary frequency and phase data on a line-by-line basis.

In genlocking mode (ANCTREN and $\overline{SVF}$ = HIGH), the subcarrier synthesizer is allowed to free run, with phase and frequency being set from the ancillary data packet PH_{12-0} and FR_{31-0} data. The field counter increments just like it does in basic mode.

Field sequence mode (ANCTREN = HIGH and $\overline{SVF}$=LOW), is the same as basic mode except that the field counter is set by the F_{2-0} bits in the FIELD word of ancillary data. If ancillary data is not present on a line, the field counter will continue to count as it does in basic mode. When ancillary data is present, the contents of the field counter are loaded with field data (F_{2-0}). In this way, the TMC22290 may be synchronized with an external source by sending field data only once.

Parallel Microprocessor Interface

The parallel microprocessor interface, active when $\overline{SER}$ is HIGH, employs an 14-line interface, with an 8-bit data bus and one address bit: two addresses are required for device programming and pointer-register management. Address bit 0 selects between reading/writing the register addresses and reading/writing register data. When writing, the address is presented along with a LOW on the $\overline{R/W}$ pin during the falling edge of $\overline{CS}$. Eight bits of data are presented on D_{7-0} during the subsequent rising edge of $\overline{CS}$. One additional falling edge of $\overline{CS}$ is needed to move input data to its assigned working registers.

In read mode, the address is accompanied by a HIGH on the $\overline{R/W}$ pin during a falling edge of $\overline{CS}$. The data output pins go to a low-impedance state t_{DOZ} ns after $\overline{CS}$ falls. Valid data is present on D_{7-0} t_{DOM} after the falling edge of $\overline{CS}$. Because this port operates asynchronously with the pixel timing, there is an uncertainty in this data valid output delay of one PXCK period. This uncertainty does not apply to t_{DOZ}.

Table 18. Parallel Port Control

ADR	R/W\	Action
1	0	Load D_{7-0} into Control Register pointer.
1	1	Read Control Register pointer on D_{7-0}.
0	0	Write D_{7-0} to addressed Control Register.
0	1	Read addressed Control Register on D_{7-0}.

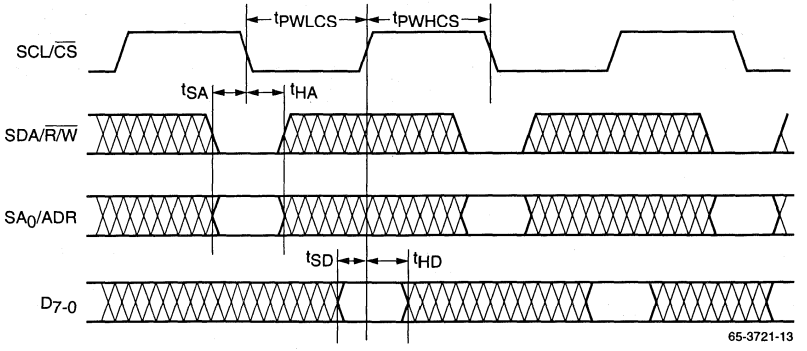


Figure 13. Microprocessor Parallel Port - Write Timing

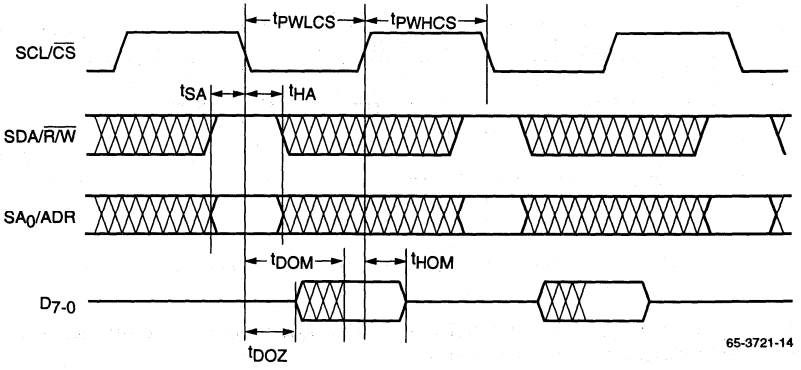


Figure 14. Microprocessor Parallel Port - Read Timing

Serial Control Port (R-Bus)

In addition to the 14-wire parallel port, a 2-wire serial control interface is also provided, and active when $\overline{SER}$ is LOW. Either port alone can control the entire chip. Up to four TMC22290 devices may be connected to the 2-wire serial interface with each device having a unique address.

The 2-wire interface comprises a clock (SCL/$\overline{CS}$) and a bi-directional data (SDA/$\overline{R/W}$) pin. The TMC22290 acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL/$\overline{CS}$ and SDA/$\overline{R/W}$ are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA/$\overline{R/W}$ line must be stable for the duration of the positive-going SCL/$\overline{CS}$ pulse. Data on SDA/$\overline{R/W}$ must change only when SCL/$\overline{CS}$ is LOW. If SDA/$\overline{R/W}$ changes state while SCL/$\overline{CS}$ is HIGH, the serial interface interprets that action as a start or stop sequence.

There are five components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL/$\overline{CS}$ and SDA/$\overline{R/W}$ are HIGH) communications are initiated by sending a start signal. The start signal is a HIGH-to-LOW transition on SDA/$\overline{R/W}$ while SCL/$\overline{CS}$ is HIGH. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a seven bit slave address and a single R/W bit. The R/W bit indicates the direction of data transfer, read from or write to the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA_0/ADR and SA_1 input pins in Table 19.), the TMC22290 acknowledges by bringing SDA/$\overline{R/W}$ LOW on the 9th SCL/$\overline{CS}$ pulse. If the addresses do not match, the TMC22290 does not acknowledge.

Table 19. Serial Port Addresses

A_6	A_5	A_4	A_3	A_2	A_1 (SA_1)	A_0 (SA_0)
0	0	0	1	1	0	0
0	0	0	1	1	0	1
0	0	0	1	1	1	0
0	0	0	1	1	1	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the TMC22290 does not acknowledge the master device during a write sequence, the SDA/$\overline{R/W}$ remains HIGH so the master can generate a stop signal. If the master device does not acknowledge the TMC22290 during a read sequence, the TMC22290 interprets this as "end of data." The SDA/$\overline{R/W}$ remains HIGH so the master can generate a stop signal.

Writing data to specific control registers of the TMC22290 requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 20h. Any base address higher than 20h will not produce an ACKnowledge signal. If no ACKnowledge is received from the master, the encoder will automatically stop sending data.

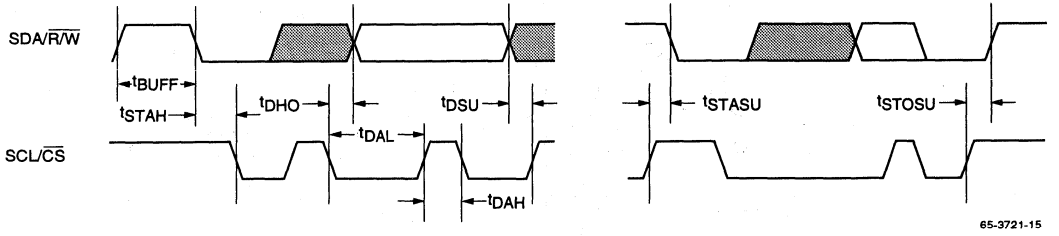


Figure 15. Serial Port Read/Write Timing

Data is read from the control registers of the TMC22290 in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/W bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the TMC22290, a stop signal must be sent. A stop signal comprises a LOW-to-HIGH transition of SDA/$\overline{R/W}$ while SCL/$\overline{CS}$ is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to one control register

↓ Start signal
↓ Slave Address byte (R/W bit = LOW)
↓ Base Address byte
↓ Data byte to base address
↓ Stop signal

Write to four consecutive control registers

↓ Start signal
↓ Slave Address byte (R/W bit = LOW)
↓ Base Address byte
↓ Data byte to base address
↓ Data byte to (base address + 1)
↓ Data byte to (base address + 2)
↓ Data byte to (base address + 3)
↓ Stop signal

Read from one control register

↓ Start signal
↓ Slave Address byte (R/W bit = LOW)
↓ Base Address byte
↓ Stop signal
↓ Start signal
↓ Slave Address byte (R/W bit = HIGH)
↓ Data byte from base address
↓ Stop signal

Read from four consecutive control registers

↓ Start signal
↓ Slave Address byte (R/W bit = LOW)
↓ Base Address byte
↓ Stop signal
↓ Start signal
↓ Slave Address byte (R/W bit = HIGH)
↓ Data byte from base address
↓ Data byte from (base address + 1)
↓ Data byte from (base address + 2)
↓ Data byte from (base address + 3)
↓ Stop signal

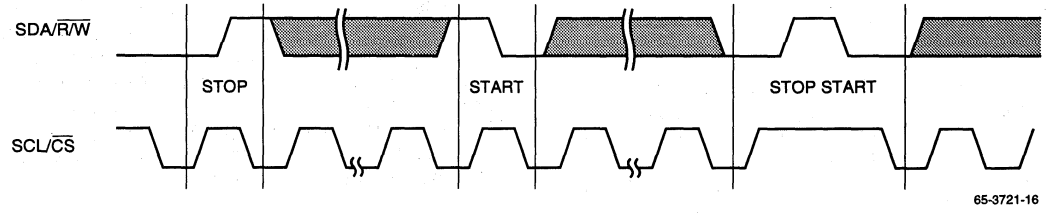


Figure 16. Serial Interface - Start/Stop Signal

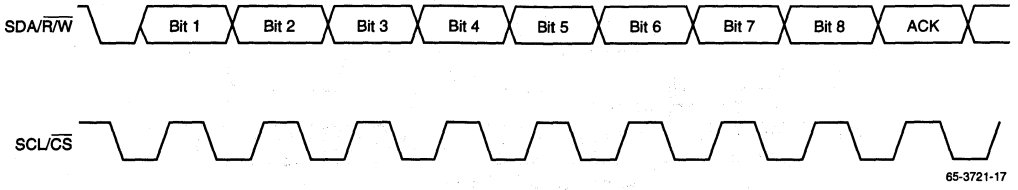


Figure 17. Serial Interface - Typical Byte Transfer

JTAG Test Interface

The JTAG test port accesses registers at every digital I/O pin except the JTAG test port pins.

Table 20 specifies the sequence of the test registers. The register number (Reg) indicates the order in which the register data is loaded and read (Reg 1 is loaded and read first, therefore it is at the end of the serial path). The scan path is 23 registers long. The six TEST pins function as JTAG registers.

The JTAG port is a 4-wire interface, following IEEE Std. 1149.1-1990 specifications. The Test Data Input (TDI) and Test Mode Select (TMS) inputs are referred to the rising edge of the Test ClocK (TCK) input. The Test Data Output (TDO) is referred to the falling edge of TCK.

The JTAG standard has been implemented into the TMC22290 without the UPDATE data register (it treats output pins and there are none on the TMC22290).

The CAPTURE Instruction Register is implemented with force value of 01 which allows SAMPLE or PRELOAD data to the data path.

The Instruction register contains two bits: IRM and IRL (TDI shift to IRM; IRM shift to IRL; IRL shift to TDO) - see Table 21.

There are 16 states in TAP and all are fully implemented.

In general, TMS is commanding the state machine and puts the system into JTAG states. The TMC22290 can be operated freely because there is no means to interrupt its function. There is NO output driver related to the JTAG data path.

While TMS determines the state, there are only a few events that may happen:

1. Capture DR. In this state, all the data at the pins will be LOADed into the data scan path only if IRM is not equal to IRL. If IRM = IRL, even though the state machine at this state, NO ACTION will take place.

2. Shift DR. In this state, the data scan path is transferring data from high order bit to low order bits. It is always operational regardless of the contents of IRM and IRL.

3. Capture IR. While TMS captures IR state, the TMC22290 automatically loads 01 to the pre-instruction register (IRMp and IRLp respectively).

4. Shift IR. In this state, shift TDI to IRMp, IRMp to IRLp, and IRLp to TDO.

5. Update IR. In this state, TMC22290 LOAD contents of the Instruction register from the PRELOADED (or SHIFTED) IR to execution Instruction register (double buffered.)

The DATA SCAN PATH Register is a serial SHIFT, parallel LOAD shift register. While in Shift DR state, TMC22290 does SHIFT. While the IR (instruction register) is 01 or 10, and the TAP state is at Capture DR state, TMC22290 does LOAD.

For each input PIN (tri-state pins included, but not the analog pins), the TMC22290 has a 2:1 multiplexer and register. One of the multiplexer inputs is the PAD and the other is the shifted data from the higher order scan path.

Table 20. JTAG Sequence

Reg	Pin	Reg	Pin	Reg	Pin
1	$\overline{\text{RESET}}$	9	PD_1	17	D_6
2	PXCK	10	PD_0	18	D_5
3	PD_7	11	SA_1	19	D_4
4	PD_6	12	SA_0\ADR	20	D_3
5	PD_5	13	SDA/$\overline{\text{R/W}}$	21	D_2
6	PD_4	14	SCL/$\overline{\text{CS}}$	22	D_1
7	PD_3	15	$\overline{\text{SER}}$	23	D_0
8	PD_2	16	D_7		

Table 21. Function of IRM and IRL

IRM	IRL	Function
0	0	EXTEST, no effect while shift at DR, data keeps on shifting.
0	1	SAMPLE / PRELOAD At capture DR state, load all input pins parallel to data scan path.
1	0	Same as SAMPLE / PRELOAD
1	1	BYPASS TDI bypass to TDO

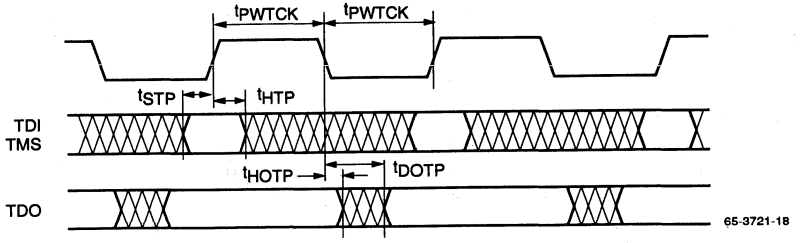


Figure 18. JTAG Test Port Timing

Equivalent Circuits

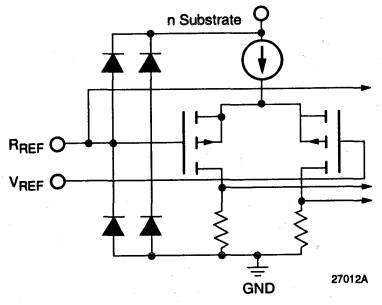


Figure 19. Equivalent Analog Input Circuit

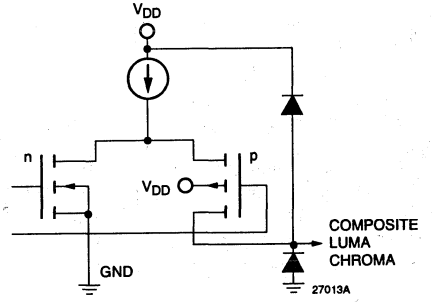


Figure 20. Equivalent Analog Output Circuit

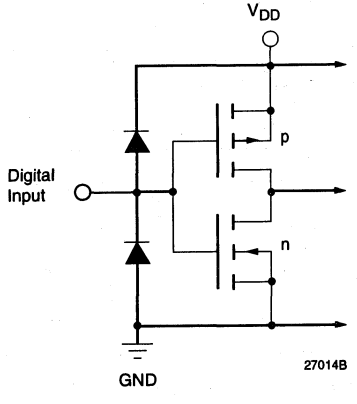


Figure 21. Equivalent Digital Input Circuit

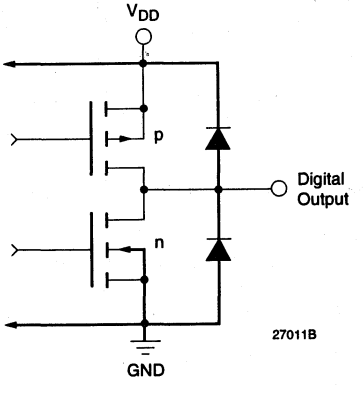


Figure 22. Equivalent Digital Output Circuit

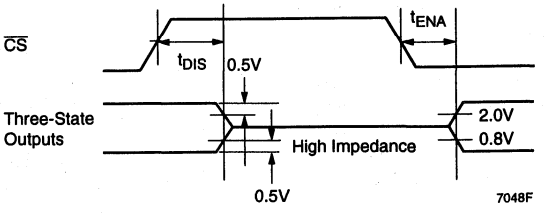


Figure 23. Threshold Levels for Three-State Measurement

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltage	-0.5		+7.0	V
Digital Inputs				
Applied Voltage	-0.5		V_{DD}+0.5	V
Forced current [3, 4]	-20.0		+20.0	mA
Output				
Applied voltage [2]	-0.5		V_{DD} + 0.5	V
Forced current [3, 4]	-3.0		+6.0	mA
Short circuit duration (single output in HIGH state to ground)			1 second	
Analog Output Short circuit duration (all outputs to ground)			infinite	
Temperature				
Operating, ambient	-20		110	°C
junction			+140	°C
Lead, soldering (10 seconds)			+300	°C
Vapor Phase soldering (1 minute)			+220	°C
Storage	-65		+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

SET TOP BOX

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH				
	TTL Compatible Inputs	2.0		V_{DD}	V
	Serial Port (SDA, SCL)	.7V_{DD}			V
	CLK Input	2.4		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW				V
	TTL Compatible Inputs	GND		0.8	V
	Serial Port (SDA, SCL)	GND		0.3V_{DD}	V
V_{REF}	External Reference Voltage		1.235		V
I_{REF}	D/A Converter Reference Current		1.57		mA
	(I_{REF}=V_{REF}/R_{REF}), flowing out of the R_{REF} pin				
R_{REF}	External Reference Resistor, V_{REF}=NOM		787		Ω
I_{OH}	Output Current, Logic HIGH (D_{7-0}, TDO)			-2.0	mA
I_{OL}	Output Current, Logic LOW (D_{7-0}, TDO)			4.0	mA
	Output Current, Logic LOW (SDA)			6.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C

Operating Conditions (continued)

Parameter		Min	Nom	Max	Units
Pixel Interface					
f_{PXL}	Pixel Rate		13.5		Mpps
f_{PXCK}	Master Clock Rate, = 2X pixel rate		27.0		MHz
t_{PWHPX}	PXCK pulse width, HIGH	10			ns
t_{PWLPX}	PXCK pulse width, LOW	15			ns
t_{SP}	PD_{7-0} Setup Time	10			ns
t_{HP}	PD_{7-0} Hold Time	0			ns
Parallel Microprocessor Interface					
t_{PWLCS}	CS\ Pulse Width, LOW	95			ns
t_{PWHCS}	CS\ Pulse Width, HIGH	30			ns
t_{SA}	Address Setup Time	10			ns
t_{HA}	Address Hold Time	0			ns
t_{SD}	Data Setup Time (write)	15			ns
t_{HD}	Data Hold Time (write)	8			ns
t_{SR}	Reset Setup Time	15			ns
t_{HR}	Reset Hold Time	2			ns
Serial Microprocessor Interface					
t_{DAL}	SCL Pulse Width, LOW		1.3		µs
t_{DAH}	SCL Pulse Width, HIGH		0.6		µs
t_{STAH}	SDA Start Hold Time		0.6		µs
t_{STASU}	SCL to SDA Setup Time (START)		0.6		µs
t_{STOSU}	SCL to SDA Setup Time (STOP)		0.6		ns
t_{BUFF}	SDA Stop to SDA Start Hold Time		1.3		µs
t_{DSU}	SDA to SCL Data Setup Time		300		ns
tDHO	SCL to SDA Hold Time		300		ns
JTAG Interface					
f_{TCK}	Test Clock (TCK) Rate			10	Mhz
t_{PWLTCK}	TCK Pulse Width, LOW	10			ns
t_{PWHTCK}	TCK Pulse Width, HIGH	10			ns
t_{STP}	Test Port Setup Time, TDI, TMS	10			ns
t_{HTP}	Test Port Hold Time, TDI, TMS	0			ns

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
I_{DD}	Power Supply Current[1]	V_{DD} = Max, f_{PXCK} = 27MHz			125	
I_{DDQ}	Power Supply Current, DACs disabled[2]	V_{DD} = Max, f_{PXCK} = 27MHz			75	mA
V_{RO}	Voltage Reference Output		0.988	1.235	1.482	V
Z_{RO}	VREF Output Impedance			1000		Ω
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = VDD			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = VDD			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	D_{7-0}, TDO, I_{OH} = MAX	2.4			V
V_{OL}	Output Voltage, LOW	D_{7-0}, TDO, I_{OL} = MAX			0.4	V
		SDA, I_{OL} = 3mA			0.4	V
		SDA, I_{OL} = 6mA			0.6	V
C_I	Digital Input Capacitance			4	10	pF
C_I	Digital Output Capacitance			10		pF
V_{OC}	Video Output Compliance		-0.3		1.6	V
R_{OUT}	Video Output Resistance			15		kΩ
C_{OUT}	Video Output Capacitance	I_{OUT} = 0mA, f = 1MHz		15	25	pF

Notes:

1. Maximum I_{DD} with V_{DD} = MAX and T_A = MIN. Outputs loaded wtih 75Ω.
2. I_{DDQ} when YCDIS = COMPDIS = HIGH, disabling D/A converters.

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DOZ}	Output Delay, $\overline{CS}$ to low-Z		10			ns
t_{HOM}	Output Hold Time, $\overline{CS}$ to high-Z		10			ns
t_{DOM}	Output Delay, $\overline{CS}$ to Data Valid			30		ns
t_{DOTP}	Output Delay, TCK to TDO Valid				30	ns
t_{HOTP}	Output Hold Time, TCK to TDO Valid			5		ns
t_R	D/A Output Current Risetime	10% to 90% of full scale		2		ns
t_F	D/A Output Current Falltime	90% to 10% of full scale		2		ns
t_{DOV}	Analog Output Delay			20		ns

Note: Timing reference points are at the 50% level. Analog C_{LOAD} <10pF, D_{7-0} load <40pF.

System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Units
RES	D/A Converter Resolution		9	9	9	Bits
dp	Differential Phase	PXCK = 27 MHz, 40 IRE Ramp		.51	1.0	degree
dg	Differential Gain	PXCK = 27 MHz, 40 IRE Ramp		.8	1.5	%
CNLP	Chroma Nonlinear Phase	NTC-7 Combination		.1	±1.25	degree
CNLG	Chroma Nonlinear Gain	NTC-7 Combination		.2	±1.0	%
CLIM	Chroma/Luma Intermodulation	NTC-7 Combination		.05		IRE
CLGI	Chroma/Luma Gain inequality	NTC-7 Composite		97.6		%
CLDI	Chroma/Luma Delay inequality	NTC-7 Composite	-5	0	5	ns
LNLD	Luma Nonlinear Distortion	NTC-7		1.0		%
FTWD	Field Time Waveform Distortion	NTC-7		.6		%
LTWD	Line Time Waveform Distortion	NTC-7		.1		%
LOTWD	Long Time Waveform Distortion, initial and peak overshoot	10% / 90% APL Bounce				IRE
LOTWD	Long Time Waveform Distortion, peak overshoot	after 5 seconds, 10% / 90% APL Bounce				IRE
LDCOFF	Line-by-Line DC Offset					IRE
DYNG	Dynamic Gain	NTC-7				IRE
NOISE	Noise Level (Note 1)	100% unmod. ramp		-65.4		dB rms
NOISE	Noise Level (Note 2)	100% unmod. ramp				dB rms
CAMN	Chroma AM Noise	Red field		-59		dB rms
CPMN	Chroma PM Noise	Red field		-59		dB rms
SYRF	Sync Pulse Rise and Fall Time					ns
BERF	Burst envelope Rise and Fall Time					ns
PSRR	Power Supply Rejection Ratio	C_{BYP} = 0.1 µF, f = 1 kHz		0.5		%/ %V_{DD}

Notes:

1. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, with Tilt Null ON measured using VM700 "Measure Mode."
2. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, measured using VM700 "Auto Mode."

Applications Information

The circuit in Figure 25 shows the connection of power supply voltages, output reconstruction filters and the external voltage reference. All V_{DD} pins should be connected to the same power source.

The full-scale output voltage level, V_{OUT}, on the COMPOSITE, LUMA, and CHROMA pins is found from:

$$V_{OUT} = I_{OUT} \times RL = K \times I_{REF} \times R_L$$

$$= K \times (V_{REF}/R_{REF}) \times R_L$$

where:

1. I_{OUT} is the full-scale output current sourced by the TMC22290 D/A converters.
2. R_L is the net resistive load on the COMPOSITE, CHROMA, and LUMA output pins.
3. K is a constant for the TMC22290 D/A converters (approximately equal to 10.4).
4. I_{REF} is the reference current flowing out of the R_{REF} pin to ground.

5. V_{REF} is the voltage measured on the V_{REF} pin.

6. R_{REF} is the total resistance connected between the R_{REF} pin and ground.

The reference voltage in Figure 25 is from an LM185 1.2 Volt band-gap reference. The 392 Ohm resistor connected from R_{REF} to ground sets the overall "gain" of the three D/A converters of the TMC22290. Varying R_{REF} ±5% will cause the full-scale output voltage on COMPOSITE, LUMA, and CHROMA to vary by ±5%.

The suggested output reconstruction filter is the same one used on the TMC2063P7C Demonstration Board. The phase and frequency response of this filter is shown in Figure 24.

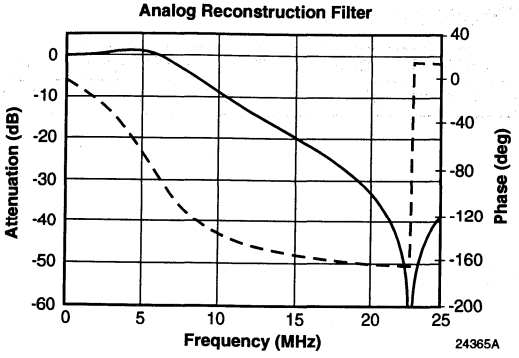


Figure 24. Response of Recommended Output Filter

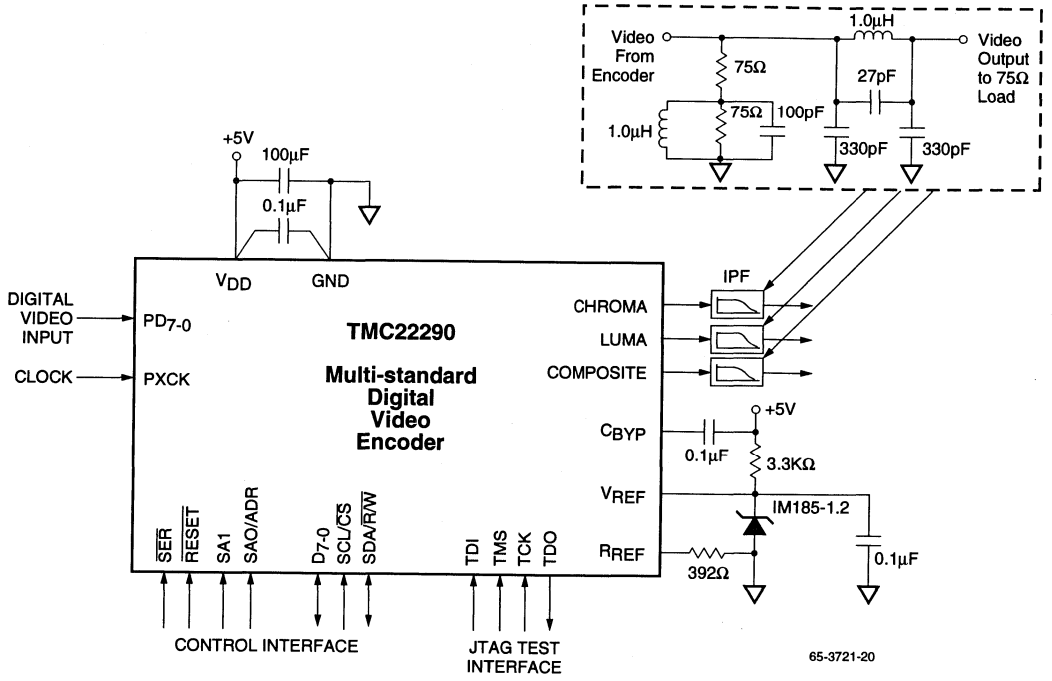


Figure 25. Typical Application Circuit

SET TOP BOX

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC22290R2C	0°C to 70°C	Commercial	44-Lead PLCC	22290R2C

TMC2490

Multistandard Digital Video Encoder

Features

- All-Digital Video Encoding
- Internal Digital Subcarrier Synthesizer
- 8-Bit Parallel CCIR-601/CCIR-656/ANSI/SMPTE 125M Input Format
- CCIR-624/SMPTE-170M Compliant Output
- Switchable Chrominance Bandwidth
- Switchable Pedestal with Gain Compensation
- Pre-Programmed Horizontal and Vertical Timing
- 13.5 Mpps Pixel Rate
- Master or slave (CCIR656) operation
- MPEG Interface
- Internal Interpolation Filters Simplify Output Reconstruction Filters
- 9-Bit D/A Converters for Video Reconstruction
- Supports NTSC and PAL Standards
- Output Encoding Per Macrovision Copy Protection (Revision 6) Available (TMC2491)
- Closed-Caption Waveform Insertion
- Simultaneous S-Video (Y/C) Output
- Controlled Edge Rates
- JTAG (IEEE Std 1149.1-1990) Test Interface
- Single +5V Power Supply
- 44 Lead PLCC Package
- Parallel and Serial Control Interface

Applications

- Settop Digital Cable Television Receivers
- Settop Digital Satellite Television Receivers
- Studio Parallel CCIR-601 to Analog Conversion

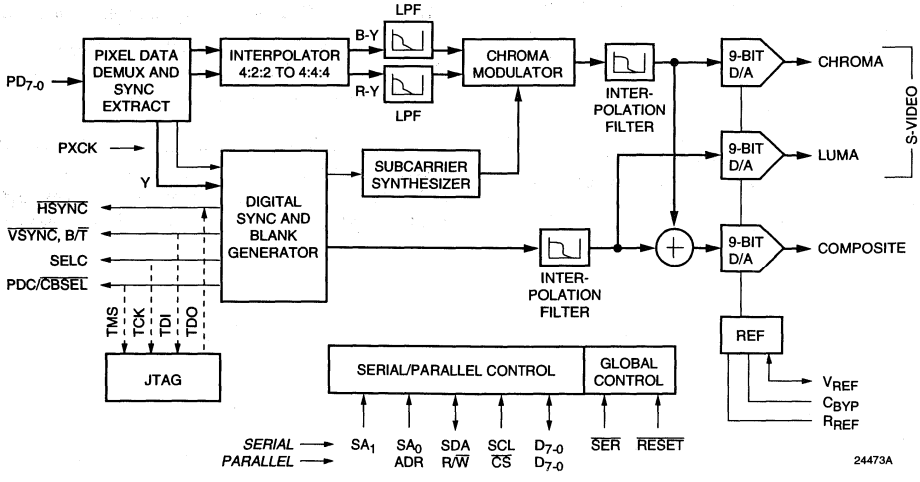
Description

The TMC2490 video encoder converts digital component video (in 8-bit parallel CCIR-601/656 or ANSI/SMPTE 125M format) into a standard analog baseband television (NTSC, NTSC-EIA, all PAL standards) signal with a modulated color subcarrier. Both composite (single lead) and S-Video (separate chroma and luma) formats are active simultaneously at all three analog outputs. Each video output generates a standard video signal capable of driving a singly- or doubly-terminated 75 Ohm load.

The TMC2490 is fabricated in a submicron CMOS process and is packaged in a 44-lead PLCC. Performance is guaranteed over the full 0°C to 70°C operating temperature range.

SET TOP BOX

Block Diagram



Rev. 0.9.3

Functional Description

The TMC2490 is a fully-integrated digital video encoder with simultaneous composite and Y/C (S-Video) outputs, compatible with NTSC, NTSC-EIA, and all PAL television standards. No external component selection or tuning is required.

To prevent unauthorized video taping, the output data stream may be modified per the Macrovision copy protection system (Revision 6). This feature is available on the TMC2491 only to Macrovision licensees. Consult the factory for information.

Digital component video is accepted at the PD port in 8-bit parallel CCIR-601/656 format. It is demultiplexed into luminance and chrominance components. The chrominance components modulate a digitally synthesized subcarrier. The luminance and chrominance signals are then separately interpolated to twice the input pixel rate and converted to analog signals by 9-bit D/A converters. They are also digitally combined and the resulting composite signal is output by a third 9-bit D/A converter.

The TMC2490 operates from a single clock at 27 MHz, twice the system pixel rate. Programmable control registers allow software control of subcarrier frequency and phase parameters. Incoming YC_BC_R422 digital video is interpolated to YC_BC_R444 format for encoding.

Internal control registers can be accessed over a standard 8-bit parallel microprocessor port or a 2-pin (clock and data) serial port.

Sync Generator

The TMC2490 operates in master or slave mode. In slave mode, it extracts its horizontal and vertical sync timing and field information from the CCIR-656 SAV (Start of Active Video) and EAV (End of Active Video) signal in the incoming data stream. In master mode, it generates a 13.5MHz timebase and sends line and field synchronizing signals to the host system.

Horizontal and vertical synchronization pulses in the analog output are digitally generated by the TMC2490 with controlled rise and fall times on all sync edges, the beginning and end of active video, and the burst envelope.

MSB		LSB
PD_7	C_B (n)	PD_0
PD_7	Y (n)	PD_0
PD_7	C_R (n)	PD_0
PD_7	Y (n+1)	PD_0

Figure 1. Pixel Data Format

Chroma Modulator

A digital subcarrier synthesizer generates the reference for a quadrature modulator, producing a digital chrominance signal. The chroma bandwidth may be programmed to 650kHz or 1.3 MHz.

Interpolation Filters

Interpolation filters on the luminance and chrominance signals double the pixel rate before D/A conversion. This low-pass filtering and oversampling process reduces sin(x)/x roll-off, and greatly simplifies the analog reconstruction filter required after the D/A converters.

D/A Converters

Analog outputs of the TMC2490 are driven by three 9-bit D/A converters, operating at 27 MHz. The outputs drive standard video levels into 37.5 or 75 Ohm loads. An internal voltage reference is used to provide reference current for the D/A converters. For more accurate video levels, an external fixed or variable voltage reference source is accommodated. The video signal levels from the TMC2490 may be adjusted to overcome the insertion loss of analog low-pass output filters by varying R_{REF} or V_{REF}.

Parallel and Serial Microprocessor Interfaces

The parallel microprocessor interface employs 11 pins. These are shared with the serial interface. A single pin, $\overline{SER}$, selects between the two interface modes.

In parallel interface mode, one address pin is decoded for access to the internal control register and its pointer. Controls are reached by loading a desired address through the 8-bit D_{7-0} port, followed by the desired data (read or write)

for that address. The control register address pointer auto-increments to address 22h and then remains there.

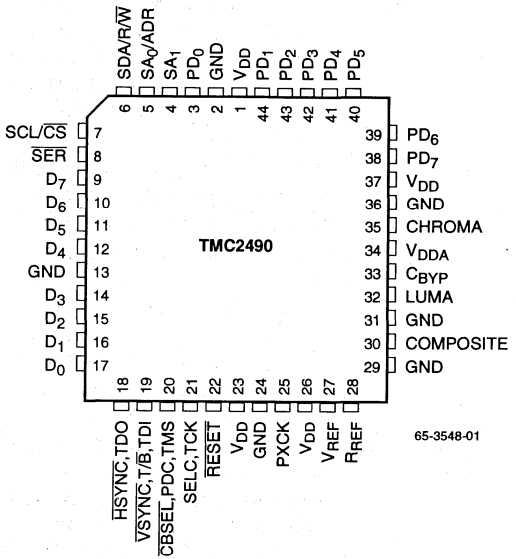
A 2-line serial interface is also provided on the TMC2490 for initialization and control. The same set of registers accessed by the parallel port is available to the serial port.

The $\overline{\text{RESET}}$ pin sets all internal state machines and control registers to their initialized conditions, disables the analog outputs, and places the encoder in a reset mode. At power-up, the encoder is automatically initialized in NTSC-M format.

JTAG Test Interface

The TMC2490 includes a standard 4-line JTAG (IEEE Std 1149.1-1990) test interface port, providing access to all digital input/output data pins. This is provided to facilitate board-level testing of the TMC2490.

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Value	Pin Function Description
Clock			
PXCK	25	TTL	**Pixel Clock Input.** This 27.0 MHz clock is internally divided by 2 to generate the internal pixel clock. PXCK drives the entire TMC2490, except the asynchronous microprocessor interface. All internal registers are strobed on the rising edge of PXCK.
Data Input Port			
PD_{7-0}	38–44, 3	TTL	**Pixel Data Inputs.** Video data enter the TMC2490 on PD7-0 (Figure 1).
Microprocessor Interface			
D_{7-0}	9–12, 14–17	TTL	**Data I/O, General Purpose I/O, Chroma Input Port.** When $\overline{SER}$ is HIGH, all control parameters are loaded into and read back over this 8-bit port. When $\overline{SER}$ = LOW, D_0 can serve as a composite sync output, D_1 outputs a burst flag during the back porch, D_{2-5} are General Purpose Outputs, and D_{6-7} are General Purpose Inputs.
$\overline{RESET}$	22	TTL	**Master Reset Input.** Bringing $\overline{RESET}$ LOW forces the internal state machines to their starting states and disables all outputs.
SA_1	4	TTL	**Serial/Parallel Port Select.** When $\overline{SER}$ is LOW, SA_1 in conjunction with SA_0 selects one of four addresses for the TMC2490.
SA_0, ADR	5	TTL	**Serial/Parallel Port Select.** When $\overline{SER}$ is LOW, SA_0 in conjunction with SA_1 selects one-of-four addresses for the TMC2490. When $\overline{SER}$ is HIGH, this control governs whether the parallel microprocessor interface selects a table address or reads/writes table contents.
SDA, R/$\overline{W}$	6	R-Bus/TTL	**Serial Data/Read/Write Control.** When $\overline{SER}$ is LOW, SDA is the data line of the serial interface. When $\overline{SER}$ is HIGH, the pin is the read/write control for the parallel interface. When R/$\overline{W}$ and $\overline{CS}$ are LOW, the microprocessor can write to the control registers over D_{7-0}. When R/$\overline{W}$ is HIGH and $\overline{CS}$ is LOW, it can read the contents of any selected control register over D_{7-0}.
SCL, $\overline{CS}$	7	R-Bus/TTL	**Serial Clock/Chip Select.** When $\overline{SER}$ is LOW, SCL is the clock line of the serial interface. When $\overline{SER}$ is HIGH, the pin is the chip select control for the parallel interface. When $\overline{CS}$ is HIGH, the microprocessor interface port, D_{7-0}, is set to HIGH impedance and ignored. When $\overline{CS}$ is LOW, the microprocessor can read or write parameters over D_{7-0}.
$\overline{SER}$	8	TTL	**Serial/Parallel Port Select.** When LOW, the 2-line serial interface is activated. Pins 5, 6, and 7 function as SA_0, SDA, and SCL respectively. When HIGH, the parallel interface port is active and pins 5, 6, and 7 function as ADR, R/$\overline{W}$, and $\overline{CS}$ respectively.
Outputs			
CHROMA	35	1.35V p-p	**Chrominance-only Video.** Analog output of chrominance D/A converter, maximum output is 1.35 volts peak-to-peak into a doubly terminated 75 Ohm load.
COMPOSITE	30	1.35V p-p	**Composite NTSC/PAL Video.** Analog output of composite D/A converter, maximum output is 1.35 volts peak-to-peak into a doubly terminated 75 Ohm load.

Preliminary Information

Pin Descriptions (continued)

Pin Name	Pin Number	Value	Pin Function Description
LUMA	32	1.35V p-p	**Luminance-only Video.** Analog output of luminance D/A converter, maximum output is 1.35 volts peak-to-peak into a doubly terminated 75 Ohm load.
Analog Interface			
C_{BYP}	33	0.1µF	**Reference Bypass Capacitor.** Connection point for 0.1 µF decoupling capacitor to V_{DD} at pin 34..
R_{REF}	28	787Ω	**Current-setting Resistor.** Connection point for external current-setting resistor for D/A converters. The resistor is connected between R_{REF} and GND. Output video levels are inversely proportional to the value of R_{REF}.
V_{REF}	27	+1.235V	**Voltage Reference Input.** External voltage reference input, internal voltage reference output, nominally 1.235 V.
SYNC Out and JTAG Test Interface			
$\overline{HSYNC}$, TDO	18	TTL	**Horizontal Sync Out/JTAG Data Output Port.** Dual-function pin.
$\overline{VSYNC}$, T/$\overline{B}$, TDI	19	TTL	**Vertical Sync I/O, Odd/Even Field ID Output, and JTAG Data Input.** Triple-function pin.
$\overline{CBSEL}$, PDC, TMS	20	TTL	**Pixel Data Phase Output, Video Blanking Output, and JTAG Scan Select Port.** Triple-function pin.
SELC, TCK	21	TTL	**Luma/Chroma MUX Control and JTAG Scan Clock Input.** Dual-function pin.
Power Supply			
V_{DD}	1, 23, 26, 37	+5V	**Power Supply.** Positive power supply.
GND	2, 13, 24, 29, 31, 36	0.0V	**Ground.** Ground.
V_{DDA}	34	+5V	**Analog Power Supply.** Positive power supply.

Control Registers

The TMC2490 is initialized and controlled by a set of registers which determine the operating modes.

An external controller is employed to write and read the Control Registers through either the 8-bit parallel or 2-line serial interface port. The parallel port, D7-0, is governed by pins $\overline{CS}$, R/$\overline{W}$, and ADR. The serial port is controlled by SDA and SCL.

Table 1. Control Register Map

Reg	Bit	Mnemonic	Function
TMC2490 Identification Registers (Read only)			
00	7-0	PARTID2	Reads back 94h
01	7-0	PARTID1	Reads back 24h
02	7-0	PARTID0	Reads back 90h
03	7-0	REVID	Silicon revision #
Global Control Register			
04	7	MASTER	Master Mode
04	6	Reserved	Program LOW
04	5	YCDELAY	Luma to chroma delay
04	4	RAMPEN	Modulated ramp enable
04	3	YCDIS	LUMA, CHROMA disable
04	2	COMPDIS	COMPOSITE disable
04	1-0	FORMAT	Television standard select
Video Output Control Register			
05	7	PALN	Select PAL-N Subcarrier
05	6	$\overline{BURSTF}$	Burst flag disable
05	5	CHRBW	Chroma bandwidth select
05	4	SYNCDIS	Sync pulse disable
05	3	BURDIS	Color burst disable
05	2	LUMDIS	Luminance disable
05	1	CHRDIS	Chrominance disable
05	0	PEDEN	Pedestal enable
Field ID Register			
06	7-6	Reserved	Program LOW
06	5-3	FIELD	Field ID (Read only)
06	2-0	Reserved	Program LOW
Reserved Registers			
07-0D	7-0	Reserved	Program LOW
General Purpose Port Register			
0E	7	PORT7-6	General purpose Inputs
0E	6	PORT5-2	General purpose Outputs
0E	1	BURSTF	Burst Flag Output
0E	0	CSYNC	Composite Sync Output
General Control Register			
0F	7	PED21	VBI Pedestal Enable
0F	6	$\overline{JTAGEN}$	JTAG Enable
0F	5	VSEL	Vertical Sync Select
0F	4	CBSEL	CBSEL/PDC Pin Function
0F	3	VBIEN	VBI Pixel Data Enable
0F	2-0	Reserved	Program LOW
Reserved Registers			
10-1F	7-0	Reserved	May be left unprogrammed
Closed-Caption Insertion Registers			
20	7-0	CCD1	First Byte of CC Data
21	7-0	CCD2	Second Byte of CC Data
22	7	CCON	Enable CC Data Packet
22	6	CCRTS	Request To Send Data
22	5	CCPAR	Auto Parity Generation
22	4	CCFLD	CC Field Select
22	3-0	CCLINE	CC Line Select

Notes:

1. For each register listed above, all bits not specified are reserved and should be set to zero to ensure proper operation.

Table 2. Default Register Values on Reset

Reg	Dflt	Reg	Dflt	Reg	Dflt	Reg	Dflt	Reg	Dflt
00	94	04	00	08	00	0C	00	20	80
01	24	05	00	09	00	0D	00	21	80
02	90	06	00	0A	00	0E	00	22	00
03	xx	07	00	0B	00	0F	00		

Control Register Definitions

Reg	Bit	Name	Description
00	7–0	PARTID2	Reads back 94h
01	7–0	PARTID1	Reads back 24h
02	7–0	PARTID0	Reads back 90h
03	7–0	REVID	Reads back a value corresponding to the revision letter of the silicon.

Global Control Register (04)

7	6	5	4	3	2	1	0
MASTER	Reserved	YCDELAY	RAMPEN	YCDIS	COMPDIS	FORMAT	

Reg	Bit	Name	Description
04	7	MASTER	**Master Mode.** When MASTER = 1, the encoder generates its own video timing and outputs signals $\overline{\text{VSYNC}}$ (or T/$\overline{\text{B}}$), $\overline{\text{HSYNC}}$, SELC, and PDC (or CBSEL). When MASTER = 0, the TMC2490 extracts timing from the embedded EAV codeword in the video datastream and optionally outputs signals $\overline{\text{VSYNC}}$ (or T/$\overline{\text{B}}$), $\overline{\text{HSYNC}}$, SELC, and PDC (or CBSEL).
04	6	Reserved	Program LOW
04	5	YCDELAY	**Luma to chroma delay.** When HIGH, the luminance path within the TMC2490 is delayed by one PXCK period. The delay applies to both COMPOSITE and LUMA outputs and may be used to compensate for group delay variation of external filters. When LOW, luminance and chrominance have the same latency.
04	4	RAMPEN	**Modulated ramp enable.** When HIGH, the TMC2490 outputs a modulated ramp test signal. When LOW, incoming digital video is encoded.
04	3	YCDIS	**LUMA, CHROMA disable.** When HIGH, the LUMA and CHROMA outputs are disabled, reducing power consumption. Set LOW for normal enabled operation.
04	2	COMPDIS	**COMPOSITE disable.** When HIGH, the COMPOSITE output is disabled. Set LOW for normal enabled operation.
04	1–0	FORMAT	**Television standard select.** Selects basic H&V timing parameters and subcarrier frequency. Pedestal level and chrominance bandwidth are independently programmed. 0 0 NTSC 0 1 PAL-B,G,H,I,N 1 0 PAL-M 1 1 Reserved

SET TOP BOX

Control Register Definitions (continued)

Video Output Control Register (05)

7	6	5	4	3	2	1	0
PALN	$\overline{\text{BURSTF}}$	CHRBW	SYNCDIS	BURDIS	LUMDIS	CHRDIS	PEDEN

Reg	Bit	Name	Description
05	7	PALN	**Select PAL-N Subcarrier.** When HIGH, selects PAL-N subcarrier frequency. When LOW, the encoder produces the PAL-B,G,H,I subcarrier. Program LOW for NTSC and PAL-M video.
05	6	$\overline{\text{BURSTF}}$	**Burst flag disable.** When $\overline{\text{BURSTF}}$ is LOW, a clamp gate signal is produced on the D1 output and register 0E bit 1.
05	5	CHRBW	**Chroma bandwidth select.** When LOW, the chrominance bandwidth is ±650 kHz. When HIGH, the chrominance bandwidth is ±1.3 MHz.
05	4	SYNCDIS	**Sync pulse disable.** When HIGH, horizontal and vertical sync pulses on the COMPOSITE video output are suppressed (to blanking level). Color burst, active video, and the $\overline{\text{CSYNC}}$ output remain active. Set LOW for normal composite video operation.
05	3	BURDIS	**Color burst disable.** When HIGH, color burst is suppressed (blanking level). Set LOW for normal operation.
05	2	LUMDIS	**Luminance disable.** When HIGH, incoming Y values are forced to black level. Color burst, CHROMA, and sync are not affected. Set LOW for normal operation.
05	1	CHRDIS	**Chrominance disable.** When HIGH, incoming color components C_B and C_R are suppressed, enabling monochrome operation. Output color burst is not affected. Set LOW for normal color operation.
05	0	PEDEN	**Pedestal enable.** When LOW, black and blanking are the same level for ALL lines. When HIGH, a 7.5 IRE pedestal is inserted into the output video for NTSC and PAL-M lines 23-262 and 286-525 only. Chrominance and luminance gain factors are adjusted to keep video levels within range. PEDEN is valid for NTSC and PAL-M only and should be LOW for all other formats.

Field Data Register (06)

7	6	5	4	3	2	1	0
Reserved		FIELD			Reserved		

Reg	Bit	Name	Description
06	7–6	Reserved	Program LOW.
06	5–3	FIELD	**Field ID (Read only).** A value of 000 corresponds to field 1 and 111 corresponds to field 8.
06	2–0	Reserved	Program LOW.

Preliminary Information

Control Register Definitions (continued)

Reserved Registers (07–0D)

7	6	5	4	3	2	1	0
Reserved							

Reg	Bit	Name	Description
07–0D	7–0	Reserved	Program LOW.

General Purpose Port Register (0E)

7	6	5	4	3	2	1	0
PORT7	PORT6	PORT5	PORT4	PORT3	PORT2	BURSTF	CSYNC

Reg	Bit	Name	Description
0E	7–6	PORT7–6	**General purpose Inputs.** When in serial control mode, these register read-only bits indicate the state present on data port pins D_7 and D_6.
0E	5–2	PORT5–2	**General purpose Outputs.** When in serial control mode or when reading register 0E in parallel control mode, these register read/write bits drive data pins D_5–D_2 to the state contained in the respective register bits.
0E	1	BURSTF	**Burst Flag Output.** Produces Burst Flag on data pin D_1 when in serial control mode, or when reading register 0E.
0E	0	CSYNC	**Composite Sync Output.** Produces Composite Sync on data pin D_0 when in serial control mode, or when reading register 0E.

Control Register Definitions (continued)

General Control Register (0F)

7	6	5	4	3	2	1	0
PED21	$\overline{\text{JTAGEN}}$	VSEL	CBSEL	VBIEN	Reserved		

Reg	Bit	Name	Description
0F	7	PED21	**VBI Pedestal Enable.** When HIGH and FORMAT is 00 (NTSC) or 10 (PAL-M), pedestal is added to lines 21, 22, 283, 284, 285. When LOW, no pedestal is placed on these lines. PED21 is valid for NTSC and PAL-M only and should be LOW for all other formats.
0F	6	$\overline{\text{JTAGEN}}$	**JTAG Enable.** When LOW, the JTAG port is active. When HIGH, the JTAG port is disabled, and signals $\overline{\text{VSYNC}}$ (or T/$\overline{\text{B}}$), $\overline{\text{HSYNC}}$, SELC, and PDC (or CBSEL) appear on the JTAG pins.
0F	5	VSEL	**Vertical Sync Select.** When LOW, the TMC2490 outputs a traditional vertical sync on $\overline{\text{VSYNC}}$. When HIGH, the chip outputs odd/even field identification on the $\overline{\text{VSYNC}}$ pin, with 0 denoting an odd field.
0F	4	CBSEL	**CBSEL/PDC pin function.** When CBSEL = 0, the PDC signal is produced on the CBSEL/PCD pin. When CBSEL = 1, the CBSEL signal is produced on the CBSEL/PDC pin.
0F	3	VBIEN	**VBI Pixel Data Enable.** When VBIEN = 0, the vertical interval lines are blanked. When VBIEN = 1, Pixel data is encoded into the VBI lines. VBI blanking is available only in master mode.
0F	2–0	Reserved	Program LOW.

Reserved Registers (10–1F)

7	6	5	4	3	2	1	0
Reserved							

Reg	Bit	Name	Description
10–1F	7–0	Reserved	May be left unprogrammed

Control Register Definitions (continued)

Closed-Caption Insertion (20)

20	7–0	CCD1	**First Byte of CC Data.** Bit 0 is the LSB. The MSB will be overwritten by an ODD Parity bit if CCPAR is HIGH.

Closed-Caption Insertion (21)

7	6	5	4	3	2	1	0
CCD2							

Reg	Bit	Name	Description
21	7–0	CCD2	**Second Byte of CC Data.** Bit 0 is the LSB. The MSB will be overwritten by an ODD Parity bit if CCPAR is HIGH.

Closed-Caption Insertion (22)

7	6	5	4	3	2	1	0
CCON	CCRTS	CCPAR	CCFLD	CCLINE			

Reg	Bit	Name	Description
22	7	CCON	**Enable CC Data Packet.** Command the CC data generator to send either CC data or a NULL byte whenever the specified line is transmitted.
22	6	CCRTS	**Request To Send Data.** This bit is set HIGH by the user when bytes 20 and 21 have been loaded with the next two bytes to be sent. When the encoder reaches the falling edge of the HSYNC preceding the line specified in bits 4-0 of this register, data will be transferred from registers 20 and 21, and RTS will be reset LOW. A new pair of bytes may then be loaded into registers 20 and 21. If CCON = 1 and CCRTS = 0 when the CC line is to be sent, NULL bytes will be sent.
22	5	CCPAR	**Auto Parity Generation.** When set HIGH, the encoder replaces the MSB of bytes 20 and 21 with a calculated ODD parity. When set LOW, the CC processor transmits the 16 bits exactly as loaded into registers 20 and 21.
22	4	CCFLD	**CC Field Select.** When LOW, CC data is transmitted on the selected line of ODD fields. When HIGH, it is sent on EVEN fields.
22	3–0	CCLINE	**CC Line Select.** Defines (with an offset) the line on which CC data are transmitted.

General Purpose Port

The TMC2490 provides a general purpose I/O port for system utility functions. Input, output, and sync functions are implemented. Register 0E is the General Purpose Register.

Full functionality is provided when the encoder is in Serial control mode ($\overline{SER}$ = LOW). Most of the functions are available in parallel interface mode ($\overline{SER}$ = HIGH).

General Purpose Input (serial mode only)

Bits 7 and 6 of Register 0E are general purpose inputs. When the encoder is in serial control mode, data bits D_7 and D_6 are mirrored to these register locations. When Register 0E is read, the states of bits 7 and 6 reflect the TTL logic levels present on D_7 and D_6, respectively, at the time of read command execution. Writing to these bits has no effect.

This function is not available when the encoder is in parallel control mode.

General Purpose Output

Register 0E read/write bits 5-2 are connected to pins D_{5-2}, respectively, when the encoder is in serial control mode. The output pins continually reflects the values most recently written into register 0E (1 = HIGH, 0 = LOW). Note that these pins are always driven outputs when the encoder is in serial control mode.

When register 0E is read, these pins report the values previously stored in the corresponding register bits, i.e., it acts as a read/write register. When the encoder is in parallel control mode, this reading produces the output bit values on the corresponding data pins, just as in the serial control mode. However, the values are only present when reading register 0E. The controller can command a continuous read on this register to produce continuous outputs from these pins.

Burst Flag and Composite Sync (output/read-only)

Register 0E bit 1 is associated with the encoder burst flag. It is a 1 (HIGH) from just before the start of the color burst to just after the end of the burst. It is a 0 (LOW) at all other times.

Register 0E bit 0 outputs the encoder composite sync status. It is a 0 (LOW) during horizontal and vertical sync tips. It is a 1 (HIGH) at all other times.

These register bits may be read at any time over either the serial or parallel control port. As they are dynamic, their states will change as appropriate during a parallel port read. In fact, if the parallel control port is commanded to read register 0E continually, the pins associated with these bits behave as burst flag and composite sync timing outputs.

In serial control mode, these same data output pins (D_{1-0}) always act as a burst flag and composite sync TTL outputs, the conditions of the serial control notwithstanding. The states of the flags may be read over the serial port, but due to the low frequency of the serial interface, it may be difficult to get meaningful information.

Pixel Interface

The TMC2490 interfaces with an 8-bit 13.5 Mpps (27 MHz) video datastream. It will automatically synchronize with embedded Timing Reference Signals, per CCIR-656. It also includes a master sync generator on-chip, which may produce outputs.

CCIR-656 Mode

When operating in CCIR-656 Mode (MASTER = 0), the TMC2490 identifies the SAV and EAV 4-byte codewords embedded in the video datastream and, from them, derives all timing. Both SAV and EAV are required.

When $\overline{JTAGEN}$ = 0, the JTAG port is operational. When $\overline{JTAGEN}$ = 1, SYNC signals are output and JTAG is not available.

MASTER Mode

When in MASTER Mode (MASTER = 1), and JTAGEN = 1, the Encoder produces its own timing, and provides $\overline{HSYNC}$, $\overline{VSYNC}$ (or B/$\overline{T}$), SELC, and PDC (or $\overline{CBSEL}$) to the Pixel Data Source.

JTAG is not available.

SELC Output

The SELC output toggles at 13.5 Msps (1/2 the pixel rate), providing a phase reference for the multiplexed luma/chroma CCIR-656 format datastream. It is HIGH during the rising edge of the clock intended to load chroma data. This is useful when interfacing with a 16-bit data source, and can drive a Y/C multiplexer.

CBSEL Output

The CBSEL output identifies the CB element of the C_B-Y-C_R-Y CCIR-656 data sequence. It is HIGH during the rising edge of the clock intended to load C_B data. This can prevent unintentionally swapping the C_B and C_R color components when operating in MASTER mode and reading data from a framestore.

PDC Output

The PDC output is a blanking signal, indicating when the Encoder expected to receive pixel data. It goes HIGH four clocks before the first pixel is required, and goes LOW four clocks before the last pixel is accepted to accommodate pipeline delays in the video data source.

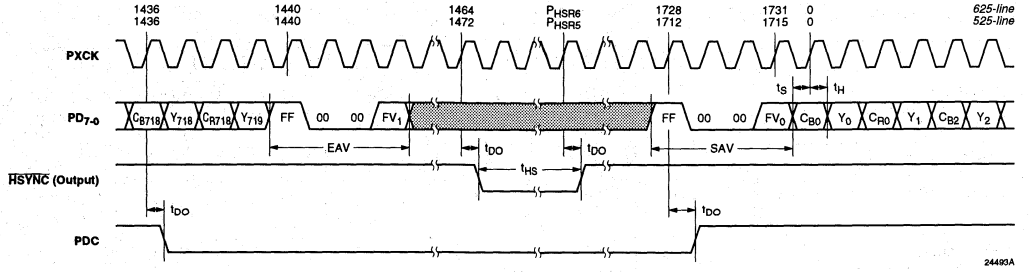


Figure 2. CCIR-656 Horizontal Interval Timing Detail

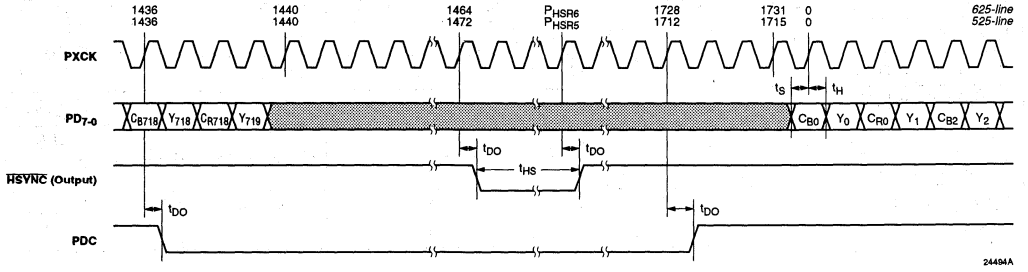


Figure 3. Master Mode Horizontal Interval Timing Detail

SET TOP BOX

Horizontal and Vertical Timing

Horizontal and vertical video timing in the TMC2490 is pre-programmed for line-locked systems with a 2x pixel clock of 27.0 MHz.

Table 3 and Table 4 show timing parameters for NTSC and PAL standards and the resulting TMC2490 analog output timing. The user provides exactly 720 pixels of active video per line. In master mode, the TMC2490 precisely controls the duration and activity of every segment of the horizontal line and vertical field group. In external sync slave mode, it holds the end-of-line blank state (e.g. front porch for active video lines) until it receives the next horizontal sync signal. In CCIR-656 slave mode, it likewise holds each end-of-line blank state until it receives the next end of active video (EAV) signal embedded in the incoming data stream. (See timing diagrams.)

The vertical field group comprises several different line types based upon the Horizontal line time.

H = (2 x SL) + (2 x SH) [Vertical sync pulses]
= (2 x EL) + (2 x EH) [Equalization pulses]

SMPTE 170M NTSC and Report 624 PAL video standards call for specific rise and fall times on critical portions of the video waveform. The chip does this automatically, requiring no user intervention. The TMC2490 digitally defines slopes compatible with SMPTE 170M NTSC or CCIR Report 624 PAL on all vital edges:

1. Sync leading and trailing edges.
2. Burst envelope.
3. Active video leading and trailing edges.
4. All vertical interval equalization pulse and sync edges.

Table 3. Horizontal Timing Standards and Actual Values for 60 fps Video Standards (µs)

Parameter		NTSC (SMPTE 170M)			PAL-M (CCIR 624)			TMC2490
		Min	Nom	Max	Min	Nom	Max	
Front porch	FP	1.4	1.5	1.6	1.27		2.22	1.53
Horiz. Sync	SY	4.6	4.7	4.8	4.6	4.7	4.8	4.74
Breezeway	BR	0.508	0.608	0.809	0.9	1.1	1.3	0.59 (NTSC) 1.04 (PAL-M)
Color Burst	BU	2.235	2.514	2.794	2.237	2.517	2.797	2.31
Color Back porch	CBP	0.998	1.378	1.857	0.503		2.363	1.65 (NTSC) 0.89 (PAL-M)
Blanking	BL	10.5	10.7	11.0	10.7	10.9	11.1	10.8
Active Video	VA	52.56	52.86	53.06	52.46	52.66	52.86	52.633
Line Time	H		63.556			63.556		63.557
Equalization HIGH	EH		29.5			29.5		29.47
Equalization LOW	EL		2.3			2.3		2.31
Sync HIGH	SH		4.7			4.7		4.67
Sync LOW	SL		27.1			27.1		27.13
Sync rise and fall times			140±20ns			<250 ns		135ns

Table 4. Horizontal Timing Standards and Actual Values for 50 fps Video Standards (µs)

Parameter		PAL-B,G,H,I (CCIR 624)			PAL-N (CCIR 624)			TMC2490
		Min	Nom	Max	Min	Nom	Max	
Front porch	FP	1.2	1.5	1.8	1.2	1.5	1.8	1.57
Horiz. Sync	SY	4.5	4.7	4.9	4.5	4.7	4.9	4.74
Breezeway	BR	0.6	0.9	1.2	0.6	0.9	1.2	0.89
Color Burst	BU	2.030	2.255	2.481	2.233	2.513	2.792	2.3
Color Back porch	CBP		2.654			2.387		2.3
Blanking	BL	11.7	12.0	12.3	11.7	12.0	12.3	1.8
Active Video	VA	51.7	52.0	52.3	51.7	52.0	52.3	52.2
Line Time	H		64			64		64.0
Equalization HIGH	EH		29.65			29.65		29.63
Equalization LOW	EL		2.35			2.35		2.37
Sync HIGH	SH		4.7			4.7		4.67
Sync LOW	SL		27.3			27.3		27.3
Sync rise and fall times			250±50 ns			200±100 ns		250

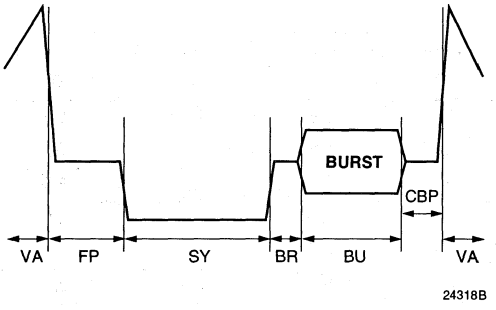


Figure 4. Horizontal Blanking Interval Timing

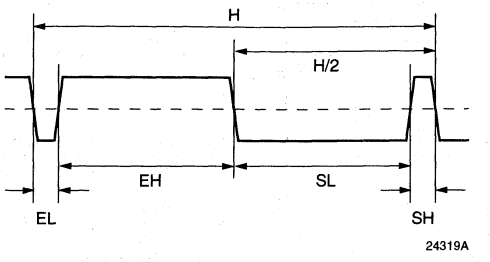


Figure 5. Vertical Sync and Equalization Pulse Detail

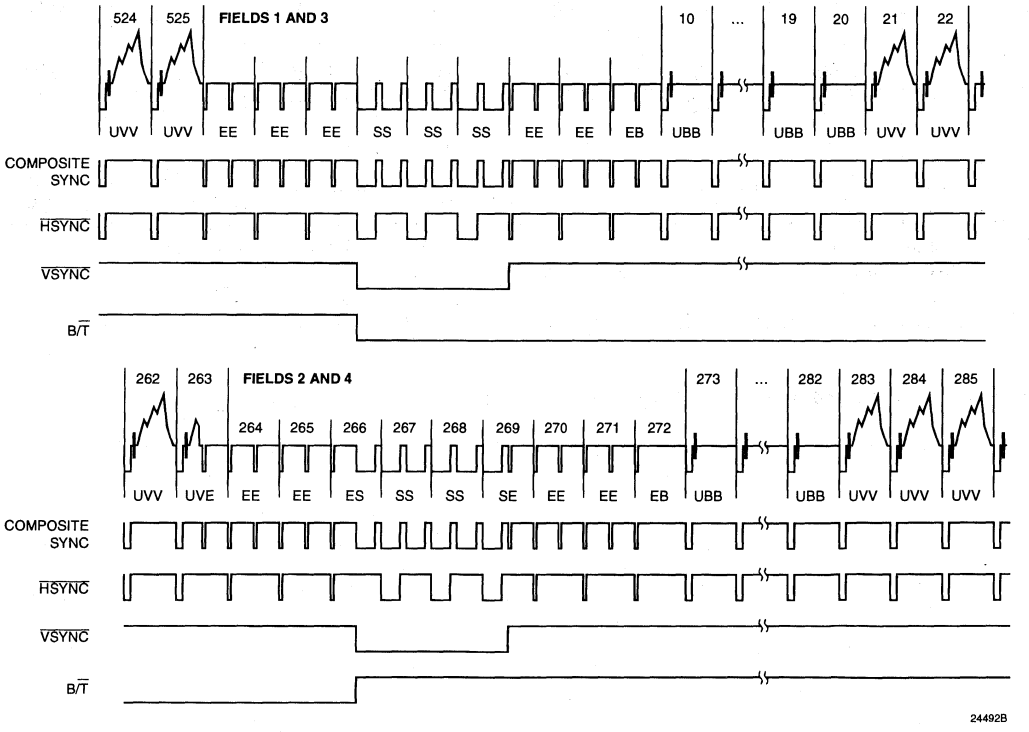


Figure 6. NTSC Vertical Interval

SET TOP BOX

Table 6. NTSC Field/Line Sequence and Identification

Field 1, FID = 00		Field 2, FID = 01		Field 3, FID = 10		Field 4, FID = 11	
Line	ID	Line	ID	Line	ID	Line	ID
1	EE	264	EE	1	EE	264	EE
2	EE	265	EE	2	EE	265	EE
3	EE	266	ES	3	EE	266	ES
4	SS	267	SS	4	SS	267	SS
5	SS	268	SS	5	SS	268	SS
6	SS	269	SE	6	SS	269	SE
7	EE	270	EE	7	EE	270	EE
8	EE	271	EE	8	EE	271	EE
9	EE	272	EB	9	EE	272	EB
10	UBB	273	UBB	10	UBB	273	UBB
...	...	...	...	...	...	...	...
20	UBB	282	UBB	20	UBB	282	UBB
21	UVV	283	UVV	10	UVV	273	UVV
...	...	...	...	...	...	...	...
262	UVV	524	UVV	262	UVV	524	UVV
263	UVE	525	UVV	263	UVE	525	UVV

EE Equalization pulse
SE Half-line vertical sync pulse, half-line equalization pulse
SS Vertical sync pulse
ES Half-line equalization pulse, half-line vertical sync pulse
EB Equalization broad pulse
UBB Black and Burst[1]
UVV Active video
UVE Half-line video, half-line equalization pulse

Note:
1. VBB lines are changed to UVV (Active Video) when VBIEN = 1.

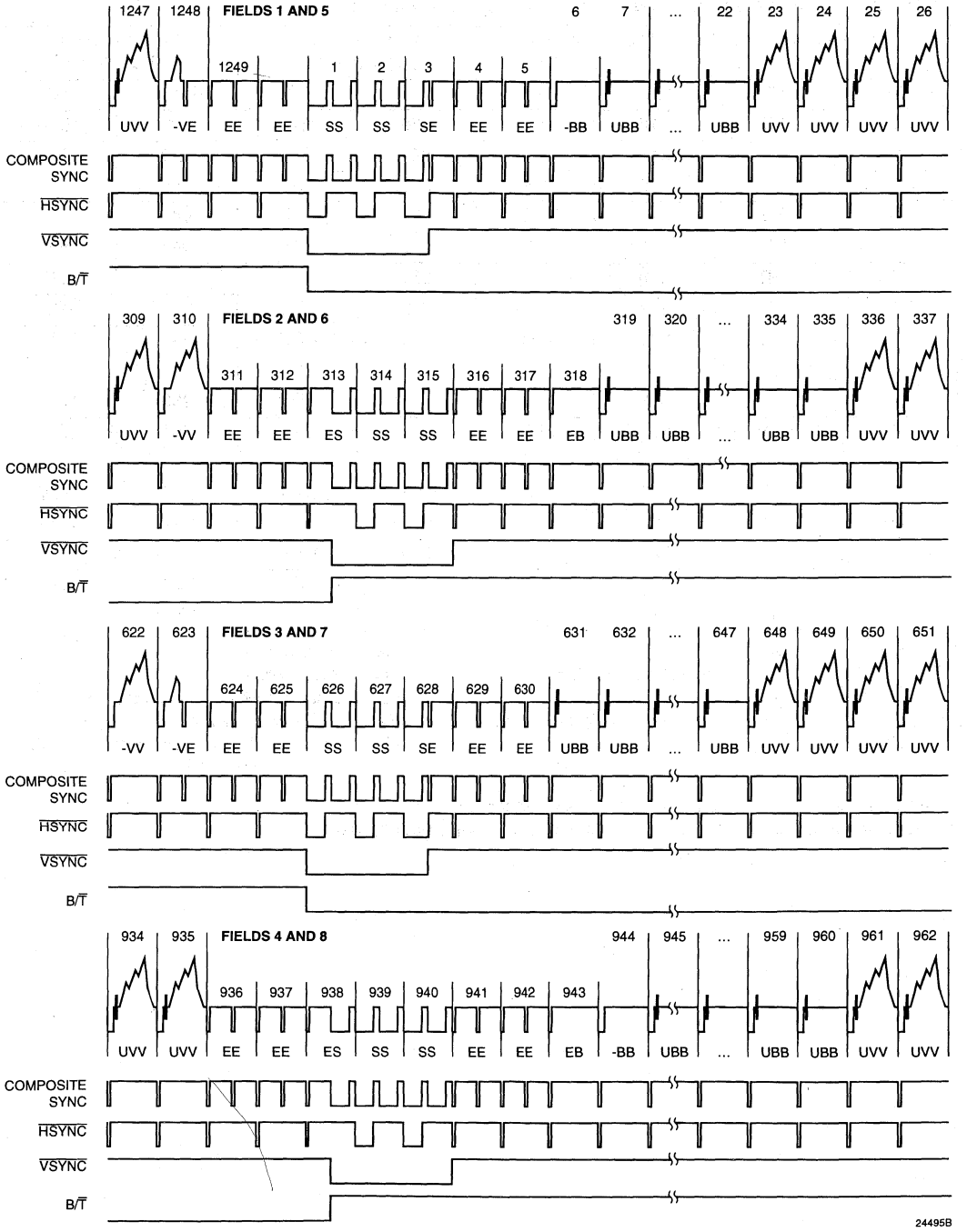


Figure 7. PAL-B,G,H,I,N Vertical Interval

Table 7. PAL-B,G,H,I,N Field/Line Sequence and Identification

Fields 1 and 5 FID = 000, 100		Fields 2 and 6 FID = 001, 101		Fields 3 and 7 FID = 010, 110		Fields 4 and 8 FID = 011, 111	
Line	**ID**	**Line**	**ID**	**Line**	**ID**	**Line**	**ID**
1	SS	313	ES	626	SS	938	ES
2	SS	314	SS	627	SS	939	SS
3	SE	315	SS	628	SE	940	SS
4	EE	316	EE	629	EE	941	EE
5	EE	317	EE	630	EE	942	EE
6	-BB	318	EV	631	UBB	943	EB
7	UBB	319	UBB	632	UBB	944	-BB
8	UBB	320	UBB	633	UBB	945	UBB
...	...	...	...	...	...	...	...
22	UBB	335	UBB	647	UBB	960	UBB
23	UVV	336	UVV	648	UVV	961	UVV
...	...	...	...	...	...	...	...
308	UVV	621	UVV	933	UVV	1246	UVV
309	UVV	622	-VV	934	UVV	1247	UVV
310	-VV	623	-VE	935	UVV	1248	-VE
311	EE	624	EE	936	EE	1249	EE
312	EE	625	EE	937	EE	1250	EE

EE	Equalization pulse	UBB	Black and Burst[1]
SE	Half-line vertical sync pulse, half-line equalization pulse	UVV	Active video
SS	Vertical sync pulse	-BB	Blank line with color burst suppression[2]
ES	Half-line equalization pulse, half-line vertical sync pulse	-VV	Active video with color burst suppressed
EB	Equalization broad pulse	-VE	Half-line video, half-line equalization pulse, color burst suppressed

Notes:

1. VBB lines are changed to UVV (Active Video) when VBIEN = 1.
2. -BB lines are changed to -VV (Active Video, Burst Suppressed) when VBIEN = 1.

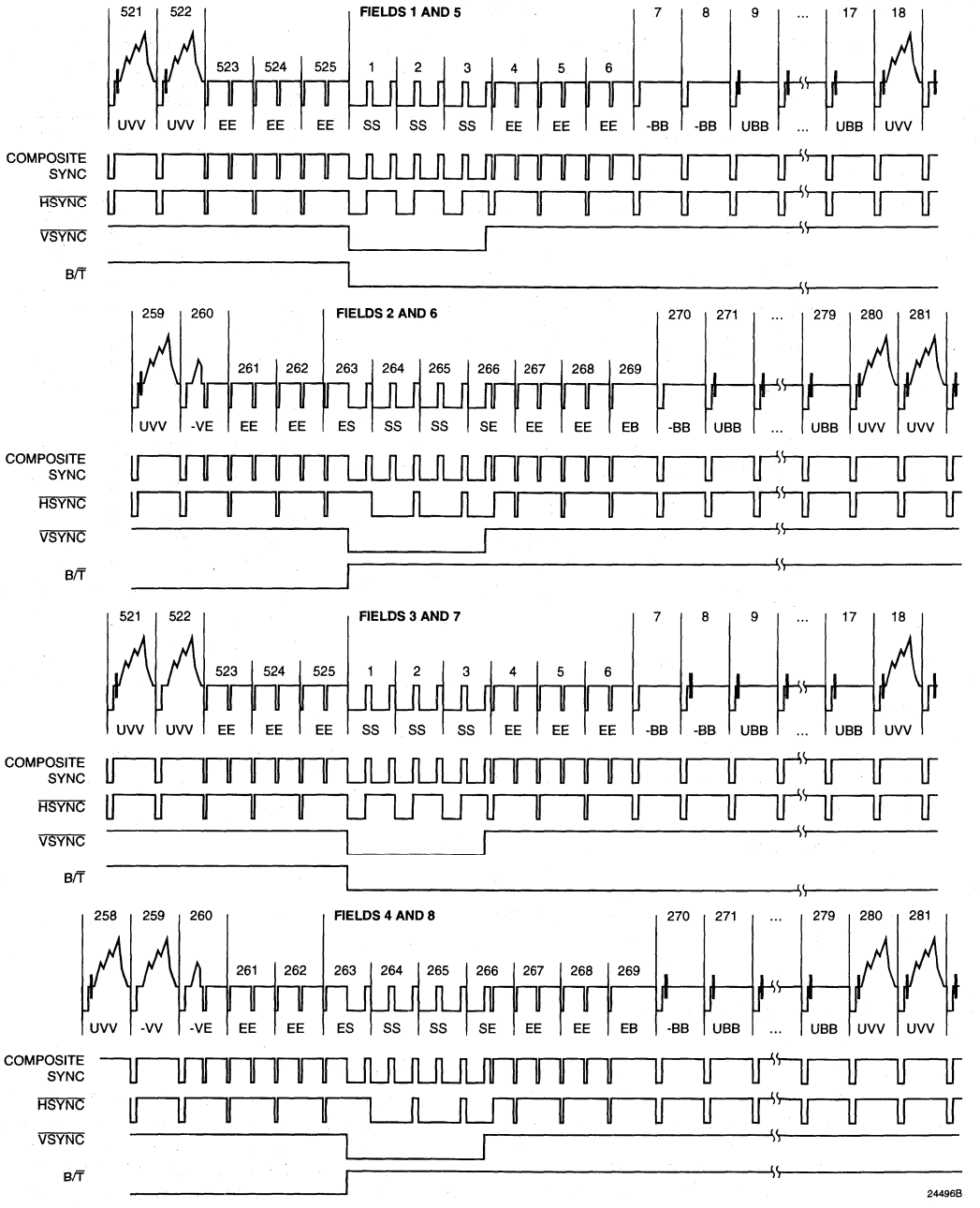


Figure 8. PAL-M Vertical Interval

Table 8. PAL-M Field/Line Sequence and Identification

Field 1 and 5 FID = 000, 100		Field 2 and 6 FID = 001, 101		Field 3 and 7 FID = 010, 110		Field 4 and 8 FID = 011, 111	
Line	ID	Line	ID	Line	ID	Line	ID
1	SS	263	ES	1	SS	263	ES
2	SS	264	SS	2	SS	264	SS
3	SS	265	SS	3	SS	265	SS
4	EE	266	SE	4	EE	266	SE
5	EE	267	EE	5	EE	267	EE
6	EE	268	EE	6	EE	268	EE
7	-BB	269	EB	7	-BB	269	EB
8	-BB	270	-BB	8	UBB	270	-BB
9	UBB	271	UBB	9	UBB	271	UBB
...	...	...	...	...	...	...	...
17	UBB	279	UBB	17	UBB	279	UBB
18	UVV	280	UVV	18	UVV	280	UVV
...	...	...	...	...	...	...	...
258	UVV	521	UVV	258	UVV	521	UVV
259	UVV	522	-VV	259	-VV	522	UVV
260	-VE	523	EE	260	-VE	523	EE
261	EE	524	EE	261	EE	524	EE
262	EE	525	EE	262	EE	525	EE

EE	Equalization pulse	UBB	Black and Burst[1]
SE	Half-line vertical sync pulse, half-line equalization pulse	UVV	Active video
SS	Vertical sync pulse	-BB	Blank line with color burst suppression[2]
ES	Half-line equalization pulse, half-line vertical sync pulse	-VV	Active video with color burst suppressed
EB	Equalization broad pulse	UVV	half-line black, half-line video
-VE	Half-line video, half-line equalization pulse, color burst suppressed		

Notes:
1. VBB lines are changed to UVV (Active Video) when VBIEN = 1
2. -BB lines are changed to -VV (Active Video, Burst Suppressed) when VBIEN = 1

Preliminary Information

Subcarrier Generation and Synchronization

The color subcarrier is produced by an internal digital frequency synthesizer. The subcarrier synthesizer gets its frequency and phase values preprogrammed into the TMC2490.

In Master Mode, the subcarrier is internally synchronized on field 1 of the eight-field sequence to establish and maintain a specific relationship between the leading edge of horizontal sync and color burst phase (SCH). Proper subcarrier phase is maintained through the entire eight field set, including the 25 Hz offset in PAL-N/B/I systems. The subcarrier is reset to the phase values found in Table 9.

SCH Phase Control

SCH refers to the timing relationship between the 50% point of the leading edge of horizontal sync and the first positive or negative zero-crossing of the color burst subcarrier reference. In PAL, SCH is defined for line 1 of field 1, but since there is no color burst on line 1, SCH is usually measured at line 7 of field 1. The need to specify SCH relative to a particular line in PAL is due to the 25 Hz offset of PAL subcarrier frequency. Since NTSC has no such 25 Hz offset, SCH applies to all lines.

Table 9. Subcarrier and Color Burst Reset Values

	NTSC	PAL-M	PAL-B,G,H,I,N
Digital field:	1	1	1
Line number:	4	4	1
Subcarrier phase reset value:	180°	0°	0°
Resultant color burst phase:	0°	+135°	+135°

Note:

1. Line numbering is in accordance with Figure 6, Figure 7, and Figure 8. Subcarrier and color burst phase are relative to the horizontal reference of the line specified above.

Table 10. Standard Subcarrier Parameters

Standard	Horizontal Frequency (KHz)	Subcarrier Frequency (MHz)
NTSC	15.734266	3.579545455
PAL B,G,H,I	15.625000	4.43361875
PAL-M	15.734266	3.57561189
PAL-N	15.625000	3.58205625

Luminance Processing

During horizontal and vertical blanking, the luma processor generates blanking levels and properly timed and shaped sync and equalization pulses. During active video, it captures and rescales the incoming Y components and adds the results to the blank level to complete a proper monochrome television waveform, which is then upsampled to drive the luma D/A and the composite adder.

For NTSC-EIA (5:2 white:sync, no black pedestal), the overall luma input-to-output equation for 0<Y<255 is:

luma out (IRE, relative to blank) = (Y - 16) * 100/219

For NTSC and PAL-M (5:2, with 7.5 IRE pedestal), the equation becomes:

luma out (IRE, relative to blank) = (Y - 16) * 92.5/219 + 7.5

For all 625-line PAL standards (7:3, no pedestal), the equation becomes:

luma out (mV, relative to blank) = (Y-16) * 700/219

Since Y=0 and Y=255 are reserved values in CCIR-601, results in the luma D/A outputting black, i.e., 0mV or 0 IRE without pedestal, 7.5 IRE with pedestal.

Table 11. Luminance Input Codes

PD_{7-0} Input		Luma Level (CCIR-601)	NTSC, PAL-M Luma Level (IRE)		PAL-B,G,H,I,N Luma Level (mV)
Dec	Hex		PEDEN = 0	PEDEN = 1	
255	FF	Reserved	0	7.5	0
254	FE		108.7	108	761
235	EB	100% white	100	100	700
16	10	Black	0	7.5	0
1	01		-6.9	1.2	-48
0	00	Reserved	0	7.5	0

Table 12. D/A Converter and Analog Levels

	NTSC, PAL-M		NTSC w/o Setup		PAL-B,G,H,I,N	
Video Level	D/A	IRE	D/A	IRE	D/A	mV
Maximum Output	511	134.8	511	138.4	511	964
100% white	410	100	410	100	400	700
Black	142	7.5	120	0	128	0
Blank	120	0	120	0	128	0
Sync	4	-40	4	-40	6	-300
White-to-blank	290	100	290	100	280	700
White-to- sync	406	140	406	140	406	1000
Color burst p-p	116	40	116	40	122	300

Filtering Within the TMC2490

The TMC2490 incorporates internal digital filters to establish appropriate bandwidths and simplify external analog reconstruction filter designs.

The chroma portion of the incoming digital video is band-limited to reduce edge effect and other distortions of the image compression process. Chrominance bandwidth is selected by CHRBW. When LOW, the chrominance passband attenuation is <3 dB within ±650 kHz from f_{SC}. The stopband rejection is >26 dB outside f_{SC} ±2 MHz. When HIGH, the chrominance passband attenuation is <3 dB within ±1.3 MHz from f_{SC}. The stopband rejection is >33 dB outside f_{SC} ±4 MHz.

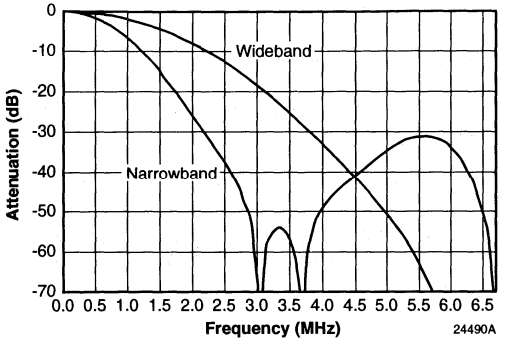


Figure 9. Color-Difference Low-Pass Filter Response

The Chroma Modulator output and the luminance data are digitally filtered with sharp-cutoff low-pass interpolation filters. These filters ensure that aliased subcarrier, chrominance, and luminance frequencies are sufficiently suppressed above the video base-band and below the pixel frequency range ($f_S/4$ to 3 x $f_S/4$, where f_S is the PXCK frequency).

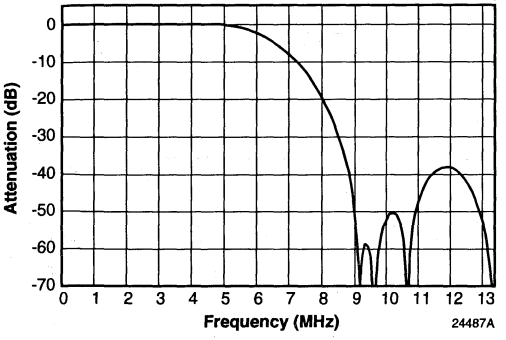


Figure 10. Chrominance and Luminance Interpolation Filter - Full Spectrum Response

Virtually all digital-to-analog converters have a response with high frequency roll-off as a result of the zero-order hold characteristic of classic D/A converters. This response is commonly referred to as a sin(x)/x response. The sin(x)/x vs. sampling frequency is shown in Figure 12.

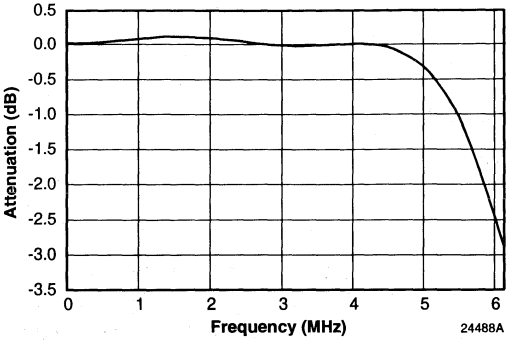


Figure 11. Chrominance and Luminance Interpolation Filter - Passband Detail

The TMC2490's digital interpolation filters convert the data stream to a sample rate of twice the pixel rate. This results in much less high frequency sin(x)/x rolloff and the output spectrum between $f_S/4$ and 3 x $f_S/4$ contains very little energy. Since there is so little signal energy in this frequency band, the demands placed on the output reconstruction filter are greatly reduced. The output filter needs to be flat to $f_S/4$ and have good rejection at 3 x $f_S/4$. The relaxed requirements greatly simplify the design of a filter with good phase response and low group delay distortion. A small amount of peaking may be added to compensate residual sin(x)/x rolloff.

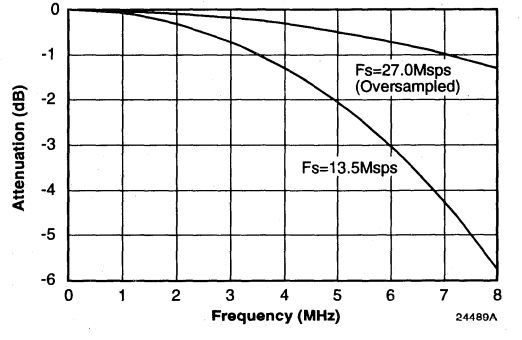


Figure 12. Sin(x)/x Response

Closed Caption Insertion

The TMC2490 includes a flexible closed caption processor. It may be programmed to insert a closed caption signal on any line within a range of 16 lines on ODD and/or EVEN fields.

Closed Caption insertion overrides all other configurations of the encoder: if it is specified on an active video line, it takes precedence over the video data and removes NTSC setup if setup has been programmed for the active video lines.

Closed Caption Control

Closed caption is turned on by setting CCON HIGH. Whenever the encoder begins producing a line specified by CCFLD and CCLINE, it will insert a closed caption line in its place. If CCRTS is HIGH, the data contained in CCDx will be sent. IF CCRTS is LOW, Null Bytes (hex 00 with ODD parity) will be sent.

Line Selection

The line to contain CC data is selected by a combination of the CCFLD bit and the CCLINE bits. CCLINE is added to the offset shown in Table 13 to specify the line.

Table 13. Closed Caption Line Selection

Standard	Offset	Field	Lines
525	12	ODD	12-27
	274	EVEN	274-289
625	9	ODD	9-24
	321	EVEN	321-336

Parity Generation

Standard Closed-Caption signals employ ODD parity, which may be automatically generated by setting CCPAR HIGH. Alternatively, parity may be generated externally as part of the bytes to be transmitted, and, with CCPAR LOW, the entire 16 bits loaded into the CCDx registers will be sent unchanged.

Operating Sequence

A typical operational sequence for closed-caption insertion on Line 21 is:

1. Read Register 22 and check that bit 6 is LOW, indicating that the CCDx registers are ready to accept data.
2. If ready, write two bytes of CC data into registers 20 and 21.
3. Write into register 22 the proper combination of CCFLD and CCLINE. CCPAR may be written as desired. Set CCRTS HIGH.
4. The CC data is transmitted during the specified line.

As soon as CCDx s transferred into the CC processor (and CCRTS goes LOW), new data may be loaded into registers 20 and 21. This allows the user to transmit CC data on several consecutive lines by loading data for line n+1 while data is being sent on line n.

Registers 20-21 autoincrement when read or written. Register 22 does not. The microcontroller can repeatedly read register 22 until CCRTS is found to be low, then address register 20 and write three autoincremented bytes to set up for the next CC line.

Parallel Microprocessor Interface

The parallel microprocessor interface, active when $\overline{SER}$ is HIGH, employs an 11-line interface, with an 8-bit data bus and one address bit: two addresses are required for device programming and pointer-register management. Address bit 0 selects between reading/writing the register addresses and reading/writing register data. When writing, the address is presented along with a LOW on the R/$\overline{W}$ pin during the falling edge of $\overline{CS}$. Eight bits of data are presented on D_{7-0} during the subsequent rising edge of $\overline{CS}$.

In read mode, the address is accompanied by a HIGH on the R/$\overline{W}$ pin during a falling edge of $\overline{CS}$. The data output pins go to a low-impedance state t_{DOZ} ns after $\overline{CS}$ falls. Valid data is present on D_{7-0} t_{DOM} after the falling edge of $\overline{CS}$.

Table 14. Parallel Port Control

ADR	R/$\overline{W}$	Action
1	0	Load D_{7-0} into Control Register pointer.
1	1	Read Control Register pointer on D_{7-0}.
0	0	Write D_{7-0} to addressed Control Register.
0	1	Read addressed Control Register on D_{7-0}.

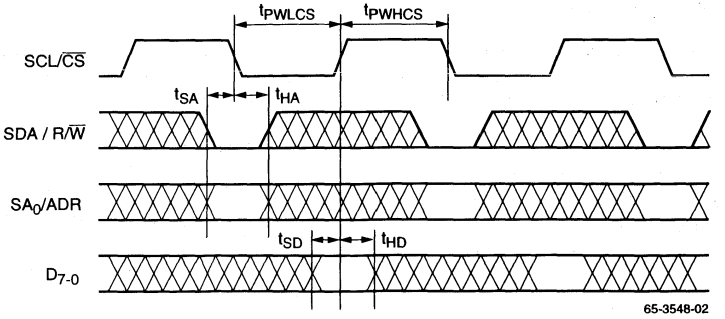


Figure 13. Microprocessor Parallel Port - Write Timing

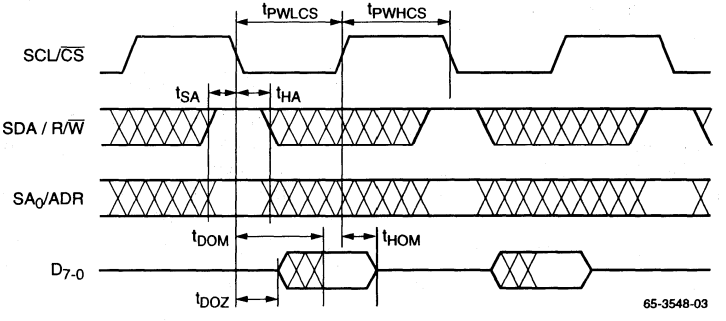


Figure 14. Microprocessor Parallel Port - Read Timing

Serial Control Port (R-Bus)

In addition to the 11-wire parallel port, a 2-wire serial control interface is also provided, and active when $\overline{SER}$ is LOW. Either port alone can control the entire chip. Up to four TMC2490 devices may be connected to the 2-wire serial interface with each device having a unique address.

The 2-wire interface comprises a clock (SCL/$\overline{CS}$) and a bi-directional data (SDA/R/$\overline{W}$) pin. The TMC2490 acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL/$\overline{CS}$ and SDA/R/$\overline{W}$ are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA/R/W\ line must be stable for the duration of the positive-going SCL/$\overline{CS}$ pulse. Data on SDA/R/$\overline{W}$ must change only when SCL/$\overline{CS}$ is LOW. If SDA/R/$\overline{W}$ changes state while SCL/$\overline{CS}$ is HIGH, the serial interface interprets that action as a start or stop sequence.

There are five components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL/$\overline{CS}$ and SDA/R/$\overline{W}$ are HIGH) communications are initiated by sending a start signal. The start signal is a HIGH-to-LOW transition on SDA/R/$\overline{W}$ while SCL/$\overline{CS}$ is HIGH. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a seven bit slave address and a single R/W bit. As shown in Figure 16A, the R/W bit indicates the direction of data transfer, read from or write to the slave device. If the transmitted slave address marches the address of the device (set by the state of the SA_0/ADR and SA_1 input pins in Table 15.), the TMC2490 acknowledges by bringing SDA/R/$\overline{W}$ LOW on the 9th SCL/$\overline{CS}$ pulse. If the addresses do not match, the TMC2490 does not acknowledge.

Table 15. Serial Port Addresses

A_6	A_5	A_4	A_3	A_2	A_1 (SA_1)	A_0 (SA_0)
0	0	0	1	1	0	0
0	0	0	1	1	0	1
0	0	0	1	1	1	0
0	0	0	1	1	1	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the TMC2490 does not acknowledge the master device during a write sequence, the SDA/R/$\overline{W}$ remains HIGH so the master can generate a stop signal. If the master device does not acknowledge the TMC2490 during a read sequence, the TMC2490 interprets this as "end of data." The SDA/R/$\overline{W}$ remains HIGH so the master can generate a stop signal.

Writing data to specific control registers of the TMC2490 requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 22h. Any base address higher than 22h will not produce an ACKnowledge signal.

Data is read from the control registers of the TMC2490 in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/W bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the TMC2490, a stop signal must be sent. A stop signal comprises a LOW-to-HIGH transition of SDA/R/$\overline{W}$ while SCL/$\overline{CS}$ is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

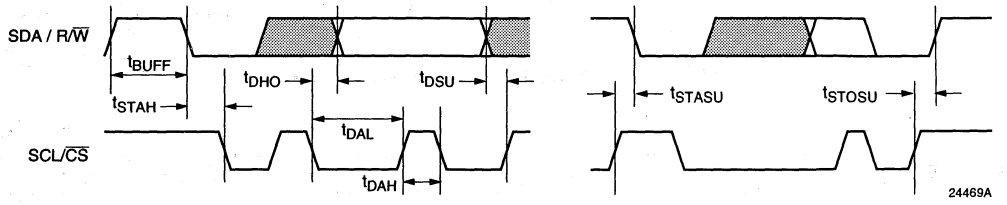


Figure 15. Serial Port Read/Write Timing

Serial Interface Read/Write Examples

Write to one control register

- Start signal
- Slave Address byte (R/W bit = LOW)
- Base Address byte
- Data byte to base address
- Stop signal

Write to four consecutive control registers

- Start signal
- Slave Address byte (R/W bit = LOW)
- Base Address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Read from one control register

- Start signal
- Slave Address byte (R/W bit = LOW)
- Base Address byte
- Stop signal
- Start signal
- Slave Address byte (R/W bit = HIGH)
- Data byte from base address
- Stop signal

Read from four consecutive control registers

- Start signal
- Slave Address byte (R/W bit = LOW)
- Base Address byte
- Stop signal
- Start signal
- Slave Address byte (R/W bit = HIGH)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

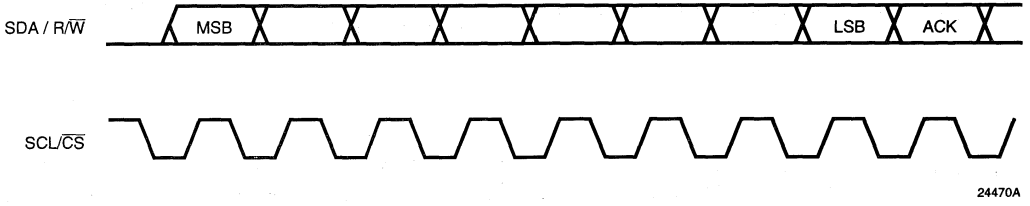


Figure 16. Serial Interface – Typical Byte Transfer

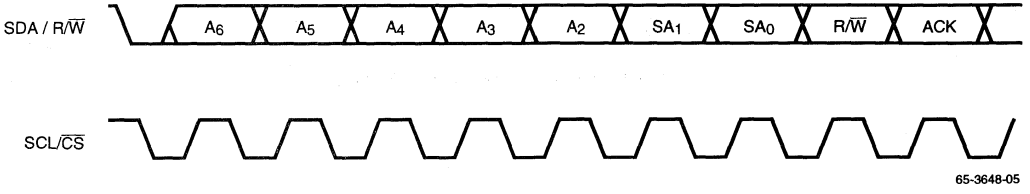


Figure 16A. Chip Address with Read/Write Bit

JTAG Test Interface

The JTAG test port accesses registers at every digital I/O pin except the JTAG test port pins.

Table 16 specifies the sequence of the test registers. The register number (Reg) indicates the order in which the register data is loaded and read (Reg 1 is loaded and read first, therefore it is at the end of the serial path). The scan path is 23 registers long.

The JTAG port is a 4-wire interface, following IEEE Std. 1149.1-1990 specifications. The Test Data Input (TDI) and Test Mode Select (TMS) inputs are referred to the rising edge of the Test ClocK (TCK) input. The Test Data Output (TDO) is referred to the falling edge of TCK.

The JTAG standard has been implemented into the TMC2490 without the UPDATE data register.

The CAPTURE Instruction Register is implemented with force value of 01 which allows SAMPLE or PRELOAD data to the data path.

The Instruction register contains two bits: IRM and IRL (TDI shift to IRM; IRM shift to IRL; IRL shift to TDO) - see Table 17.

There are 16 states in TAP and all are fully implemented.

In general, TMS is commanding the state machine and puts the system into JTAG states. The TMC2490 can be operated freely because there is no means to interrupt its function. There is NO output driver related to the JTAG data path.

While TMS determines the state, there are only a few events that may happen:

1. Capture DR. In this state, all the data at the pins will be LOADed into the data scan path only if IRM is not equal to IRL. If IRM = IRL, even though the state machine is at this state, NO ACTION will take place.

2. Shift DR. In this state, the data scan path is transferring data from high order bit to low order bits. It is always operational regardless of the contents of IRM and IRL.

3. Capture IR. While TMS captures IR state, the TMC2490 automatically loads 01 to the pre-instruction register (IRMp and IRLp respectively).

4. Shift IR. In this state, shift TDI to IRMp, IRMp to IRLp, and IRLp to TDO.

5. Update IR. In this state, TMC2490 LOAD contents of the Instruction register from the PRELOADED (or SHIFTED) IR to execution Instruction register (double buffered.)

The DATA SCAN PATH Register is a serial SHIFT, parallel LOAD shift register. While in Shift DR state, TMC2490 does SHIFT. While the IR (instruction register) is 01 or 10, and the TAP state is at Capture DR state, TMC2490 does LOAD.

For each input PIN (three-state pins included, but not the analog pins), the TMC2490 has a 2:1 multiplexer and register. One of the multiplexer inputs is the PAD and the other is the shifted data from the higher order scan path.

The JTAG test port is disabled when JTAGEN = 1.

Table 16. JTAG Sequence

Reg	Pin	Reg	Pin	Reg	Pin
1	$\overline{\text{RESET}}$	9	PD_1	17	D_6
2	PXCK	10	PD_0	18	D_5
3	PD_7	11	SA_1	19	D_4
4	PD_6	12	SA_0/ADR	20	D_3
5	PD_5	13	SDA/R/$\overline{W}$	21	D_2
6	PD_4	14	SCL/$\overline{CS}$	22	D_1
7	PD_3	15	$\overline{\text{SER}}$	23	D_0
8	PD_2	16	D_7		

Table 17. Function of IRM and IRL

IRM	IRL	Function
0	0	EXTEST, no effect while shift at DR, data keeps on shifting.
0	1	SAMPLE/PRELOAD At capture DR state, load all input pins parallel to data scan path.
1	0	Same as SAMPLE/PRELOAD
1	1	BYPASS TDI bypass to TDO

SET TOP BOX

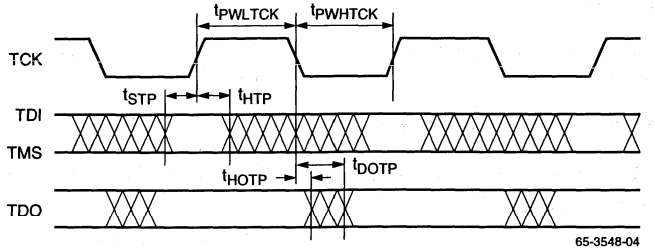


Figure 17. JTAG Test Port Timing

Equivalent Circuits

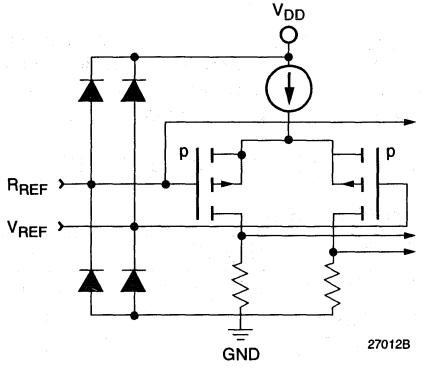


Figure 18. Equivalent Analog Input Circuit

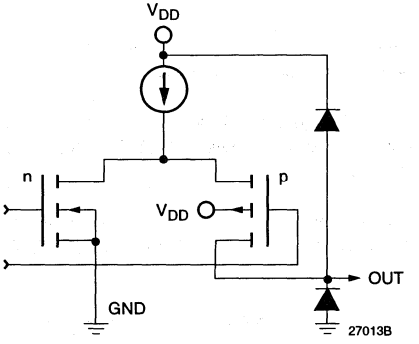


Figure 19. Equivalent Analog Output Circuit

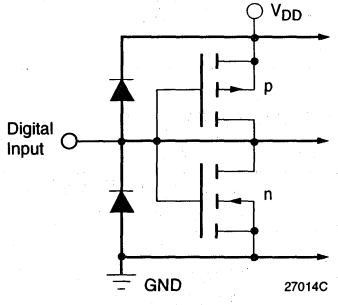


Figure 20. Equivalent Digital Input Circuit

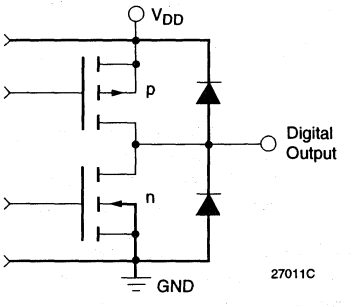


Figure 21. Equivalent Digital Output Circuit

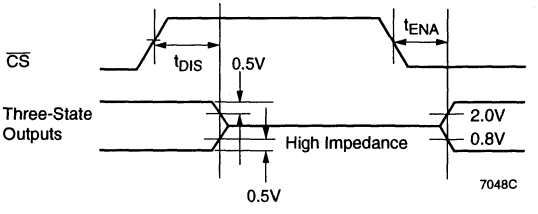


Figure 22. Threshold Levels for Three-State Measurements

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltage	-0.5		7.0	V
Digital Inputs				
Applied Voltage[2]	-0.5		V_{DD} + 0.5	V
Forced Current[3,4]	-20.0		20.0	mA
Output				
Applied Voltage[2]	-0.5		V_{DD} + 0.5	V
Forced Current[3,4]	-3.0		6.0	mA
Short Circuit Duration (single output in HIGH state to ground)			1	sec
Analog Short Circuit Duration (all outputs to ground)	Infinite			
Temperature				
Operating, Ambient	-20		110	°C
Junction			140	°C
Storage Temperature	-65		150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

SET TOP BOX

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH	TTL Compatible Inputs	2.0		V_{DD}	V
		CLK Input	2.4		V_{DD}	
		R-Bus Inputs	0.7V_{DD}			
V_{IL}	Input Voltage, Logic LOW	TTL Compatible Inputs	GND		0.8	V
		R-Bus Inputs			0.3V_{DD}	
V_{REF}	External Reference Voltage			1.235		V
I_{REF}	D/A Converter Reference Current	(I_{REF} = V_{REF}/R_{REF}), flowing out of the R_{REF} pin		1.57		mA
R_{REF}	External Reference Resistor	V_{REF} = NOM		787		Ω
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				2.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C
Pixel Interface						
f_{PXL}	Pixel Rate			13.5		Mpps
f_{PXCK}	Master Clock Rate	= 2X pixel rate		27.0		MHz

Operating Conditions (continued)

Parameter		Conditions	Min	Typ	Max	Units
t_{PWHPX}	PXCK pulse width, HIGH		10			ns
t_{PWLPX}	PXCK pulse width, LOW		15			ns
t_{SP}	PD_{7-0} Setup Time		15			ns
t_{HP}	PD_{7-0} Hold Time		0			ns
Parallel Microprocessor Interface						
t_{PWLCS}	$\overline{CS}$ Pulse Width, LOW		95			ns
t_{PWHCS}	$\overline{CS}$ Pulse Width, HIGH		3			pixels
t_{SA}	Address Setup Time		17			ns
t_{HA}	Address Hold Time		0			ns
t_{SD}	Data Setup Time (write)		17			ns
t_{HD}	Data Hold Time (write)		0			ns
t_{SR}	Reset Setup Time		15			ns
t_{HR}	Reset Hold Time		2			ns
Serial Microprocessor Interface						
t_{DAL}	SCL Pulse Width, LOW			1.3		µs
t_{DAH}	SCL Pulse Width, HIGH			0.6		µs
t_{STAH}	SDA Start Hold Time			0.6		µs
t_{STASU}	SCL to SDA Setup Time (Stop)			0.6		µs
t_{STOSU}	SCL to SDA Setup Time (Start)			0.6		µs
t_{BUFF}	SDA Stop Hold Time Setup			1.3		µs
t_{DSU}	SDA to SCL Data Setup Time			300		ns
t_{DHO}	SDA to SCL Data Hold Time			300		ns
JTAG Interface						
f_{TCK}	Test Clock (TCK) Rate				10	MHz
t_{PWLTCK}	TCK Pulse Width, LOW		10			ns
t_{PWHTCK}	TCK Pulse Width, HIGH		10			ns
t_{STP}	Test Port Setup Time, TDI, TMS		15			ns
t_{HTP}	Test Port Hold Time, TDI, TMS		0			ns

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Current, Unloaded[2]	V_{DD} = Max, f_{PXCK} = 27MHz			120	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max			50	mA
V_{RO}	Voltage Reference Output		1.136	1.235	1.334	V
I_{BR}	Reference Bias		-100		100	µA
Z_{RO}	V_{REF} Output Impedance			1000		Ω
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V			±10	µA
I_{OS}	Short-Circuit Current		-50		-10	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max			0.4	V
C_I	Digital Input Capacitance			4	10	pF
C_I	Digital Output Capacitance			10		pF
V_{OC}	Video Output Compliance		-0.3		2.0	V
R_{OUT}	Video Output Resistance			15		kΩ
C_{OUT}	Video Output Capacitance	I_{OUT} = 0mA, f = 1MHz		15	25	pF

Notes:

1. Maximum I_{DD} with V_{DD} = Max and T_A = Min. Outputs loaded wtih 75Ω.
2. I_{DDQ} when $\overline{RESET}$ = LOW, disabling D/A converters.

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DOZ}	Output Delay, $\overline{CS}$ to low-Z		4			ns
t_{HOM}	Output Hold Time, $\overline{CS}$ to high-Z		30			ns
t_{DOM}	Output Delay, $\overline{CS}$ to Data Valid				23	ns
t_{DOTP}	Output Delay, TCK to TDO Valid				13	ns
t_{HOTP}	Output Hold Time, TCK to TDO Valid		3			ns
t_R	D/A Output Current Risetime	10% to 90% of full scale		2		ns
t_F	D/A Output Current Falltime	90% to 10% of full scale		2		ns
t_{DOV}	Analog Output Delay		3	10	17	ns

Note: Timing reference points are at the 50% level. Analog C_{LOAD} <10pF, D_{7-0} load <40pF.

SET TOP BOX

System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Units
RES	D/A Converter Resolution		9	9	9	Bits
dp	Differential Phase	PXCK = 27 MHz, 40 IRE Ramp			1.0	degree
dg	Differential Gain	PXCK = 27 MHz, 40 IRE Ramp			1.5	%
CNLP	Chroma Nonlinear Phase	NTC-7 Combination			±1.25	degree
CNLG	Chroma Nonlinear Gain	NTC-7 Combination			±1.0	%
CLIM	Chroma/Luma Intermodulation	NTC-7 Combination				IRE
CLGI	Chroma/Luma Gain inequality	NTC-7 Composite			3	%
CLDI	Chroma/Luma Delay inequality	NTC-7 Composite				ns
LNLD	Luma Nonlinear Distortion	NTC-7			2	%
FTWD	Field Time Waveform Distortion	NTC-7			.5	%
LTWD	Line Time Waveform Distortion	NTC-7			.5	%
LOTWD	Long Time Waveform Distortion, initial and peak overshoot	10%/90% APL Bounce				IRE
LOTWD	Long Time Waveform Distortion, peak overshoot	after 5 seconds, 10%/90% APL Bounce				IRE
LDCOFF	Line-by-Line DC Offset					IRE
DYNG	Dynamic Gain	NTC-7				IRE
NOISE	Noise Level (Note 1)	100% unmod. ramp	-55			dB rms
CAMN	Chroma AM Noise	Red field	-63			dB rms
CPMN	Chroma PM Noise	Red field	-62			dB rms
SYR	Sync Pulse Rise Time	NTSC		137		ns
		PAL		250		
SYF	Sync Pulse Fall Time	NTSC		134		ns
		PAL		248		
PSRR	Power Supply Rejection Ratio	C_{BYP} = 0.1 µF, f = 1 kHz		0.02		%/%V_{DD}

Notes:

1. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, with Tilt Null ON measured using VM700 "Measure Mode."

Preliminary Information

Applications Information

The circuit in Figure 24 shows the connection of power supply voltages, output reconstruction filters and the external voltage reference. All VDD pins should be connected to the same power source.

The full-scale output voltage level, V_{OUT}, on the COMPOSITE, LUMA, and CHROMA pins is found from:

$$V_{OUT} = I_{OUT} \times RL = K \times I_{REF} \times R_L$$
$$= K \times (V_{REF}/R_{REF}) \times R_L$$

where:

1. I_{OUT} is the full-scale output current sourced by the TMC2490 D/A converters.
2. R_L is the net resistive load on the COMPOSITE, CHROMA, and LUMA output pins.
3. K is a constant for the TMC2490 D/A converters (approximately equal to 10.4).
4. I_{REF} is the reference current flowing out of the R_{REF} pin to ground.
5. V_{REF} is the voltage measured on the V_{REF} pin.
6. R_{REF} is the total resistance connected between the R_{REF} pin and ground.
7. A 0.1µF capacitor should be connected between C_{BYP} and V_{DDA}.

The reference voltage in Figure 24 is from an LM185 1.2 Volt band-gap reference. The 392 Ohm resistor connected from R_{REF} to ground sets the overall "gain" of the three D/A converters of the TMC2490. Varying R_{REF} ±5% will cause the full-scale output voltage on COMPOSITE, LUMA, and CHROMA to vary by ±5%.

The suggested output reconstruction filter is the same one used on the TMC2063P7C Demonstration Board. The phase and frequency response of this filter is shown in Figure 23. The Schottky diode is for ESD protection.

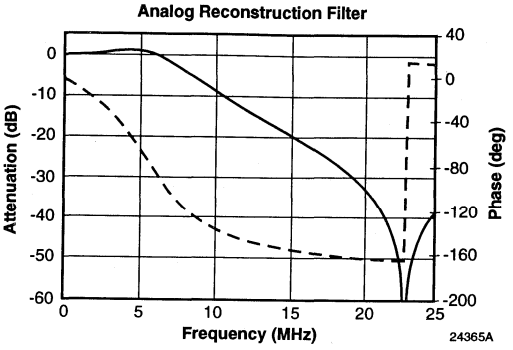


Figure 23. Response of Recommended Output Filter

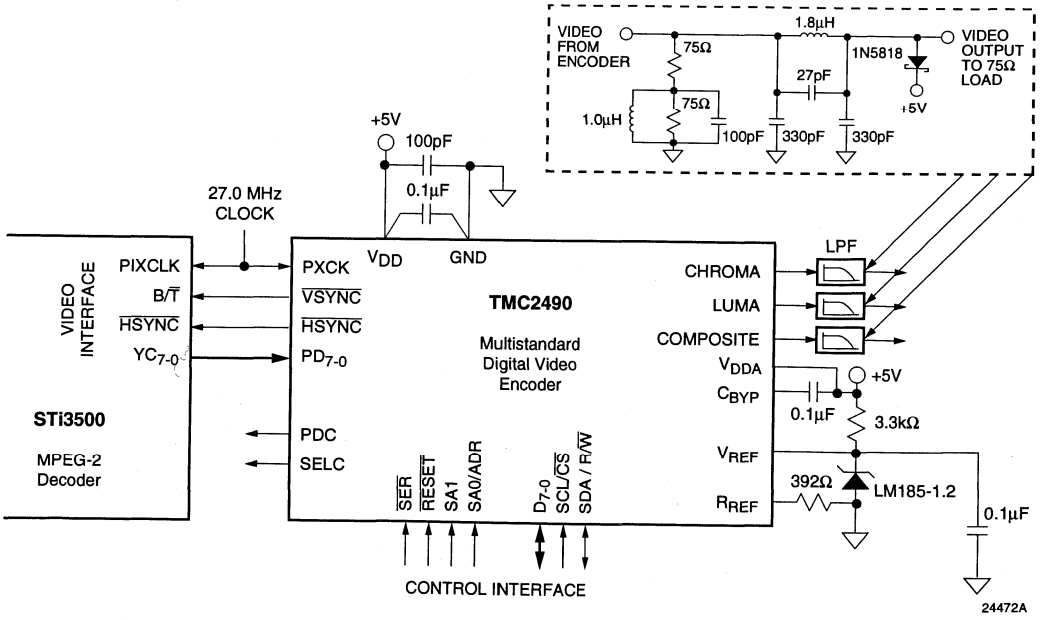


Figure 24. Typical Application Circuit

SET TOP BOX

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2490R2C	0°C to 70°C	Commercial	44-Lead PLCC	2490R2C

Ceramic Dual Inline Packages

Plastic Dual Inline Packages

Pin Grid Array Packages

Metal Can IC Header Packages

Small Outline IC Packages

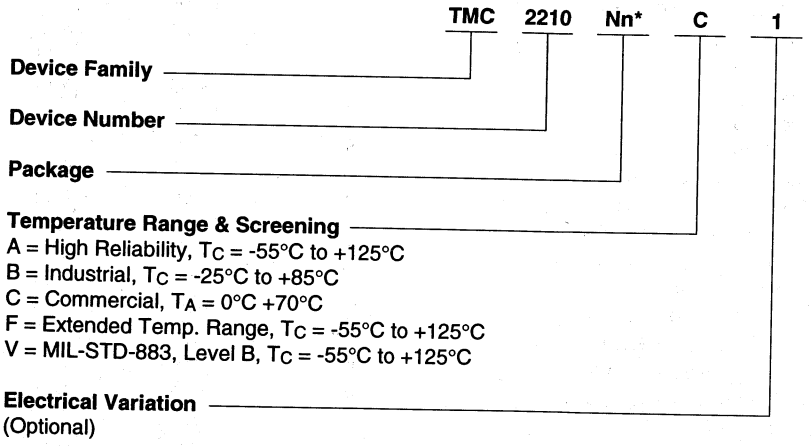
Ceramic Leadless Chip Carrier Packages

Plastic Leaded Chip Carrier Packages

Metric Quad Flat Pack Packages

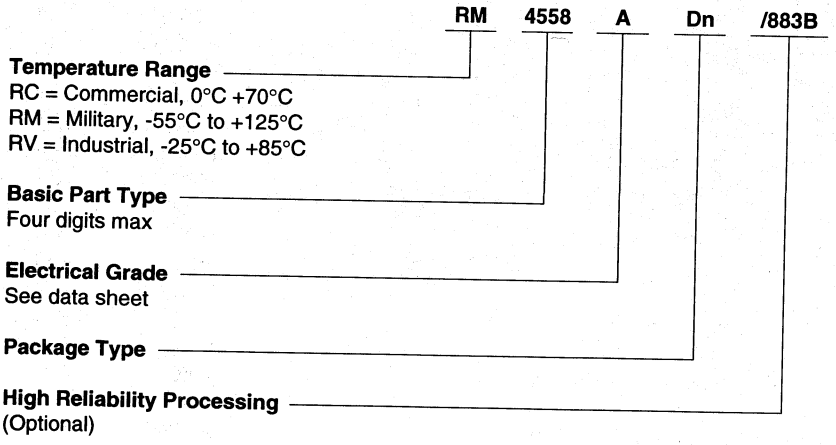
Ordering Information

TMC Series



*n – Refer to product listing for second digit

RC/RM/RV Series



*Second digit is optional. Refer to product listing.

Cross-Reference by Part Number

Device	Description	Lead Count	Package Type	Page #
RC2211N	FSK Decoder	14	PDIP	6-15
RC3403AN	Ground Sensing Quad Op Amp	14	PDIP	6-15
RC4136M	Quad Op Amp	14	SOIC	6-25
RC4136N	Quad Op Amp	14	PDIP	6-15
RC4156D	Quad Op Amp	14	CerDIP	6-10
RC4156M	Quad Op Amp	14	SOIC	6-25
RC4156N	Quad Op Amp	14	PDIP	6-15
RC4157M	High Speed Quad Op Amp	14	SOIC	6-25
RC4157N	High Speed Quad Op Amp	14	PDIP	6-15
RC4190D	Micro Power Switching Regulator	8	CerDIP	6-9
RC4190M	Micro Power Switching Regulator	8	SOIC	6-24
RC4190N	Micro Power Switching Regulator	8	PDIP	6-14
RC4191N	Micro Power Switching Regulator	8	PDIP	6-14
RC4192N	Micro Power Switching Regulator	8	PDIP	6-14
RC4193M	Micro Power Switching Regulator	8	SOIC	6-24
RC4193N	Micro Power Switching Regulator	8	PDIP	6-14
RC4194D	Variable Dual Regulator	14	CerDIP	6-10
RC4194K	Variable Dual Regulator	9	TO-66	6-23
RC4194N	Variable Dual Regulator	14	PDIP	6-15
RC4195K	Dual Voltage Regulator	9	TO-66	6-23
RC4195N	Dual Voltage Regulator	8	PDIP	6-14
RC4195T	Dual Voltage Regulator	8	TO-99	6-22
RC4200AN	Four Quadrant Multiplier	8	PDIP	6-14
RC4200N	Four Quadrant Multiplier	8	PDIP	6-14
RC4207FN	Dual OP-07	8	PDIP	6-14
RC4207GN	Dual OP-07	8	PDIP	6-14
RC4227FN	Dual OP-27	8	PDIP	6-14
RC4227GN	Dual OP-27	8	PDIP	6-14
RC4277FD	Dual Precision Op Amp	8	CerDIP	6-9
RC4277FN	Dual Precision Op Amp	8	PDIP	6-14
RC4391M	Micro Power Inverting Regulator	8	SOIC	6-24
RC4391N	Micro Power Inverting Regulator	8	PDIP	6-14
RC4558M	Dual Op Amp Low Noise	8	SOIC	6-24
RC4558N	Dual Op Amp Low Noise	8	PDIP	6-14
RC4559D	Dual Op Amp High Slew Rate	8	CerDIP	6-9
RC4559M	Dual Op Amp High Slew Rate	8	SOIC	6-24
RC4559N	Dual Op Amp High Slew Rate	8	PDIP	6-14
RC5032M8	5V–3.3V Step-Down DC-DC Converter	8	SOIC	6-24
RC5032N8	5V–3.3V Step-Down DC-DC Converter	8	PDIP	6-14
RC5033M16	Adjustable Synchronous DC-DC Converter	16	SOIC	6-27
RC5034M16	High Accuracy Synchronous DC-DC Converter	16	SOIC	6-27
RC5040M20	Programmable Synchronous DC-DC Converter	20	SOIC	6-28
RC5510V	Rapper Stereo Sound Drivers	28	PLCC	6-32
RC5512V	Rapper Stereo Sound Drivers	28	PLCC	6-32
RC5532AD	Dual Low Noise Op Amp	8	CerDIP	6-9
RC5532AN	Dual Low Noise Op Amp	8	PDIP	6-14
RC5532D	Dual Low Noise Op Amp	8	CerDIP	6-9
RC5532N	Dual Low Noise Op Amp	8	PDIP	6-14
RC5534AN	Low Noise Op Amp	8	PDIP	6-14
RC5534N	Low Noise Op Amp	8	PDIP	6-14
RC6100NC	NTSC/PAL Horizontal Line Genlock	24	SOIC	6-30

Cross-Reference by Part Number (continued)

Device	Description	Lead Count	Package Type	Page #
RC6302M8	Dual Video Amplifier	8	SOIC	6-24
RC6303PN	Triple Video Amplifier With Enable	16	SOIC	6-26
RC6601NE	Programmable Analog Video Filter	16	SOIC	6-27
RC6702PN	RGB To YC_BC_R Transcoder	16	SOIC	6-26
RC6704PN	Triple Fixed Gain Video Amps With Enable	16	SOIC	6-26
RCC700AKA	Fibre Channel Transceiver	64	MQFP	6-36
RCC700AQD	Fibre Channel Transceiver	68	PLCC	6-34
RM2211D	FSK Decoder	14	CerDIP	6-10
RM2211D/883B	FSK Decoder	14	CerDIP	6-10
RM4136D	Quad Op Amp	14	CerDIP	6-10
RM4136D/883B	Quad Op Amp	14	CerDIP	6-10
RM4156D	Quad Op Amp	14	CerDIP	6-10
RM4156D/883B	Quad Op Amp	14	CerDIP	6-10
RM4190D	Micro Power Switching Regulator	8	CerDIP	6-9
RM4190D/883B	Micro Power Switching Regulator	8	CerDIP	6-9
RM4191D	Micro Power Switching Regulator	8	CerDIP	6-9
RM4191D/883B	Micro Power Switching Regulator	8	CerDIP	6-9
RM4192D	Micro Power Switching Regulator	8	CerDIP	6-9
RM4193D	Micro Power Switching Regulator	8	CerDIP	6-9
RM4194D	Variable Dual Regulator	8	CerDIP	6-9
RM4194D/883B	Variable Dual Regulator	8	CerDIP	6-9
RM4194K	Variable Dual Regulator	9	TO-66	6-23
RM4195K	Dual Voltage Regulator	9	TO-66	6-23
RM4195T	Dual Voltage Regulator	8	TO-99	6-22
RM4195T/883	Dual Voltage Regulator	8	TO-99	6-22
RM4200AD	Four Quadrant Multiplier	8	CerDIP	6-9
RM4200AD/883B	Four Quadrant Multiplier	8	CerDIP	6-9
RM4200D	Four Quadrant Multiplier	8	CerDIP	6-9
RM4227BD/883B	Dual OP-27 Mil	8	CerDIP	6-9
RM4391D	Micro Power Inverting Regulator	8	CerDIP	6-9
RM4558D	Dual Op Amp Low Noise	8	CerDIP	6-9
RM4558D/883B	Dual Op Amp Low Noise	8	CerDIP	6-9
RM4559D	Dual Op Amp High Slew Rate	8	CerDIP	6-9
RM4559D/883B	Dual Op Amp High Slew Rate	8	CerDIP	6-9
RM4559T	Dual Op Amp High Slew Rate	8	TO-99	6-22
RM5532AD	Dual Low Noise Op Amp	8	CerDIP	6-9
RM5532AD/883B	Dual Low Noise Op Amp	8	CerDIP	6-9
RM5532AT	Dual Low Noise Op Amp	8	TO-99	6-22
RM5532AT/883B	Dual Low Noise Op Amp	8	TO-99	6-22
RM5532D	Dual Low Noise Op Amp	8	CerDIP	6-9
RM5532D/883B	Dual Low Noise Op Amp	8	CerDIP	6-9
RM5532T	Dual Low Noise Op Amp	8	TO-99	6-22
RM5532T/883B	Dual Low Noise Op Amp	8	TO-99	6-22
RM5534AD	Low Noise Op Amp	8	CerDIP	6-9
RM5534AD/883B	Low Noise Op Amp	8	CerDIP	6-9
RM5534AT	Low Noise Op Amp	8	TO-99	6-22
RM5534AT/883B	Low Noise Op Amp	8	TO-99	6-22
RM5534D	Low Noise Op Amp	8	CerDIP	6-9
RM5534D/883B	Low Noise Op Amp	8	CerDIP	6-9
RM5534T	Low Noise Op Amp	8	TO-99	6-22
RM5534T/883B	Low Noise Op Amp	8	TO-99	6-22

Cross-Reference by Part Number (continued)

Device	Description	Lead Count	Package Type	Page #
RV2211N	FSK Decoder	14	PDIP	6-15
RV4145M	Low Power GFI	8	SOIC	6-24
RV4145N	Low Power GFI	8	PDIP	6-14
RV4190N	Micro Power Switching Regulator	8	PDIP	6-14
RV4191N	Micro Power Switching Regulator	8	PDIP	6-14
RV4192N	Micro Power Switching Regualtor	8	PDIP	6-14
RV4193N	Micro Power Switching Regulator	8	PDIP	6-14
RV4391D	Micro Power Inverting Regulator	8	CerDIP	6-9
RV4391N	Micro Power Inverting Regulator	8	PDIP	6-14
TMC1103KLC20	Triple 8-bit ADC, 20 Msps, PLL	80	MQFP	6-37
TMC1103KLC30	Triple 8-bit ADC, 30 Msps, PLL	80	MQFP	6-37
TMC1103KLC40	Triple 8-bit ADC, 40 Msps, PLL	80	MQFP	6-37
TMC1173AM7C05	A/D, 8 bit, 5 Msps, CMOS, +3V Supply	24	SOIC	6-29
TMC1173AM7C10	A/D, 8 bit, 10 Msps, CMOS, +3V Supply	24	SOIC	6-29
TMC1173AN2C05	A/D, 8 bit, 5 Msps, CMOS, +3V Supply	24	PDIP	6-16
TMC1173AN2C10	A/D, 8 bit, 10 Msps, CMOS, +3V Supply	24	PDIP	6-16
TMC1173AR3C05	A/D, 8 bit, 5 Msps, CMOS, +3V Supply	28	PLCC	6-32
TMC1173AR3C10	A/D, 8 bit, 10 Msps, CMOS, +3V Supply	28	PLCC	6-32
TMC1175AM7C20	A/D, 8 bit, 20 Msps, CMOS	24	SOIC	6-29
TMC1175AM7C30	A/D, 8 bit, 30 Msps, CMOS	24	SOIC	6-29
TMC1175AM7C40	A/D, 8 bit, 40 Msps, CMOS	24	SOIC	6-29
TMC1175AN2C20	A/D, 8 bit, 20 Msps, CMOS	24	PDIP	6-16
TMC1175AN2C30	A/D, 8 bit, 30 Msps, CMOS	24	PDIP	6-16
TMC1175AN2C40	A/D, 8 bit, 40 Msps, CMOS	24	PDIP	6-16
TMC1175AR3C20	A/D, 8 bit, 20 Msps, CMOS	28	PLCC	6-32
TMC1175AR3C30	A/D, 8 bit, 30 Msps, CMOS	28	PLCC	6-32
TMC1175AR3C40	A/D, 8 bit, 40 Msps, CMOS	28	PLCC	6-32
TMC1175B2V20	A/D, 8 bit, 20 Msps, CMOS	24	CerDIP	6-11
TMC1175C3V20	A/D, 8 bit, 20 Msps, CMOS	28	LCC	6-31
TMC1203KLC20	Triple 8-bit ADC, 20 Msps	80	MQFP	6-37
TMC1203KLC30	Triple 8-bit ADC, 30 Msps	80	MQFP	6-37
TMC1203KLC40	Triple 8-bit ADC, 40 Msps	80	MQFP	6-37
TMC1273M7C05	A/D, 8 bit, 5 Msps, CMOS, +3V Supply	24	SOIC	6-29
TMC1273M7C10	A/D, 8 bit, 10 Msps, CMOS, +3V Supply	24	SOIC	6-29
TMC1273N2C05	A/D, 8 bit, 5 Msps, CMOS, +3V Supply	24	PDIP	6-16
TMC1273N2C10	A/D, 8 bit, 10 Msps, CMOS, +3V Supply	24	PDIP	6-16
TMC1273R3C05	A/D, 8 bit, 5 Msps, CMOS, +3V Supply	28	PLCC	6-32
TMC1273R3C10	A/D, 8 bit, 10 Msps, CMOS, +3V Supply	28	PLCC	6-32
TMC1275M7C20	A/D, 8 bit, 20 Msps, CMOS	24	SOIC	6-29
TMC1275M7C30	A/D, 8 bit, 30 Msps, CMOS	24	SOIC	6-29
TMC1275M7C40	A/D, 8 bit, 40 Msps, CMOS	24	SOIC	6-30
TMC1275N2C20	A/D, 8 bit, 20 Msps, CMOS	24	PDIP	6-16
TMC1275N2C30	A/D, 8 bit, 30 Msps, CMOS	24	PDIP	6-16
TMC1275N2C40	A/D, 8 bit, 40 Msps, CMOS	24	PDIP	6-16
TMC1275R3C20	A/D, 8 bit, 20 Msps, CMOS	28	PLCC	6-32
TMC1275R3C30	A/D, 8 bit, 30 Msps, CMOS	28	PLCC	6-32
TMC1275R3C40	A/D, 8 bit, 40 Msps, CMOS	28	PLCC	6-32
TMC2011AB2C	Prog. Digital Delay, 3-18x8, 30 MHz	24	CerDIP	6-11
TMC2011AB2C1	Prog. Digital Delay, 3-18x8, 40 MHz	24	CerDIP	6-11
TMC2011AN2C	Prog. Digital Delay, 3-18x8, 30 MHz	24	PDIP	6-16
TMC2011AN2C1	Prog. Digital Delay, 3-18x8, 40 MHz	24	PDIP	6-16

Cross-Reference by Part Number (continued)

Device	Description	Lead Count	Package Type	Page #
TMC2011AR3C	Prog. Digital Delay, 3-18x8, 30 MHz	28	PLCC	6-32
TMC2011AR3C1	Prog. Digital Delay, 3-18x8, 40 MHz	28	PLCC	6-32
TMC2011B2A	Prog. Digital Delay, 3-18x8 bit, 30 MHz	24	CerDIP	6-11
TMC2011B2V	Prog. Digital Delay, 3-18x8 bit, 30 MHz	24	CerDIP	6-11
TMC2011C3A	Prog. Digital Delay, 3-18x8 bit, 30 MHz	28	LCC	6-31
TMC2011C3V	Prog. Digital Delay, 3-18x8 bit, 30 MHz	28	LCC	6-31
TMC2081KBC	Digital Video Mixer	128	MQFP	6-40
TMC2111AB2C	Prog. Digital Delay, 1-16x8, 30 MHz	24	CerDIP	6-11
TMC2111AB2C1	Prog. Digital Delay, 1-16x8, 40 MHz	24	CerDIP	6-11
TMC2111AN2C	Prog. Digital Delay, 1-16x8, 30 MHz	24	PDIP	6-16
TMC2111AN2C1	Prog. Digital Delay, 1-16x8, 40 MHz	24	PDIP	6-16
TMC2111AR3C	Prog. Digital Delay, 1-16x8, 30 MHz	28	PLCC	6-32
TMC2111AR3C1	Prog. Digital Delay, 1-16x8, 40 MHz	28	PLCC	6-32
TMC2111B2A	Prog. Digital Delay, 1-16x8 bit, 30 MHz	24	CerDIP	6-11
TMC2111B2V	Prog. Digital Delay, 1-16x8 bit, 30 MHz	24	CerDIP	6-11
TMC2111C3A	Prog. Digital Delay, 1-16x8 bit, 30 MHz	28	LCC	6-31
TMC2111C3V	Prog. Digital Delay, 1-16x8 bit, 30 MHz	28	LCC	6-31
TMC22071R1C	Genlocking Video Digitizer	68	PLCC	6-34
TMC22091R0C	Digital Video Encoder	84	PLCC	6-35
TMC22191R0C	Digital Video Encoder Plus	84	PLCC	6-35
TMC2220G8C	Correlator, 32x4 bit, 17 MHz	68	PPGA	6-18
TMC2220G8C1	Correlator, 32x4 bit, 20 MHz	68	PPGA	6-18
TMC2220G8V	Correlator, 32x4 bit, 17 MHz	68	PPGA	6-18
TMC2220G8V1	Correlator, 32x4 bit, 20 MHz	68	PPGA	6-18
TMC2220H8C	Correlator, 32x4 bit, 17 MHz	69	PPGA	6-20
TMC2220H8C1	Correlator, 32x4 bit, 20 MHz	69	PPGA	6-20
TMC2221B6C	Correlator, 128x1 bit, 17 MHz	28	CerDIP	6-13
TMC2221B6C1	Correlator, 128x1 bit, 20 MHz	28	CerDIP	6-13
TMC2221B6V	Correlator, 128x1 bit, 17 MHz	28	CerDIP	6-13
TMC2221B6V1	Correlator, 128x1 bit, 20 MHz	28	CerDIP	6-13
TMC22290R2C	Digital Video Encoder	44	PLCC	6-33
TMC2242AR2C	Half-Band Filter, 12/16 bit, 30 MHz	44	PLCC	6-33
TMC2242AR2C1	Half-Band Filter, 12/16 bit, 40 MHz	44	PLCC	6-33
TMC2242AR2C2	Half-Band Filter, 12/16 bit, 60 MHz	44	PLCC	6-33
TMC2242BR2C	Half-Band Filter, 12/16 bit, 30 MHz	44	PLCC	6-33
TMC2242BR2C1	Half-Band Filter, 12/16 bit, 40 MHz	44	PLCC	6-33
TMC2242BR2C2	Half-Band Filter, 12/16 bit, 60 MHz	44	PLCC	6-33
TMC2243G8A	Video Filter, 10x10 bit, 3 Tap, 20 MHz	68	PPGA	6-18
TMC2243G8C	Video Filter, 10x10 bit, 3 Tap, 20 MHz	68	PPGA	6-18
TMC2243G8V	Video Filter, 10x10 bit, 3 Tap, 20 MHz	68	PPGA	6-18
TMC2243H8C	Video Filter, 10x10 bit, 3 Tap, 20 MHz	69	PPGA	6-20
TMC2246AH5C	Image Filter, 10x11 bit, 30 MHz	121	PPGA	6-21
TMC2246AH5C1	Image Filter, 10x11 bit, 40 MHz	121	PPGA	6-21
TMC2246AH5C2	Image Filter, 10x11 bit, 60 MHz	121	PPGA	6-21
TMC2246AKEC	Image Filter, 10x11 bit, 30 MHz	120	MQFP	6-39
TMC2246AKEC1	Image Filter, 10x11 bit, 40 MHz	120	MQFP	6-39
TMC2246AKEC2	Image Filter, 10x11 bit, 60 MHz	120	MQFP	6-39
TMC2249AH5C	Digital Mixer, 12x12 bit, 25 MHz	121	PPGA	6-21
TMC2249AH5C1	Digital Mixer, 12x12 bit, 40 MHz	121	PPGA	6-21
TMC2249AH5C2	Digital Mixer, 12x12 bit, 60 MHz	121	PPGA	6-21
TMC2249AKEC	Digital Mixer, 12x12 bit, 25 MHz	120	MQFP	6-39

Cross-Reference by Part Number (continued)

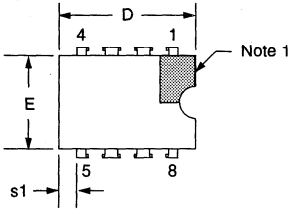
Device	Description	Lead Count	Package Type	Page #
TMC2249AKEC1	Digital Mixer, 12x12 bit, 40 MHz	120	MQFP	6-39
TMC2249AKEC2	Digital Mixer, 12x12 bit, 60 MHz	120	MQFP	6-39
TMC2250AH5C	Matrix Multiplier, 12x10 bit, 30 MHz	121	PPGA	6-21
TMC2250AH5C2	Matrix Multiplier, 12x10 bit, 40 MHz	121	PPGA	6-21
TMC2250AH5C3	Matrix Multiplier, 12x10 bit, 50 MHz	121	PPGA	6-21
TMC2250AKEC	Matrix Multiplier, 12x10 bit, 30 MHz	120	MQFP	6-39
TMC2250AKEC2	Matrix Multiplier, 12x10 bit, 40 MHz	120	MQFP	6-39
TMC2250AKEC3	Matrix Multiplier, 12x10 bit, 50 MHz	120	MQFP	6-39
TMC2255R1C	Convolver, 2D, 5x5, 8 bit, 10 MHz	68	PLCC	6-34
TMC2255R1C1	Convolver, 2D, 5x5, 8 bit, 12.5 MHz	68	PLCC	6-34
TMC2272AH5C	Colorspace Converter, 30 MHz	121	PPGA	6-21
TMC2272AH5C2	Colorspace Converter, 40 MHz	121	PPGA	6-21
TMC2272AH5C3	Colorspace Converter, 50 MHz	121	PPGA	6-21
TMC2272AKEC	Colorspace Converter, 30 MHz	120	MQFP	6-39
TMC2272AKEC2	Colorspace Converter, 40 MHz	120	MQFP	6-39
TMC2272AKEC3	Colorspace Converter, 50 MHz	120	MQFP	6-39
TMC2302H5C	Image Manipulation Sequencer, 30 MHz	121	PPGA	6-21
TMC2302H5C1	Image Manipulation Sequencer, 40 MHz	121	PPGA	6-21
TMC2302KEC	Image Manipulation Sequencer, 30 MHz	120	MQFP	6-39
TMC2302KEC1	Image Manipulation Sequencer, 40 MHz	120	MQFP	6-39
TMC2330AH5C	Coord. Transformer, 16x16 bit, 20MHz	121	PPGA	6-21
TMC2330AH5C1	Coord. Transformer, 16x16 bit, 40MHz	121	PPGA	6-21
TMC2330AH5C2	Coord. Transformer, 16x16 bit, 50MHz	121	PPGA	6-21
TMC2330AKEC	Coord. Transformer, 16x16 bit, 20MHz	120	MQFP	6-39
TMC2330AKEC1	Coord. Transformer, 16x16 bit, 40MHz	120	MQFP	6-39
TMC2330AKEC2	Coord. Transformer, 16x16 bit, 50MHz	120	MQFP	6-39
TMC2340AH5C	Digital Synthesizer, Dual 16 bit, 20MHz	121	PPGA	6-21
TMC2340AH5C1	Digital Synthesizer, Dual 16 bit, 40MHz	121	PPGA	6-21
TMC2340AH5C2	Digital Synthesizer, Dual 16 bit, 50MHz	121	PPGA	6-21
TMC2340AKEC	Digital Synthesizer, Dual 16 bit, 20MHz	120	MQFP	6-39
TMC2340AKEC1	Digital Synthesizer, Dual 16 bit, 40MHz	120	MQFP	6-39
TMC2340AKEC2	Digital Synthesizer, Dual 16 bit, 50MHz	120	MQFP	6-39
TMC2340H5C	Digital Synthesizer, Dual 16 bit, 20MOPS	121	PPGA	6-21
TMC2340H5C1	Digital Synthesizer, Dual 16 bit, 25MOPS	121	PPGA	6-21
TMC2360KLC	Video Output Processor, VGA to NTSC/PAL	80	MQFP	6-37
TMC2360R0C	Video Output Processor, VGA to NTSC/PAL	84	PLCC	6-35
TMC2490R244	Multistandard Digital Video Encoder	44	PLCC	6-33
TMC3003R2C30	CMOS, Triple 10-bit DAC, 30MHz	44	PLCC	6-33
TMC3003R2C50	CMOS, Triple 10-bit DAC, 50MHz	44	PLCC	6-33
TMC3003R2C80	CMOS, Triple 10-bit DAC, 80MHz	44	PLCC	6-33
TMC3503R2C35	CMOS, Triple 8-bit DAC, 30MHz	44	PLCC	6-33
TMC3503R2C50	CMOS, Triple 8-bit DAC, 50MHz	44	PLCC	6-33
TMC3503R2C80	CMOS, Triple 8-bit DAC, 80MHz	44	PLCC	6-33

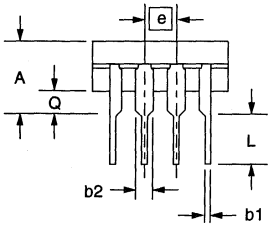
8 Lead Ceramic Dual Inline Package (CerDIP) – .300" Body Width

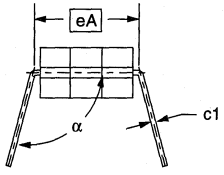
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.





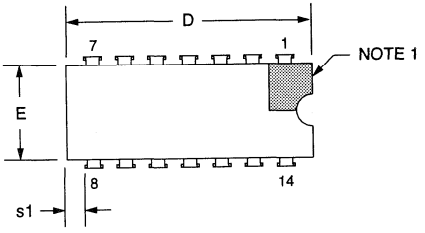


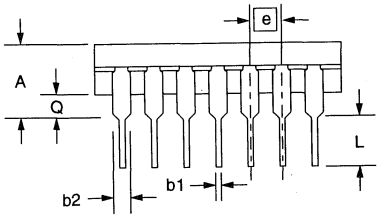
14 Lead Ceramic Dual Inline Package (CerDIP) – .300" Body Width

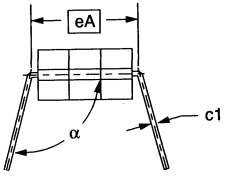
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.





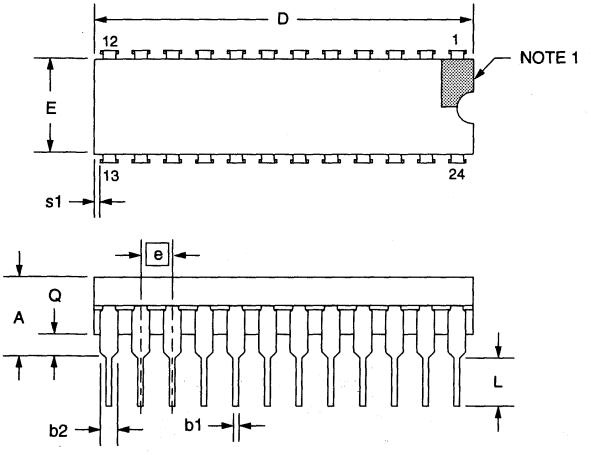


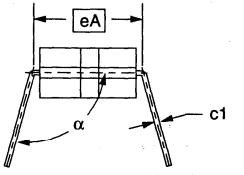
24 Lead Ceramic Dual Inline Package (CerDIP) – .300" Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	1.280	—	32.51	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 12, 13 and 24 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 24.
6. Applies to all four corners (leads number 1, 12, 13, and 24).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twenty-two spaces.





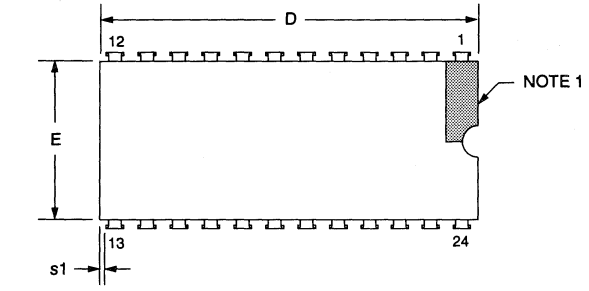
PACKAGING

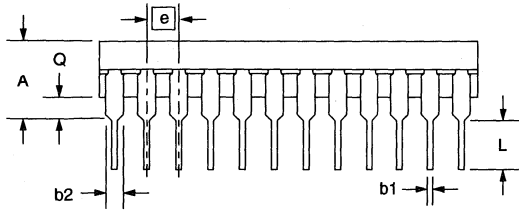
24 Lead Ceramic Dual Inline Package (CerDIP) – .600" Body Width

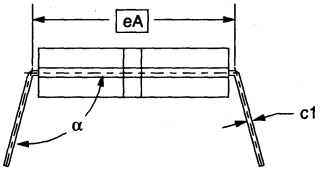
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.225	—	5.72	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	1.290	—	32.77	4
E	.500	.610	12.70	15.49	4
e	.100 BSC		2.54 BSC		5
eA	.600 BSC		15.24 BSC		7
L	.120	.200	3.05	5.08	
Q	.015	.075	.38	1.91	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 12, 13 and 24 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 28.
6. Applies to all four corners (leads number 1, 12, 13, and 24).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twenty-two spaces.





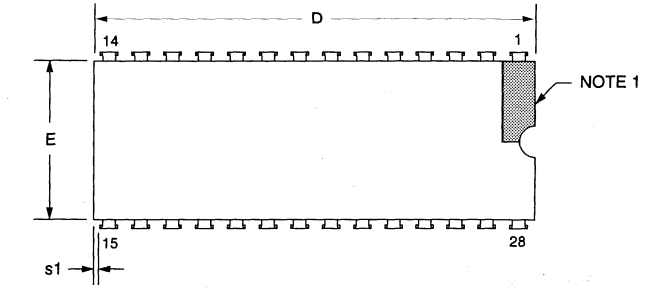


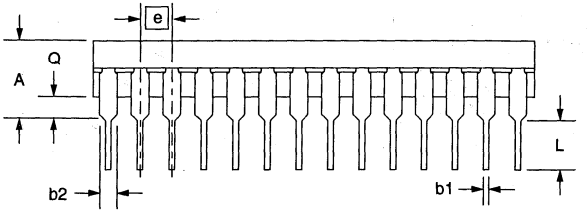
28 Lead Ceramic Dual Inline Package (CerDIP) – .600" Body Width

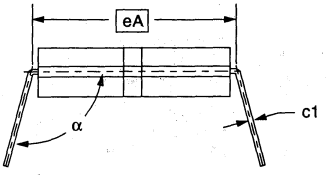
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.232	—	5.92	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	1.490	—	37.85	4
E	.500	.610	12.70	15.49	4
e	.100 BSC		2.54 BSC		5
eA	.600 BSC		15.24 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 14, 15 and 28 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 28.
6. Applies to all four corners (leads number 1, 14, 15, and 28).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twenty-six spaces.







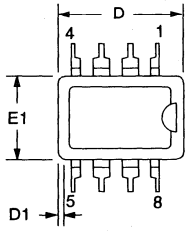
PACKAGING

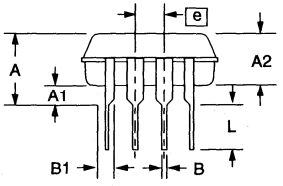
8 Lead Plastic Dual Inline Package (PDIP) – .300" Body Width

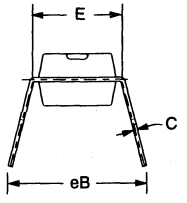
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.





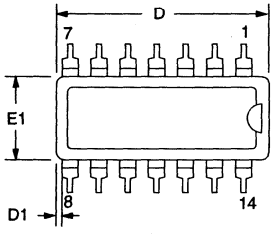


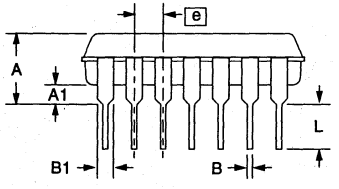
14 Lead Plastic Dual Inline Package (PDIP) – .300" Body Width

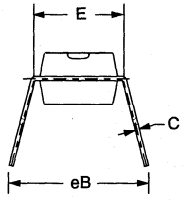
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







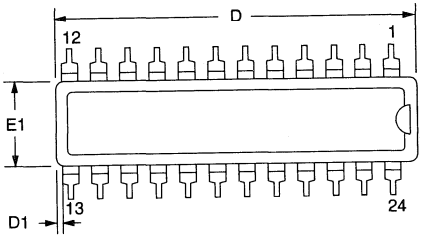
PACKAGING

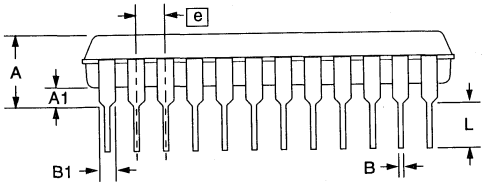
24 Lead Plastic Dual Inline Package (PDIP) – .300" Body Width

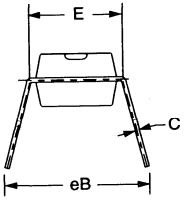
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.53	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	1.125	1.275	28.58	32.39	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	24		24		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.





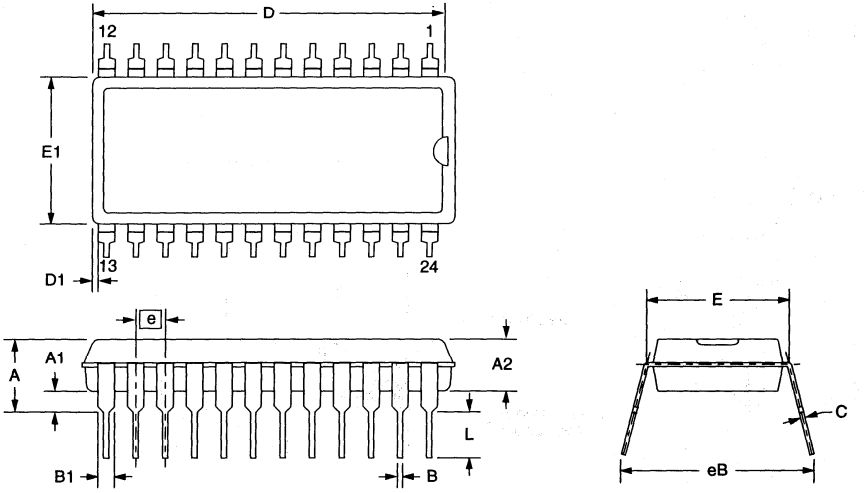


24 Lead Plastic Dual Inline Package (PDIP) – .600" Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.250	—	6.35	
A1	.015	—	.38	—	
A2	.125	.195	3.18	4.95	
B	.014	.022	.36	.56	
B1	.030	.070	.76	1.78	
C	.008	.015	.20	.38	4
D	1.150	1.290	29.21	32.77	2
D1	.005	—	.13	—	
E	.600	.625	15.24	15.88	
E1	.485	.580	12.32	14.73	2
e	.100 BSC		2.54 BSC		
eB	—	.700	—	17.78	
L	.115	.200	2.92	5.08	
N	24		24		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.

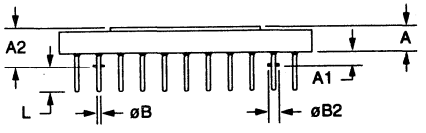


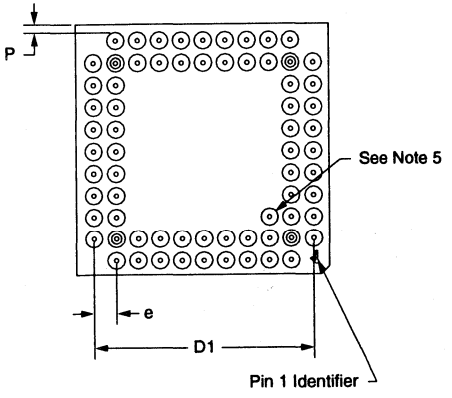
68 Pin Grid Array (PGA) – Cavity Up

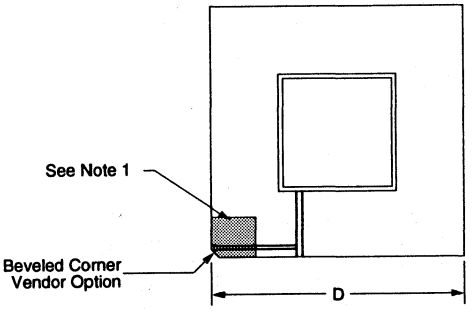
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.125	2.03	3.18	
A1	.040	.060	1.02	1.52	
A2	.115	.190	2.92	4.83	
øB	.017	.020	0.43	0.51	
øB2	.050 NOM.		1.27 NOM.		
D	1.140	1.180	28.96	29.97	
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.120	.140	3.05	3.56	
M	11		11		2
N	68		68		3
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Dimension "M" defines matrix size.
3. Dimension "N" defines the maximum possible number of pins.
4. Controlling dimension: inch.
5. Optional index pin.





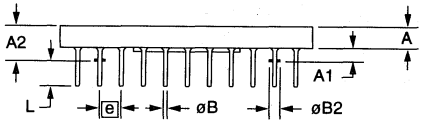


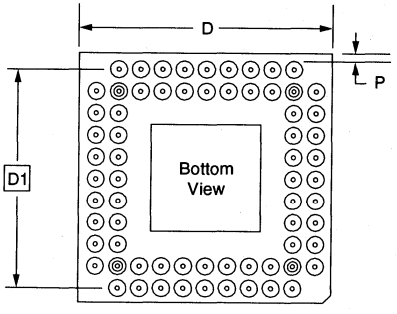
68 Pin Grid Array (PGA) – Cavity Down, No Heatsink

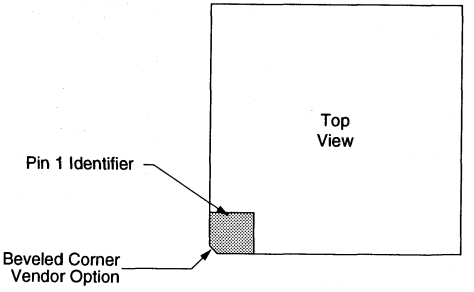
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.125	2.03	3.18	
A1	.025	.060	0.64	1.52	
A2	.105	.180	2.67	4.57	
øB	.017	.020	0.43	0.51	
øB2	.050 NOM.		1.27 NOM.		
D	1.140	1.180	28.96	29.97	
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.120	.140	3.05	3.56	
M	11		11		2
N	68		68		3
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Dimension "M" defines matrix size.
3. Dimension "N" defines the maximum possible number of pins.
4. Controlling dimension: inch.







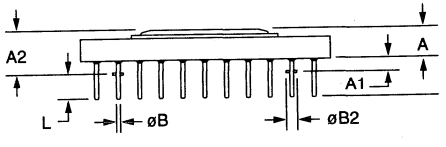
PACKAGING

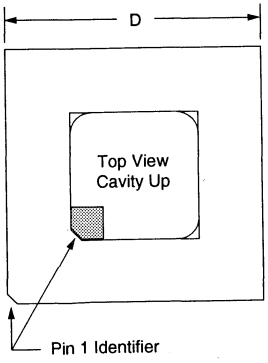
69 Plastic Pin Grid Array (PPGA)

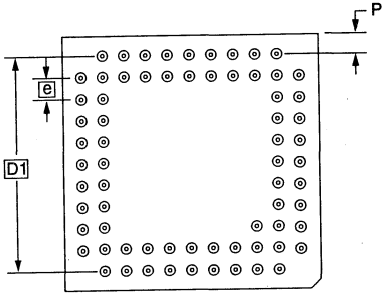
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.140	1.180	28.96	29.97	SQ
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
M	11		11		3
N	68		68		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.





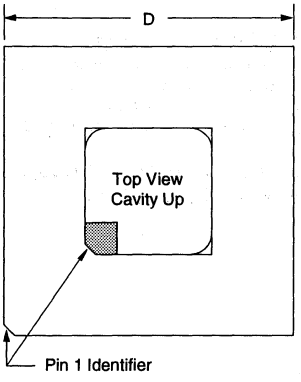


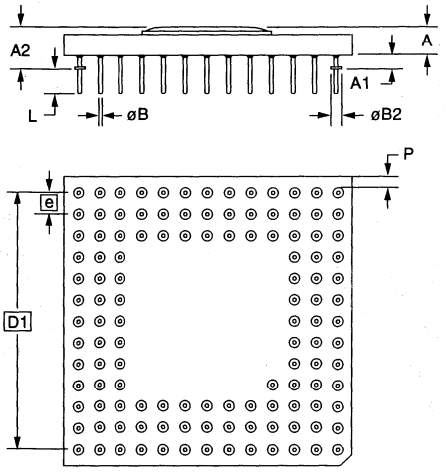
121 Plastic Pin Grid Array (PPGA)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

Notes:

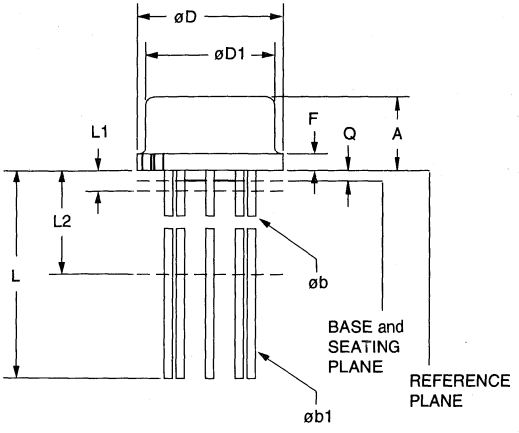
1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.

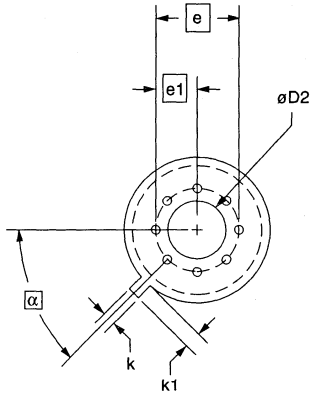




PACKAGING

8 Lead Metal Can IC Header



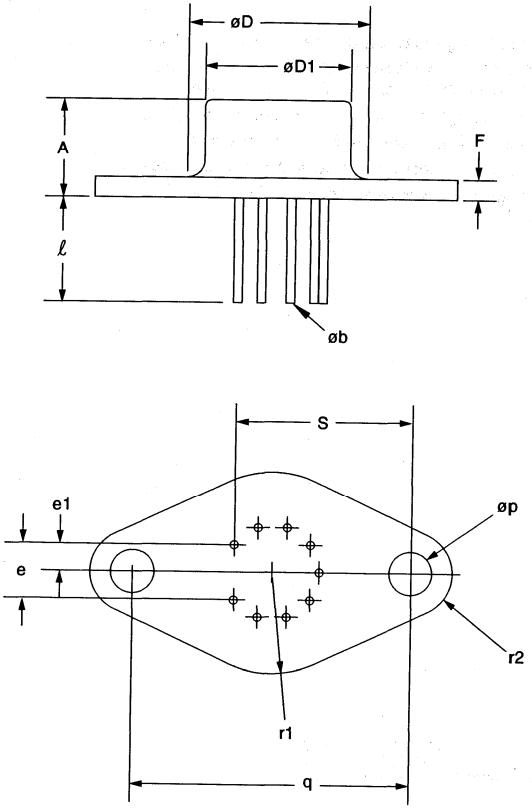


Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
e	.200 BSC		5.08 BSC		
e1	.100 BSC		2.54 BSC		
F	—	.040	—	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	—	.050	—	1.27	1
L2	.250	—	6.35	—	1
Q	.010	.045	.25	1.14	
α	45° BSC		45° BSC		

Notes:

1. (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) –.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tab.
4. The product may be measured by direct methods or by gauge.
5. All leads – increase maximum limit by .003 (.08mm) when lead finish is applied.

9 Lead Metal Can IC Header



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.250	.340	6.35	8.64	
øb	.028	.034	.71	.86	1
øD	—	.620	—	15.75	
øD1	.470	.500	11.94	12.70	
e	.190	.210	4.83	5.33	
e1	.093	.107	2.36	2.72	
F	.050	.075	1.27	1.91	
ℓ	.360	—	9.14	—	
øp	.142	.152	3.61	3.86	
q	.958	.962	24.33	24.43	
r1	—	.350	—	8.89	
r2	—	.145	—	3.68	
S	.570	.590	14.48	14.99	

Notes:

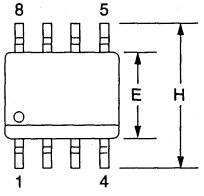
1. All leads—increase maximum limit by .003 (.08mm) when lead finish is applied.

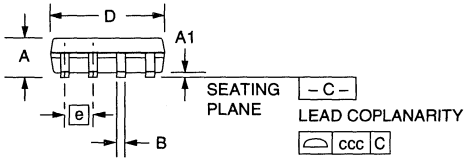
8 Lead Small Outline IC (SOIC) – .150" Body Width

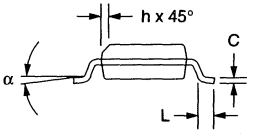
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.





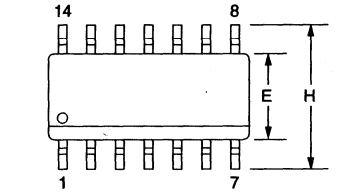


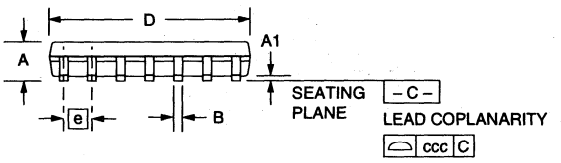
14 Lead Small Outline IC (SOIC) – .150" Body Width

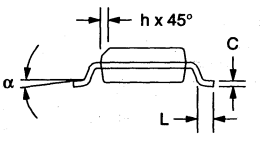
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







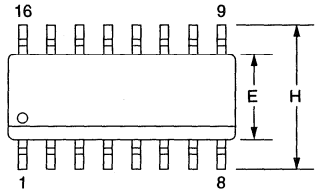
PACKAGING

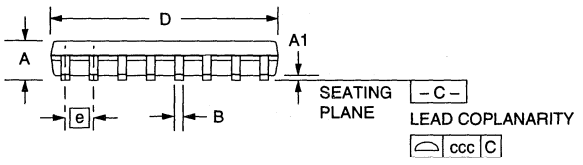
16 Lead Small Outline IC (SOIC) – .150" Body Width

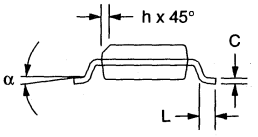
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.





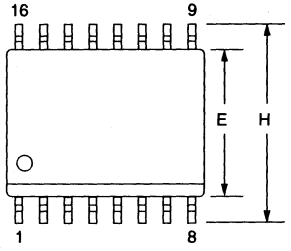


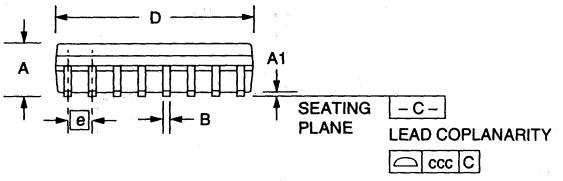
16 Lead Small Outline IC (SOIC) – .300" Body Width

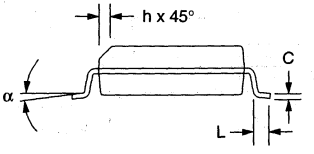
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.398	.413	10.10	10.50	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.





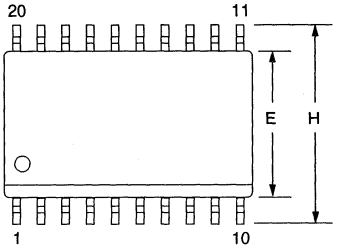


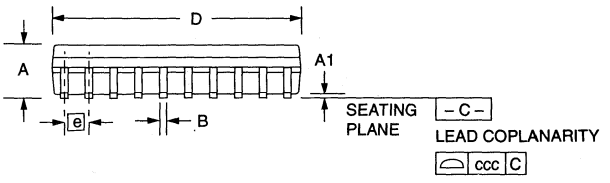
20 Lead Small Outline IC (SOIC) – .300" Body Width

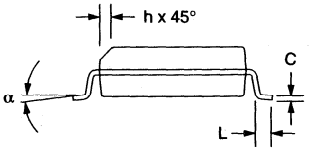
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.

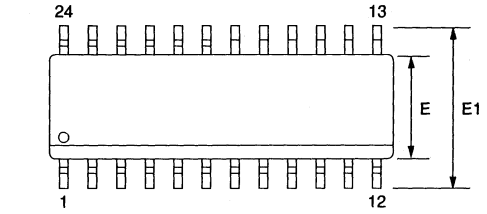


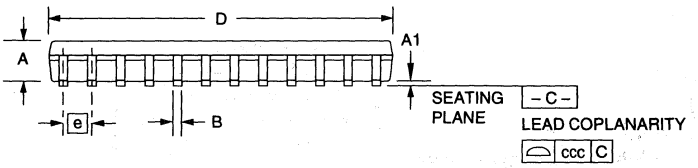


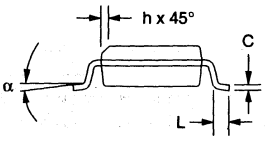


24 Lead Small Outline IC (SOIC) – 5.4mm Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.067	.075	1.70	1.90	
A1	.004	.012	0.10	0.31	
B	.014	.020	0.36	0.51	
C	.006	.012	0.15	0.30	
D	.587	.610	14.90	15.50	
E	.205	.220	5.20	5.60	
E1	.295	.319	7.50	8.10	
e	.050 BSC		1.27 BSC		
h	.010	.020	0.25	0.50	
L	.016	.050	0.41	1.27	
N	24		24		
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	







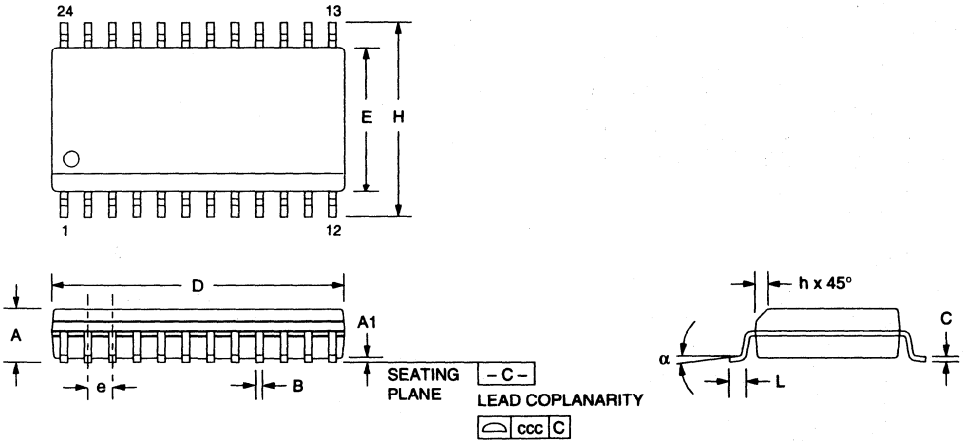
PACKAGING

24 Lead Small Outline IC (SOIC) – .300" Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.599	.614	15.20	15.60	2
E	.290	.299	7.36	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.

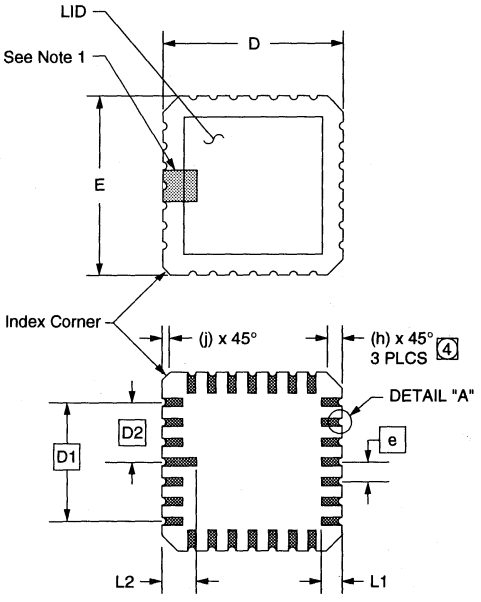


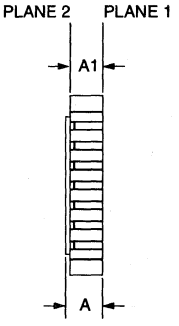
28 Lead Leadless Chip Carrier (LCC)

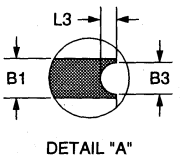
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.060	.100	1.52	2.54	3, 6
A1	.050	.088	1.27	2.24	3, 6
B1	.022	.028	.56	.71	2
B3	.006	.022	.15	.56	2, 5
D/E	.442	.460	11.23	11.68	
D1/E1	.300 BSC		7.62 BSC		
D2/E2	.150 BSC		3.81 BSC		
e	.050 BSC		1.27 BSC		
h	.040 REF		1.02 REF		4
j	.020 REF		.51 REF		4
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.91	2.41	
L3	.003	.015	.08	.38	5
ND/NE	7		7		
N	28		28		

Notes:

1. The index feature for terminal 1 identification, optical orientation or handling purposes, shall be within the shaded index areas shown on planes 1 and 2. Plane 1 terminal 1 identification may be an extension of the length of the metallized terminal which shall not be wider than the B1 dimension.
2. Unless otherwise specified, a minimum clearance of .015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.).
3. Dimension "A" controls the overall package thickness. The maximum "A" dimension is the package height before being solder dipped.
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing. The index corner shall be clearly unique.
5. Dimension "B3" minimum and "L3" minimum and the appropriately derived castellation length define an unobstructed three dimensional space traversing all of the ceramic layers in which a castellation was designed. Dimension "B3" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dripping.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.





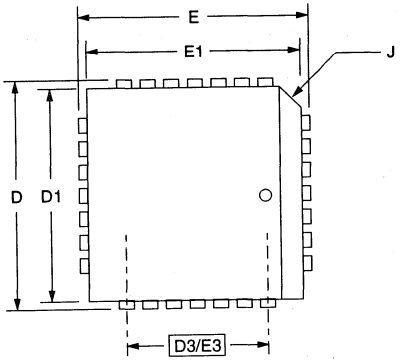


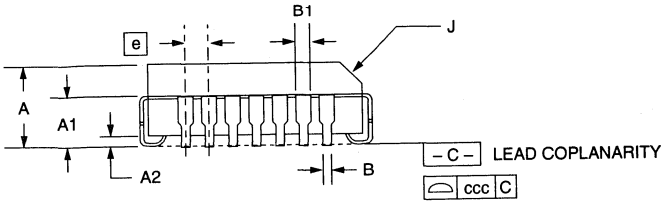
28 Lead Plastic Leaded Chip Carrier (PLCC)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



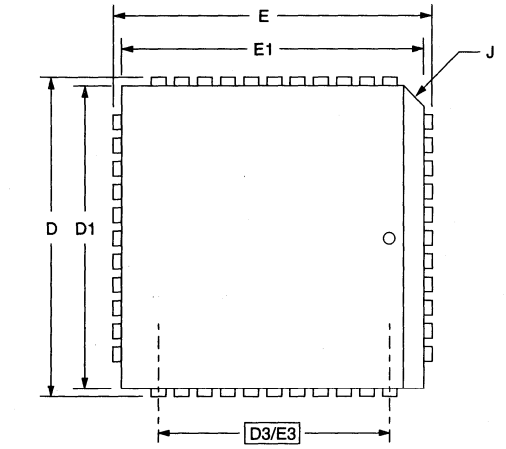


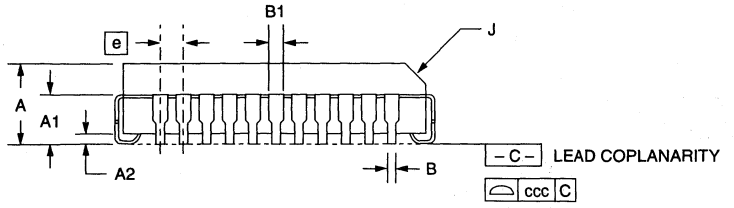
44 Lead Plastic Leaded Chip Carrier (PLCC)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.685	.695	17.40	17.65	
D1/E1	.650	.656	16.51	16.66	3
D3/E3	.500 BSC		12.7 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	11		11		
N	44		44		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



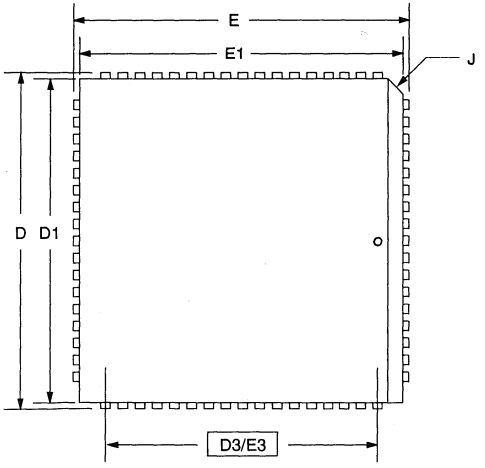


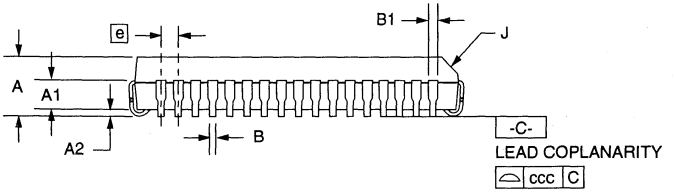
68 Lead Plastic Leaded Chip Carrier (PLCC)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.200	4.19	5.08	
A1	.090	.130	2.29	3.30	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.985	.995	25.02	25.27	
D1/E1	.950	.958	24.13	24.33	3
D3/E3	.800 BSC		20.32 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	17		17		
N	68		68		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



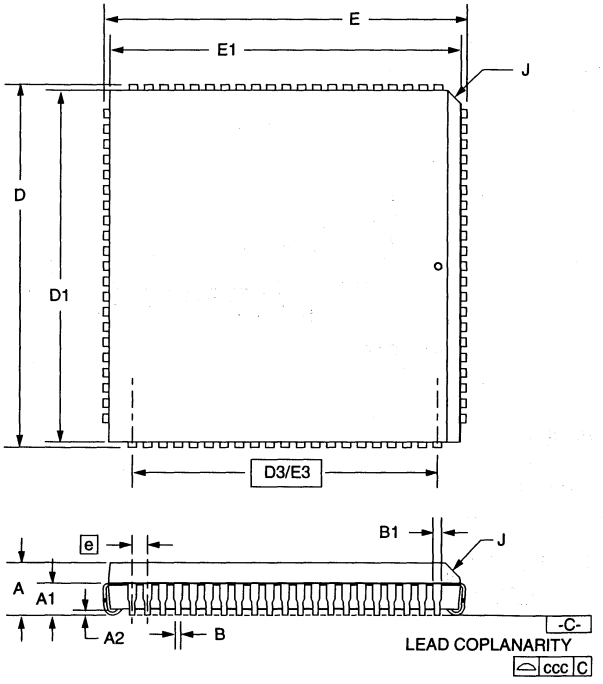


84 Lead Plastic Leaded Chip Carrier (PLCC)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.200	4.19	5.08	
A1	.090	.130	2.29	3.30	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	1.185	1.195	30.10	30.35	
D1/E1	1.150	1.158	29.21	29.41	3
D3/E3	1.000 BSC		25.40 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	21		21		
N	84		84		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Corner and edge chamfer = 45°.
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm).

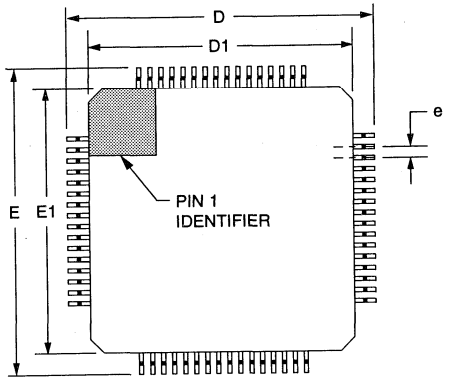


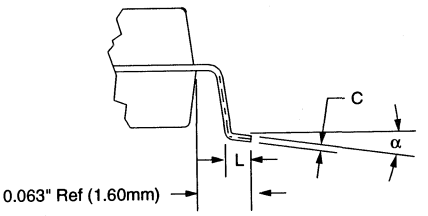
64 Lead Metric Quad Flat Pack (MQFP)

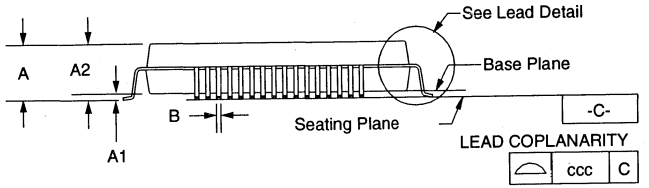
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.096	—	2.45	
A1	.010	—	.25	—	
A2	.077	.083	1.95	2.10	
B	.007	.011	.17	.27	7
D/E	.510	.530	12.95	13.45	
D1/E1	.390	.398	9.90	10.10	2
e	.020 BSC		.50 BSC		
L	.031	.040	.78	1.03	6
N	64		64		4
ND	16		16		5
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion.
3. Pin 1 identifier is optional.
4. Dimension N: number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. "B" includes lead finish thickness.





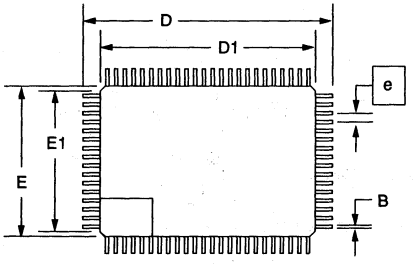


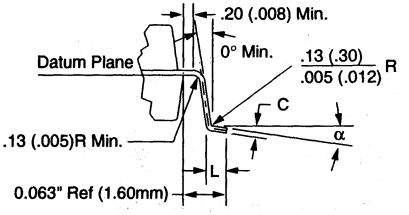
80 Lead Metric Quad Flat Pack (MQFP)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.134	—	3.40	
A1	.010	—	.25	—	
A2	.100	.120	2.55	3.05	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D	.904	.923	22.95	23.45	
D1	.783	.791	19.90	20.10	
E	.667	.687	16.95	17.45	
E1	.547	.555	13.90	14.10	
e	.0315 BSC		.80 BSC		
L	.028	.041	.73	1.03	4
N	80		80		
ND	24		24		
NE	16		16		
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

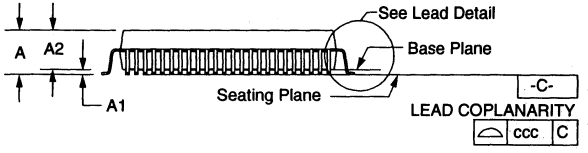
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail

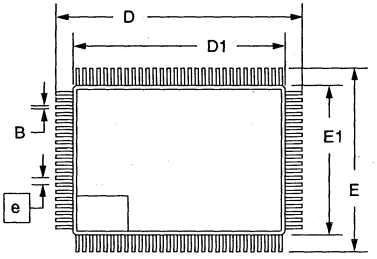


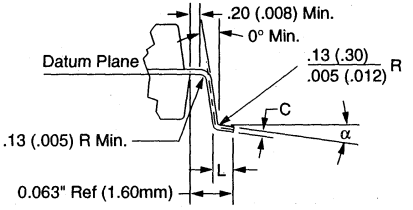
100 Lead Metric Quad Flat Pack (MQFP)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.134	—	3.40	
A1	.010	—	.25	—	
A2	.100	.120	2.55	3.05	
B	.009	.015	.23	.38	3, 5
C	.005	.009	.13	.23	5
D	.904	.923	22.95	23.45	
D1	.783	.791	19.90	20.10	
E	.667	.687	16.95	17.45	
E1	.547	.555	13.90	14.10	
e	.0256 BSC		.65 BSC		
L	.025	.037	.65	.95	4
N	100		100		
ND	30		30		
NE	20		20		
α	0°	7°	0°	7°	
ccc	—	.004	—	.10	

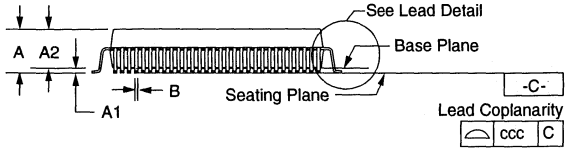
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail

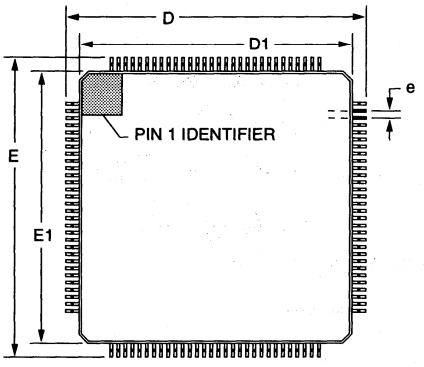


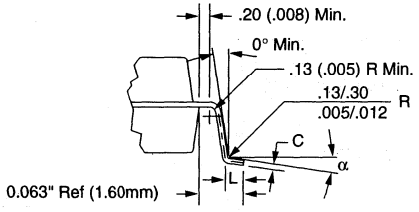
120 Lead Metric Quad Flat Pack (MQFP)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.154	—	3.92	
A1	.010	—	.25	—	
A2	.125	.144	3.17	3.67	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.026	.037	.65	.95	4
N	120		120		
ND	30		30		
α	0°	7°	0°	7°	
ccc	—	.004	—	.10	

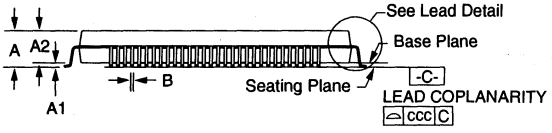
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail

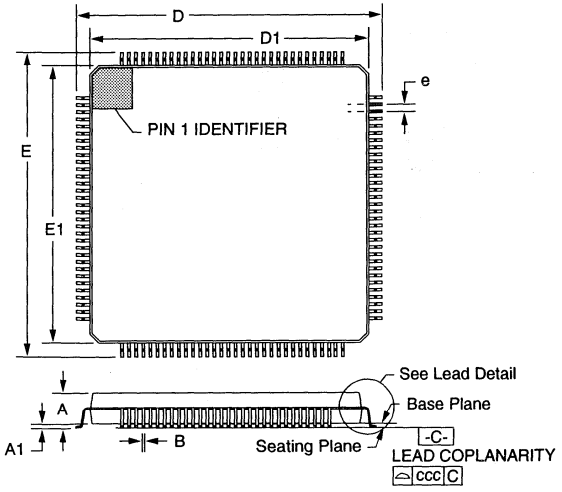


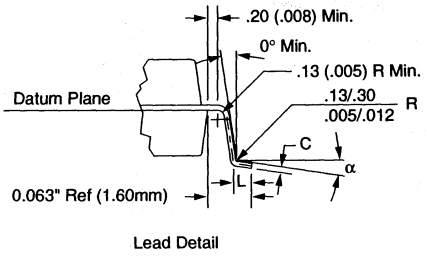
128 Lead Metric Quad Flat Pack (MQFP)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.160	—	4.07	
A1	.010	—	.25	—	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.029	.041	.73	1.03	4
N	128		128		
ND	32		32		
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail

Quality & Reliability

Raytheon's Commitment to Customers

Raytheon Semiconductor is dedicated to providing innovative high performance mixed-signal semiconductor products.

The company has embraced the Total Quality Management (TQM) concept for continuously improving its products and services.

Raytheon Semiconductor maintains relationships which are based upon integrity, open communication and commitment to mutually beneficial, long term business partnerships with its customers and suppliers.

Our definition of quality is meeting customer requirements 100% of the time. The responsibility for this quality is shared by all employees.

With these commitments in mind, the Division has developed a comprehensive Quality/Reliability Policy Manual. Raytheon welcomes the opportunity to discuss these policies with its customers and suppliers, and solicits their questions, comments and/or recommendations for improvement.

Reliability Concepts

Reliability is defined as the probability that product will perform its intended function for a specified period of time. The reliability model generally assumed for Integrated Circuits is that the failure rate over time follows a "bathtub" curve.

This model predicts an early "infant mortality" period where the failure rate is controlled by extrinsic defects. After these initial failures occur, the failure rate is essentially random and depicts the useful life of the product. In this region of the curve a prediction of the Failure rate In Time can be made, expressed as FITs (assuming a constant failure rate). The "bathtub" curve also predicts a final period in the product life where the failure rate is controlled by wear-out mechanisms inherent in the device construction.

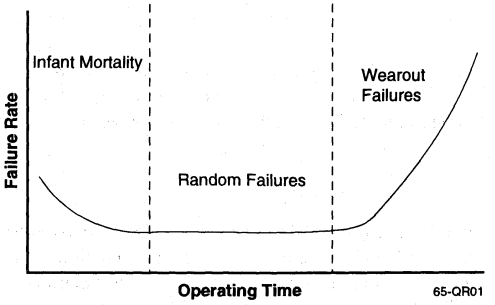


Figure 1. Failure Rate vs. Time

Integrated circuits have demonstrated characteristically long product lifetimes. In order to estimate the reliability of these products, it is necessary to understand extrinsic and intrinsic failure mechanisms and to accelerate possible "useful life" failures. Physical and environmental testing allows an understanding of potential defects contributing to early failures. For extended life prediction, the Arrhenius Model is used to extrapolate from accelerated testing of the product to useful field life.

The Arrhenius Model was originally developed to describe temperature accelerated chemical reaction rates, and is used to predict time/temperature relationship of Integrated Circuit failure rates. Increased temperature operation is one method of accelerating failure. The Arrhenius Model predicts an exponential relationship of temperature and intrinsic failure rate. Using failure statistics obtained from high temperature operation, the failure rate of the process can be estimated and extrapolated to a specified operating temperature range for the product family. An "activation energy" for the expected failure mechanism is used for this estimate of the expected failure rate under use conditions.

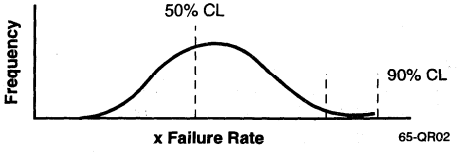


Figure 2. Frequency vs. Failure Rate

The infant mortality and random failures periods can be described through a series of probability calculations. The probability of having a failure at a specific point in time can be expressed by the equation:

$$P_O = e^{-xt}$$

where:

x = the failure rate (failures per unit time)
t = time

The failure rate "x" is usually expressed in % failures per 1000 hours and is sometimes expressed as a mean time between failures (MTBF) through the expression:

$$MTBF = \frac{1}{\text{Failure Rate}}$$

Since the data for the failure rate calculations is derived from a sample of devices from a production lot, a confidence level number is usually stated for the failure rate estimation. A 60% confidence level (CL) is used for the purposes of these calculations.

The failure rate "x" is calculated by using a Chi square (χ^2) distribution through the equation:

$$c = \frac{\chi^2 (x.2r + 2)}{2nt}$$

where:

x = 100-%CL/100
r = number of rejects
n = total number of devices
t = time

The number of failures over a period of time (x) is critical in determining an accurate failure rate number. If only device failures at room or operating temperatures were counted, it would take a large number of failures over a long period of time to gather sufficient data. Therefore, accelerated test methods using elevated temperatures are used. Temperature is used to accelerate failures in a device and the increase can be expressed in a form of the Arrhenius equation which states that the reaction rate increases exponentially with temperature.

$$R = R_O \, e^{\frac{-E}{kT}}$$

where:

R = reaction rate as a function of time and temperature
R_O = constant related to temperature
T = Kelvin temperature
E = activation energy (electron volts)

When this equation is plotted, as shown in Figures 3 and 4, it can be used to determine the failure rate at temperatures other than the test temperature of the device.

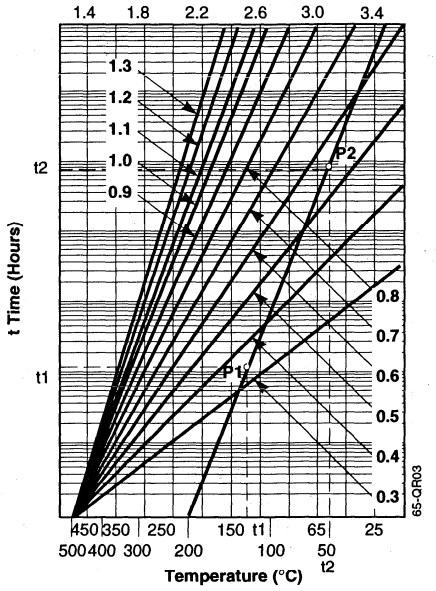


Figure 3. Normalized Time-Temperature Regressions for Various Activation Energy Values (1000°K)

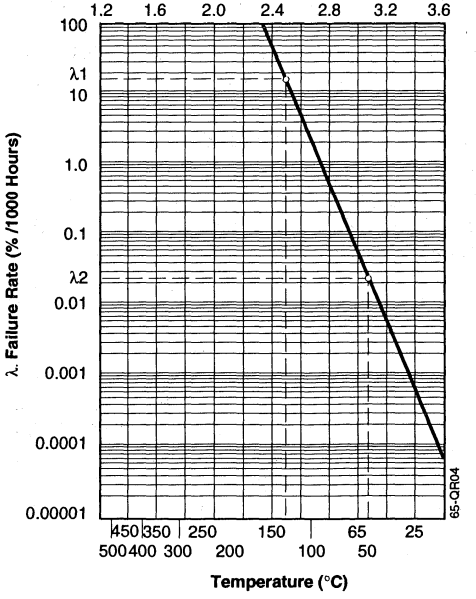


Figure 4. Failure Rate (1000°K)

Table 1. Group A Electrical Tests for Class B Devices[1]

Subgroups[2] Quality/Accept No. = 116/0[3, 4]	
Subgroup 1	Static tests at 25°C
Subgroup 2	Static tests at maximum rated operating temperature
Subgroup 3	Static tests at minimum rated operating temperature
Subgroup 4	Dynamic tests at 25°C
Subgroup 5	Dynamic tests at maximum rated operating temperature
Subgroup 6	Dynamic tests at minimum rated operating temperature
Subgroup 7	Functional tests at 25°C
Subgroup 8A	Functional tests at maximum rated operating temperatures
Subgroup 8B	Functional tests at minimum rated operating temperatures
Subgroup 9	Switching tests at 25°C
Subgroup 10	Switching tests at maximum rated operating temperature
Subgroup 11	Switching tests at minimum rated operating temperature

Notes:

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.
2. The applicable tests required for group A testing (see 1/) may be conducted individually or combined into sets of tests, subgroups (as defined in Table 1), or sets of subgroups.
3. The sample plan (quantity and accept number) for each test shall be 116/0.
4. If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

Table 2. Group B Tests for Class B[1,2]

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 2[3] a. Resistance to solvents	2015		3(0)
Subgroup 3 a. Solderability[4]	2022 or 2003	Soldering temperature of 245 ±5°C	10
Subgroup 5 a. Bond strength[5] 1. Thermocompression 2. Ultrasonic or wedge 3. Flip-chip 4. Beam Lead	2011	 1. Test condition C or D 2. Test condition C or D 3. Test condition F 4. Test condition H	

Notes:

1. Post burn-in electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.
2. Subgroups 1, 4, 6, 7, and 8 have been deleted from this table. For convenience, the remaining subgroups will not be renumbered.
3. Resistance to solvents testing required only on devices using inks or paints as the marking or contrast medium.
4. All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.
5. Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see Method 2011).

Table 3. Group C (Die-Related Tests—For Class B Only)

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 1 a. Steady-state life test b. End-point electrical parameters	1005	Test condition to be specified (1,000 hours at 125°C or equivalent in accordance with Table 1)	5

Table 4. Group D (Package Related Tests)

Test	MIL-STD-883 Method	MIL-STD-883 Condition	Quantity/ (Accept No.) or LTPD
Subgroup 1[1]			
a. Physical dimensions	2016		15
Subgroup 2[1]			
a. Lead integrity[2]	2004	Test condition B_2 (lead fatigue)	5
b. Seal[3]			
1. Fine	1014	As applicable	
2. Gross			
Subgroup 3[4]			
a. Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum	15
b. Temperature cycling		Test condition C, 100 cycles minimum	
c. Moisture resistance[5]	1010		
d. Seal	1004	As applicable	
1. Fine	1014		
2. Gross			
e. Visual examination		In accordance with visual criteria of Method 1004 & 1010	
f. End-point electrical parameters[6]		As specified in the applicable device specification	
Subgroup 4[4]			
a. Mechanical shock	2002	Test condition B minimum	15
b. Vibration, variable frequency	2007	Test condition A minimum	
c. Constant acceleration			
d. Seal	2001	Test condition E minimum (see 3), Y_1 orientation only	
1. Fine	1014	As applicable	
2. Gross			
e. Visual examination[7]			
f. End-point electrical parameters		As specified in the applicable device specification	
Subgroup 5[1]			
a. Salt atmosphere[5]	1009	Test condition A minimum	15
b. Seal	1014	As applicable	
1. Fine			
2. Gross			
c. Visual examination		In accordance with visual criteria of Method 1009	
Subgroup 6[1]			
a. Internal water-vapor content[8]	1018	5,000 ppm maximum water content at 100°C	3(0) or 5(1)
Subgroup 7[1]			
a. Adhesion of lead finish[9,10]	2025		15
Subgroup 8			
a. Lid torque[1]	2024		5(0)

Notes:

1. Electrical reject devices from that same inspection lot may be used for samples.
2. For leadless chip carrier packaged only, use test condition D. For leaded chip carrier packages, use condition B1. For pin grid array and other rigid leads use Method 2038.
3. Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.
4. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
5. Lead bend stress initial conditioning is not required for leadless chip carrier packages.
6. End-point electrical parameters are performed after moisture resistance and prior to seal test.
7. Visual examination shall be in accordance with Method 1010 or 1011.
8. Test three devices; if one fails, test two additional devices with no failures. At the manufacturers option, if the initial test sample (i.e., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with 5 additional devices from the same lot.
9. The adhesion of lead finish test shall not apply to leadless chip carrier packages.
10. LTPD based on number of leads.

Table 5. Typical Qualification Plan for Hermetic Packaged Devices[1, 2, 3]

Test	Conditions Per MIL-STD-883	Quantity	Accept No.
Group B			
Subgroup 3		15	0
Solderability	245 5°C		
Subgroup 5		15	0
Bond Strength	Condition C and record bond pull strength		
Group C			
Subgroup 1	168-hour point will be used to screen out the infant mortality failure. The sample size after the 168-hour point will be 77.	77	1
Operational Life (168, 250, 500, 1000, 2000)			
Electrical Test (25°C DC)			
(2 date codes, 77 samples each)			
Group D			
Subgroup 2		25	1
Lead Integrity	Condition B_2		
F&G Leak			
Lid Torque			
Subgroup 4		25	1
Mechanical Shock	Condition B		
Vibration	Condition A		
Constant Acceleration	Condition B Min.		
F&G Leak			
Visual Examination			
Electrical test 25°C			

Notes:

1. The above group B, C, D are run completely, if the product (package and die) has no history.
2. If the package is pre-qualified, then only Group C, Subgroups 1 and 2, and Group D, Subgroup 4 are conducted.
3. If the product is not JAN or 883 compliant, then 168-hour pre-burn in is not performed to screen out infant mortality prior to Group C Test.

Table 6. Typical Qualification Plan for Plastic Package Devices

Test	Test Conditions	Purpose of Test	Sample Size	Accept No.
Operating Life	Temperature 125°C Time 1000 hrs. Electrical Test at 168 hrs., 500 hrs., 1000 hrs., 250 hrs. Bias—per spec requirements	Accelerated Life	45	0
Autoclave	Pressure 15 PSiG Temperature 121°C, >95° RH Electrical Test at 96 hrs., (no metal deterioration), 144 hrs., 250 hrs., 500 hrs.	Package integrity and moisture resistance	45	0
85°C/85% RH	Temperature 85°C Humidity 85% Time 1000 hrs. (no metal deterioration) Electrical Test at 168 hrs.,	Accelerated life corrosion resistance	45	0
	Bias—None Electrical Test at 144 hrs., 250 hrs., 500 hrs.	temperature storage		
Temperature Cycle	Temperature -65°C to +150°C No. Cycles 100 Electrical Test 25°C	Determine the resistance to high and low temperatures	45	0
Thermal Shock	Per 883 Method 1011	Determine resistance to rapid temperature change.	45	0
Moisture (10 Day)	Temperature -10°C to +65°C Humidify 90% RH Time 240 hrs. Electrical Test at 240 hrs. Visual Inspection of Leads	Package integrity to moisture, lead corrosion, etc.	45	0
Solderability	Per 883, Method 2003	To determine the solderability of the lead finish	3	0
Lead Fatigue	Per 883, Method 2004 Condition B	To determine the physical resistance to lead bending fatigue	3	0
External Visual	10-30X Magnification	To evaluate physical construction and processing results to package and lead frame	45	0

*2 date codes of 50 each

Reliability Program

The quality and reliability activity at Raytheon is a thorough and continuous activity. It starts with initial design concepts and processes, and carries through to the finished product.

Reliability Engineering, working with Design and Product Engineering, monitors the new device design or process through all stages of development and remains the full and final authority over the qualification status of all products.

Raytheon's established RA Qualification plans are used to approve new devices, processes or manufacturing facilities. Two examples are shown in Tables 5 and 6 for hermetic package devices and plastic package devices.

The Reliability Department continually monitors all product lines through product sampling, routine re-qualification and QCI testing of JAN and other Hi-Rel products to evaluate failure modes and failure rates. The results from these tests are reviewed with Product and Production Engineering and any necessary corrective actions are taken.

Lab Facilities

Raytheon maintains a fully equipped laboratory to conduct its reliability, failure analysis, and environmental testing. The typical types of tests that are performed by this facility include:

- QCI Groups A, B, C and D environmental requirements
- Destructive Physical Analysis
- SEM Analysis
- Microprobe Analysis/Laser Cutter
- X-ray Dispersion Analysis
- Biased 85/85 and Steam Pressure Pot (PCT)
- Highly Accelerated Stress Testing (HAST)
- Electromigration Characterization
- TDDB Testing of MOS Gate Oxide
- Hot Carrier Degradation
- ESD Testing
- PIND Testing

Plastic Package Device Monitor

Raytheon is a major supplier of standard and ASIC products in plastic packages. Products are available in a variety of plastic packages such as DIPs, SOICs, and LCCs. Significant investments have been made in both the technology and manufacture of high-reliability, low-stress plastic encapsulated packages.

In addition to quality control check point inspection at every assembly step, reliability process monitoring (see Table 7) is performed.

The autoclave (steam pressure) test determines the package's moisture resistance in the shortest possible time, allowing immediate corrective action where necessary, thus ensuring the long-term reliability of the products.

All products are 100% electrically tested and visually screened followed by sample testing for electrical, visual and mechanical defects to determine the outgoing PPM defect rate. With a quality goal of 100 ppm or less, Raytheon's devices have failure rates well below the industry standards.

Table 7. Typical Plastic Process Monitor Tests

Test	Purpose of Test
Autoclave (steam pressure)	To evaluate the resistance of moisture penetration of the package and the effects of moisture on the chip under accelerated conditions of 15 pounds of steam pressure at 120°C.
Biased 85°C/85% RH	To evaluate the operational life and resistance to moisture penetration of the chip and the plastic package under the accelerated conditions of 85°C and 85% relative humidity.
Operating Life	To evaluate the operational field life of the device under accelerated conditions of 125°C.
Resistance to Solvents	To determine that the brand markings will not become illegible on the package parts when subjected to the solvents and test per MIL-STD-883C, Method 2015.
Solderability	Per Method 2004 of MIL-STD-883.
External Visual	To determine the physical construction and processing results to the package and lead frame at 30X magnification.
Lead Fatigue	To determine the physical resistance to lead bending fatigue per Condition B, Method 2004, of MIL-STD-883.
Thermal Shock	To determine that the device can survive exposure to rapid changes in temperature from -55°C to +125°C per Condition B of Method 1011 of MIL-STD-883.

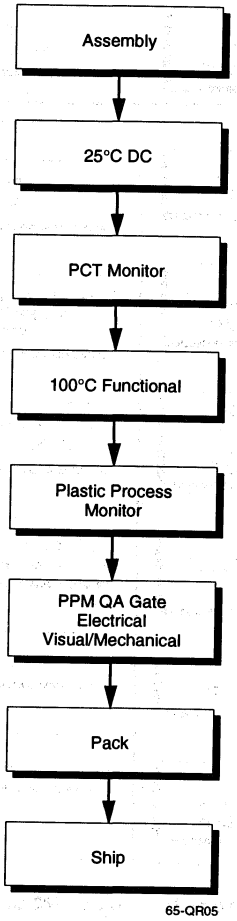


Figure 5. Linear Plastic Flow Chart

Major Programs

Raytheon Semiconductor is involved in major programs which require and support a high level of quality and reliability expertise in the design, manufacture and control of our products.

The commercial programs address such market segments as computers and automotive. These markets are a driving force within Raytheon's commercial product quality and reliability controls.

The most significant military program is JAN 38510 which requires a Defense Electronics Supply Center (DESC) certification of our fabrication and manufacturing lines. The JAN military specifications and MIL-I-45208 form the foundation of our QA system, thereby benefiting all products—JAN, 883 compliant, DESC Standard Military Drawings (SMD), Source Control Drawings (SCD), and commercial.

An extensive statistical process control program has been initiated which includes wafer fabrication processing, quality assurance monitors, assembly monitors, environmental screening and electrical testing.

Internal Audit Program

Raytheon Semiconductor maintains an internal audit program which requires the auditing of all product processing and control systems. This audit verifies conformance to manufacturing and quality procedures identifying areas needing improvement and enhancement.

Process Monitors

Extensive process monitors in fab, assembly and electrical test are a critical part of Raytheon's quality program. These enable early detection of process problems as well as characterization of process improvements.

Reliability Monitor

The Reliability Monitor Program monitors, on a continuing basis, the reliability of all IC products in hermetic and plastic packages. This program requires that periodically several different part types from each microcircuit technology group as detailed in Appendix E of MIL-M-38510 be evaluated to the MIL-STD-883 Test Method 5005 Groups A, B, C and D test requirements. The data generated from this program provide a basic library of reliability information on many product types and is used to provide Quality Conformance Inspection (QCI) data to meet customer-specific group test data requirements.

Military Programs

JAN-MIL-M-38510

Raytheon's foremost commitment is to the JAN MIL-M-38510 program which is administered by the Defense Electronics Supply Center (DESC) and the Defense Logistics Agency (DLA) of the Department of Defense. We maintain DESC certified wafer fabrication, assembly and test facilities which allow us to provide an extensive number of JAN QPL device types.

The JAN 38510 program is designed to provide a consistently high reliability hermetic product manufactured to a standard process flow and quality/reliability program as defined in MIL-M-38510, MIL-STD-976 and MIL-STD-883 and the resulting baselines.

A JAN device is identified and branded with a unique part number as shown in Figure 7 and Table 8. The device is also branded with our manufacturers' designating symbol (CORP or RP), logo (RAY or R), the sealing cycle date code, country of origin, a two-digit fab quarter code (indicating year and quarter in which die fabrication was completed, and the applicable electrostatic discharge sensitivity identifier.

A current listing of Raytheon's JAN 38510 QPL devices may be obtained by contacting the nearest Raytheon Field Sales Office.

883 Compliant

The 883 compliant program offers hermetic products assembled and tested to the requirements of paragraph 1.2.1 of MIL-STD-883 for Class B devices. With Raytheon as the qualifying activity and offshore assembly permissible, these devices are as close as one can get to JAN 38510 reliability using a standard process flow (see Figure 6).

Raytheon's 883 compliant program is complemented by our active participation in DESC's Standard Military Drawing program.

A current listing of our 883 compliant devices which includes those DESC SMDs for which Raytheon is an approved source of supply may be obtained by contacting the nearest Raytheon Semiconductor Field Sales Office.

Lead Finish

Raytheon offers two lead finished—solder dipped and matte tin plate (non-JAN only). The preferred and recommended lead finish is solder which is tin plated prior to dipping.

Raytheon offers a solder lead finish that will meet the solderability requirements of MIL-M-38510.

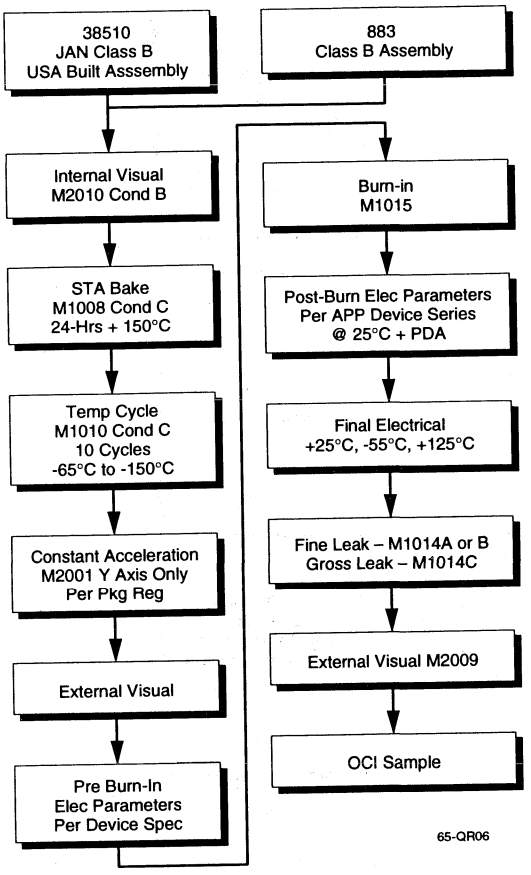


Figure 6. Screening for JAN and 883 Compliant Devices

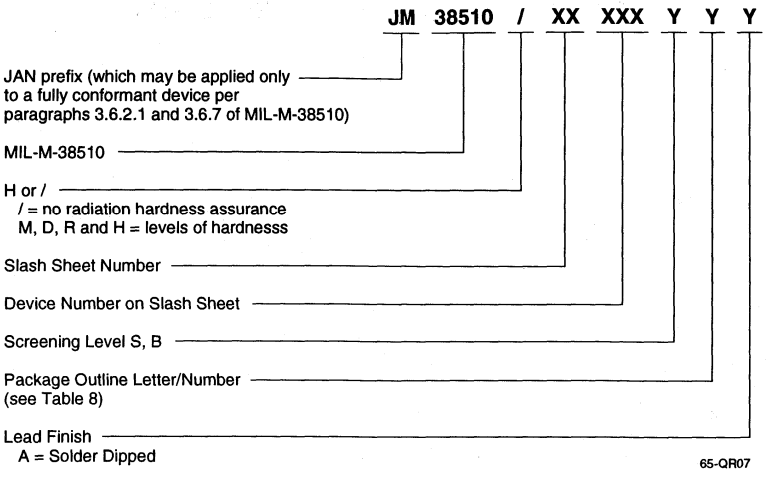


Figure 7. MIL-M-38510 Part Marking

Table 8. JAN Package Codes

38510 Outline Letter/Number	38510 Type Designation	Description
A	F-1	14-lead, 1/4 x 1/4 Cerpak
B	F-3	14-lead, 3/16 x 1/4 Cerpak
C	D-1	14-lead, 1/4 x 3/4 Cerdip
D	F-2	14-lead, 1/4 x 3/8 Cerpak
E	D-2	16-lead, 1/4 x 7/8 Cerdip
F	F-5	16-lead, 1/4 x 7/8 Cerpak
G	A-1	8-lead, TO-99 can
H	F-4	10-lead, 1/4 x 1/4 Cerpak
I	A-2	10-lead, TO-100 can
J	D-3	24-lead, 1/2 x 1-1/4 Cerdip
K	F-6	24-lead, 3/8 x 5/8 Flatpak
L	D-9	24-lead, 1/4 x 1-1/4 Cerdip
P	D-4	8-lead, 1/4 x 3/8 Cerdip
Q	D-5	40-lead, 2 x 5/8 DIP
R	D-8	20-lead, 1/4 x 1-1/16 Sidebraze DIP
S	F-9	20-lead, 1/4 x 1/2 Cerpak
V	D-6	18-lead, 1/4 x 5/16 Cerdip
2	C-2	20-terminal, 3/8 x 3/8 Chip Carrier
3	C-4	28-terminal, 1/2 x 1/2 Chip Carrier

THIS PAGE INTENTIONALLY LEFT BLANK

Headquarters

Mountain View
350 Ellis Street
Mountain View, CA 94043
TEL: 415-968-9211
FAX: 415-966-7742

San Diego
5580 Morehouse Drive
San Diego, CA 92121
TEL: 619-457-1000
FAX: 619-455-6314

Regional Sales Offices

Florida
130 Ridgewood Drive
Longwood, FL 32779
TEL: 407-682-6988
FAX: 407-682-6404

Maryland
8312 Spring Breeze Court
Ellicott City, MD 21043
TEL: 410-465-7718
FAX: 410-465-8390

Massachusetts
31 Summer Street
Chelmsford, MA 01824
TEL: 508-256-1381
FAX: 508-256-1736

New Hampshire
42 Red Deer Road
Londonderry, NH 03053
TEL: 603-434-6383
FAX: 603-434-6395

35 Pinehurst Avenue
Nashua, NH 03062
TEL: 603-888-1326
FAX: 603-888-4239

New York
59 Cardinal Street
Pearl River, NY 10965
TEL: 914-620-1326
FAX: 914-620-0951

Pennsylvania
116 Sussex Place
Berwyn, PA 19312
TEL: 610-640-4057
FAX: 610-640-4058

International Sales Offices

Europe
Robinson Way, Anchorage Park,
Portsmouth, Hampshire POS 5TD
England
TEL: 011-44-1705-665555
FAX: 011-44-705-663355

Asia
4-8-22f Nishi Azabu
Minato-ku, Tokyo 106
Japan
TEL: 011-81-3-3406-5998
FAX: 011-81-3-3406-5998

North American Representatives

Alabama
EMA
309 Jordan Lane, NW
Huntsville, AL 35805
TEL: 205-830-4030
FAX: 205-830-1947

Alaska
See Raytheon Headquarters Office, Mountain View

Arizona
D & L TECHNICAL SALES INC.
6139 S. Rural Road, #102
Tempe, AZ 85283
TEL: 602-730-9553
FAX: 602-730-9647

Arkansas
See Raytheon Regional Sales Office, Florida

California
1ST REP OF SOUTHERN CALIFORNIA
143 Triunfo Canyon, Suite #222
Westlake Village, CA 91361
TEL: 805-373-0887
FAX: 805-495-1317

K.S.A.
6150 Lusk Blvd. Ste. B-200
San Diego, CA 92121
TEL: 619-453-5720
FAX: 619-453-1695

ZEUSTEC SALES, INC.
4655 Old Ironsides Drive
Suite 385
Santa Clara, CA 95054
TEL: 408-987-0165
FAX: 408-987-0169

Colorado
WESCOM MARKETING
4860 Ward Road
Wheat Ridge, CO 80033
TEL: 303-422-8957
FAX: 303-422-9892

Connecticut
DATA MARK, INC.
2514 Boston Post Road
Unit #7C
Guilford, CT 06437
TEL: 203-453-0575
FAX: 203-453-5935

Florida
See Raytheon Regional Sales Office, Florida

Georgia
EMA
1160 Grimes Bridge Road
Suite G
Roswell, GA 30075
TEL: 770-992-7240
TEL: 800-647-3773
FAX: 770-993-3426

Hawaii
See Raytheon Headquarters Office, Mountain View

Idaho
ES/CHASE COMPANY, INC.
12025 115th Ave, NE
Suite #200
Kirkland, WA 98034
TEL: 206-823-9535
FAX: 206-821-7257

Illinois
T.E.Q. SALES, INC.
920 Davis Road, Suite 304
Elgin, IL 60123
TEL: 708)742-3767
FAX: 708-742-3947

Indiana
VICTORY SALES, INC.
3077 E. 98th St., Suite 135
Indianapolis, IN 46280
TEL: 317-581-0880
FAX: 317-581-0882

Iowa
See Raytheon Regional Sales Office, New York

Kansas
See Raytheon Regional Sales Office, New York

Kentucky
VICTORY SALES, INC.
7333 Paragon Rd.
Suite 210
Centerville, OH 45458
TEL: 513-436-1222
FAX: 513-436-1224

Louisiana
See Raytheon Regional Sales Office, Florida

Maine
See Raytheon Regional Sales Office, Massachusetts

Maryland
MICRO-COMP, INC.
1421 South Caton Avenue
Baltimore, MD 21227-1082
TEL: 410-644-5700
FAX: 410-644-5707
IOS ID: MICROB

Massachusetts
See Raytheon Regional Sales Office, Nashua, NH

Michigan
ELECTRONIC SALESMASTERS, INC.
24100 Chagrin Blvd.
Beachwood, OH 44122
TEL: 216-831-9555
FAX: 216-831-8647

Minnesota
ALDRIDGE ASSOCIATES, INC.
7138 Shady Oak Road
Eden Prairie, MN 55344
TEL: 612-944-8433
FAX: 612-944-8378

Mississippi
EMA
309 Jordan Lane, NW
Huntsville, AL 35805
TEL: 205-830-4030
FAX: 205-830-1947

Missouri
See Raytheon Regional Sales Office, New York

Montana
See Raytheon Headquarters Office, San Diego

Nebraska
See Raytheon Regional Sales Office, New York

Nevada
See Raytheon Headquarters Office, San Diego

New Hampshire
See Raytheon Regional Sales Office, Massachusetts

New Jersey
See Raytheon Regional Sales Office, Pennsylvania

New Mexico
D & L TECHNICAL SALES INC.
6139 S. Rural Road, #102
Tempe, AZ 85283
TEL: 602-730-9553
FAX: 602-730-9647

New York
PI'TRONICS/GEN-TECH
5858 E. Molloy Road
Room 110
Syracuse, NY 13211
TEL: 315-455-7346
FAX: 315-455-2630

PI'TRONICS/GEN-TECH
1623 North Forest Road
Williamsville, NY 14221
TEL: 716-689-2378
FAX: Use Syracuse Office Fax Number

North Carolina
EMA
6604 Six Forks Rd., Suite 204
Raleigh, NC 27615
TEL: 919-846-6888
FAX: 919-847-7360

EMA
2036-202 Sharon Oaks Lane
Charlotte, NC 28210
TEL: 704-365-0547

North Dakota
ALDRIDGE ASSOCIATES, INC.
7138 Shady Oak Road
Eden Prairie, MN 55344
TEL: 612-944-8433
FAX: 612-944-8378

Ohio
ELECTRONIC SALESMASTERS, INC.
24100 Chagrin Blvd.
Beachwood, OH 44122
TEL: 216-831-9555
FAX: 216-831-8647

VICTORY SALES, INC.
7333 Paragon Rd.
Suite 210
Centerville, OH 45458
TEL: 513-436-1222
FAX: 513-436-1224

Oklahoma
See Raytheon Regional Sales Office, Florida

Oregon
ES/CHASE COMPANY, INC.
6655 SW Hampton Street
Suite 120
Tigard, OR 97223
TEL: 503-684-8500
FAX: 503-684-3400

Pennsylvania
See Raytheon Regional Sales Office, Pennsylvania

Puerto Rico
P. C. ELECTRONICS, INC.
Bori St. # 1572
Suite 103, Urb. Caribe
Rio Piedras, PR 00926
TEL: 809-753-9811/753-9805
FAX: 809-753-8345

Rhode Island
See Raytheon Regional Sales Office, Massachusetts

South Carolina
EMA
6604 Six Forks Rd., Suite 204
Raleigh, NC 27615
TEL: 919-846-6888
FAX: 919-847-7360

South Dakota
ALDRIDGE ASSOCIATES, INC.
7138 Shady Oak Road
Eden Prairie, MN 55344
TEL: 612-944-8433
FAX: 612-944-8378

Tennessee
EMA
309 Jordan Lane, NW
Huntsville, AL 35805
TEL: 205-830-4030
FAX: 205-830-1947

Texas
See Raytheon Regional Sales Office, Florida

Utah
WESCOM MARKETING
3500 S. Main Street
Salt Lake City, Utah 84115
TEL: 801-269-0419
FAX: 801-269-0665

Vermont
See Raytheon Regional Sales Office, Massachusetts

Virginia
MICRO-COMP, INC.
8811 Timberlake Road
Lynchburg, VA 24502
TEL: 804-239-2626
FAX: 804-239-1333

Washington
ES/CHASE COMPANY, INC.
12025 115th Ave, NE
Suite #200
Kirkland, WA 98034
TEL: 206-823-9535
FAX: 206-821-7257

Washington, D.C.
MICRO-COMP, INC.
1421 South Caton Avenue
Baltimore, MD 21227-1082
TEL: 410-644-5700
FAX: 410-644-5707
IOS ID: MICROB

West Virginia
MICRO-COMP, INC.
8811 Timberlake Road
Lynchburg, VA 24502
TEL: 804-239-2626
FAX: 804-239-1333

Wisconsin
T.E.Q. SALES, INC.
20720 West Watertown Rd.
Suite 201
Waukesha, WI 53186
TEL: 414-780-0340
FAX: 414-780-0342

Wyoming
See Raytheon Headquarters Office, San Diego

Canada
CANTEC REPRESENTATIVES, INC.
8 Strathearn Ave., No. 18
Brampton, Ontario
Canada L6T 4L9
TEL: 905-791-5922
FAX: 905-791-7940

CANTEC REPRESENTATIVES, INC.
1573 LaPerriere Ave.
Ottawa, Ontario
Canada K1Z 7T3
TEL: 613-725-3704
TWX: 610-562-8967
FAX: 613-725-0490

CANTEC REPRESENTATIVES, INC.
84 Lasalle Street
Ste, Eustache, Quebec
Canada J7R 4P5
TEL: 514-623-5496
FAX: 514-623-5482

North American Distributors

Alabama

ARROW/SCHWEBER ELECTRONICS
1015 Henderson Road
Huntsville, AL 35816
TEL: 205-837-6955
FAX: 205-721-1581

ALL AMERICAN SEMICONDUCTOR
4900 University Square #34
Huntsville, AL 35816
TEL: 205-837-1555
FAX: 205-837-7733

Arizona

ARROW/SCHWEBER ELECTRONICS
2415 West Erie Drive
Tempe, AZ 85282
TEL: 602-431-0030
FAX: 602-431-9555

California

ACI ELECTRONICS
345 Paseo Tesoro
Walnut, CA 91789
TEL: 909-584-1731
FAX: 909-598-6515

ALL AMERICAN SEMICONDUCTOR
230 Devcon Drive
San Jose, CA 95112
TEL: 408-943-1200
TEL: 800-222-6001
FAX: 408-437-8970

ALL AMERICAN SEMICONDUCTOR
10805 Holder Street
Suite 100
Cypress, CA 90630
TEL: 714-229-8600
TEL: 800-831-8300
FAX: 714-229-8603

ALL AMERICAN SEMICONDUCTOR
26010 Mureau Road
Suite 120
Calabasas, CA 91302
TEL: 818-878-0555
TEL: 800-774-1603
FAX: 818-878-0533

ALL AMERICAN SEMICONDUCTOR
6390 Greenwich Dr.
Suite 170
San Diego, CA 92122
TEL: 619-658-0200
FAX: 619-658-0201

ARROW/SCHWEBER ELECTRONICS
9511 Ridgehaven Court
San Diego, CA 92123
TEL: 619-565-4800
FAX: 619-279-0862

ARROW/SCHWEBER ELECTRONICS
1180 Murphy Avenue
San Jose, CA 95131
TEL: 408-441-9700
FAX: 408-453-4810

ARROW PACIFIC
48834 Kato Road, Suite 103
Fremont, CA 94538
TEL: 510-490-9477
FAX: 510-490-1084

ARROW/SCHWEBER ELECTRONICS
26677 West Agoura Road
Malibu Canyon Business Park
Calabasas, CA 91302
TEL: 818-880-9686
FAX: 818-880-4687

ARROW/SCHWEBER ELECTRONICS
6 Cromwell Street, Suite 100
Irvine, CA 92718
TEL: 714-587-0404
FAX: 714-454-4206

ZEUS COMPONENTS, INC.
6276 San Ignacio Avenue
Suite E
San Jose, CA 95119
TEL: 408-629-4689
TEL: 800-366-8360
FAX: 408-629-4792

Colorado

ARROW/SCHWEBER ELECTRONICS
61 Inverness Drive East
Suite 105
Englewood, CO 80112
TEL: 303-799-0258
FAX: 303-799-0730

Connecticut

ARROW/SCHWEBER ELECTRONICS
12 Beaumont Road
Wallingford, CT 06492
TEL: 203-265-7741
FAX: 203-265-7988

ACI
206 Route 80
Killingworth, CT 06417
TEL: 203-663-3311
FAX: 203-663-2373

Florida

ALL AMERICAN SEMICONDUCTOR
16115 NW 52nd Avenue
Miami, FL 33014
TEL: 305-621-8282
FAX: 305-624-5258

ALL AMERICAN SEMICONDUCTOR
1400 E. Newport Center Dr.
Deerfield Beach, FL 33441
TEL: 800-327-6237
FAX: 305-429-0391

ARROW/SCHWEBER ELECTRONICS
400 Fairway Drive
Deerfield Beach, FL 33441
TEL: 305-429-8200
FAX: 305-428-3991

ARROW/SCHWEBER ELECTRONICS
37 Skyline Drive, Bldg. D
Suites 3101, 3102, 3103
Lake Mary, FL 32746
TEL: 407-333-9300
FAX: 407-433-9320

Georgia

ARROW/SCHWEBER ELECTRONICS
4250E River Green Parkway
Duluth, GA 30136
TEL: 404-497-1300
FAX: 404-476-1493

Illinois

ARROW/SCHWEBER ELECTRONICS
1140 West Thorndale Ave.
Itasca, IL 60143
TEL: 708-250-0500
FAX: 708-250-0916

ALL AMERICAN SEMICONDUCTOR
1930 Thoreau, Suite 200
Schaumburg, IL 60173
TEL: 708-852-7707
FAX: 708-852-0263

Indiana

ARROW/SCHWEBER ELECTRONICS
7108 Lakeview Pkwy West Dr.
Indianapolis, IN 46268
TEL: 317-299-2071
FAX: 317-299-2379

Kansas

ARROW/SCHWEBER ELECTRONICS
9801 Lagler Road
Lenexa, KS 66219
TEL: 913-541-9542
FAX: 913-752-2612

Maryland

ALL AMERICAN SEMICONDUCTOR
14636 Rothgeb Drive
Rockville, MD 20850
TEL: 301-251-1205
FAX: 301-251-8574

ARROW/SCHWEBER ELECTRONICS
9800J Patuxent Woods Dr.
Columbia, MD 21046
TEL: 301-596-7800
FAX: 301-596-7821

Massachusetts

ACI
800 West Cummings Park
Woburn, MA 01801
TEL: 617-935-7230
FAX: 617-933-9053

ALL AMERICAN SEMICONDUCTOR
19 Crosby Drive
Bedford, MA 01730
TEL: 617-275-8888
FAX: 617-275-1982

ARROW/SCHWEBER ELECTRONICS
25 Upton Drive
Wilmington, MA 01887
TEL: 508-658-0900
FAX: 508-694-1754

Michigan

ARROW/SCHWEBER ELECTRONICS
19880 Haggerty Rd.
Livonia, MI 48152
TEL: 313-462-2290
FAX: 313-462-2686

Minnesota

ARROW/SCHWEBER ELECTRONICS
10100 Viking Drive, Suite 100
Eden Prairie, MN 55344
TEL: 612-941-5280
FAX: 612-941-9405

ALL AMERICAN SEMICONDUCTOR
7716 Golden Triangle Drive
Eden Prairie, MN 55344
TEL: 612-944-2151
FAX: 612-944-9803

Missouri

ARROW/SCHWEBER ELECTRONICS
2380 Schuetz Road
St. Louis, MO 63146
TEL: 314-567-6888
FAX: 314-567-1164

New Jersey

ACI
12 Furler Street
Totowa, NJ 07512
TEL: 201-812-0507
FAX: 201-812-0709

ARROW/SCHWEBER ELECTRONICS
43 Route 46 East
Pine Brook, NJ 07058
TEL: 201-227-7880
FAX: 201-227-2064

ARROW/SCHWEBER ELECTRONICS
4 East Stow Road, Unit 11
Marlton, NJ 08053
TEL: 609-596-8000
FAX: 609-596-9632

ALL AMERICAN SEMICONDUCTOR
245-D Clifton Avenue
West Berlin, NJ 08091
TEL: 609-768-6767
FAX: 609-768-3649

New York

ACI ELECTRONICS CORP.
200 Newtown Road
Plainview, NY 11803
TEL: 516-293-6630
TEL: 800-645-4955
FAX: 516-293-5192

ALL AMERICAN SEMICONDUCTOR
275B Marcus Boulevard
Hauppauge, NY 11788
TEL: 516-434-9000
FAX: 516-434-9394

ARROW/SCHWEBER ELECTRONICS
20 Oser Avenue
Hauppauge, NY 11788
TEL: 516-231-1000
FAX: 516-231-1072

ARROW/SCHWEBER ELECTRONICS
25 Hub Drive
Melville, NY 11747
TEL: 516-391-1300
FAX: 516-391-1707

ARROW/SCHWEBER ELECTRONICS
3375 Brighton-Henrietta Townline Rd.
Rochester, NY 14623
TEL: 716-427-0300
FAX: 716-427-0735

MAST DISTRIBUTORS
710-2 Union Parkway
Ronkonkoma, NY 11779
TEL: 516-471-4422
FAX: 516-471-2040

ZEUS COMPONENTS, INC.
100 Midland Avenue
Port Chester, NY 10573
TEL: 914-937-7400
FAX: 914-937-2553

North Carolina

ARROW/SCHWEBER ELECTRONICS
5240 Greens Dairy Road
Raleigh, NC 27604
TEL: 919-876-3132
FAX: 919-878-9517

Ohio

ARROW/SCHWEBER ELECTRONICS
8200 Washington Village Dr. #A
Centerville, OH 45458
TEL: 513-435-5563
FAX: 513-435-2049

ARROW/SCHWEBER ELECTRONICS
6573E Cochran Road
Solon, OH 44139
TEL: 216-248-3990
FAX: 216-248-1106

Oklahoma

ARROW/SCHWEBER ELECTRONICS
12111 E. 51st Street, Suite 101
Tulsa, OK 74146
TEL: 918-252-7537
FAX: 918-254-0917

Oregon

ALMAC/ARROW ELECTRONICS
1885 NW 169th Place
Beaverton, OR 97006-7312
TEL: 503-629-8090
FAX: 503-645-0611

ALL AMERICAN SEMICONDUCTOR
1815 NW 169th Place
Suite 6025
Beaverton, OR 97006
TEL: 503-531-3333
FAX: 503-531-3695

Pennsylvania

ARROW/SCHWEBER ELECTRONICS
1000 RIDC Plaza, Suite 212
Pittsburgh, PA 15238
TEL: 412-963-6807
FAX: 412-963-1573

Texas

ALL AMERICAN SEMICONDUCTOR
1819 Firman Drive #127
Richardson, TX 75081
TEL: 214-231-5300
TEL: 800-541-1435
FAX: 214-437-0353

ARROW/SCHWEBER ELECTRONICS
2227 W. Braker Lane
Austin, TX 78758
TEL: 512-835-4180
FAX: 512-832-9875

ARROW/SCHWEBER ELECTRONICS
3220 Commander Drive
Carrollton, TX 75006
TEL: 214-380-6464
FAX: 214-248-7208

ARROW/SCHWEBER ELECTRONICS
10899 Kinghurst Drive
Suite 100
Houston, TX 77099
TEL: 713-530-4700
FAX: 713-568-8518

Utah

ARROW/SCHWEBER ELECTRONICS
1946 W. Parkway Blvd.
Salt Lake City, UT 84119
TEL: 801-973-6913
FAX: 801-972-0200

ALL AMERICAN SEMICONDUCTOR
4455 South 700 East
Suite 301
Salt Lake City, UT 84107
TEL: 801-261-4210
FAX: 801-261-3885

Washington

ALMAC/ARROW ELECTRONICS
14360 SE Eastgate Way
Bellevue, WA 98007
TEL: 206-643-9992
FAX: 206-649-6259

ALMAC/ARROW ELECTRONICS
East 10905 Montgomery
Spokane, WA 99206-6606
TEL: 509-924-9500
FAX: 509-928-6096

Canada

ARROW/CANADA
36 Antares Drive, Unit 100
Nepean, Ontario K2E 7W5
TEL: 613-226-6903
FAX: 613-723-2018

ARROW/CANADA
1093 Meyerside, Unit 2
Mississauga, Ontario L5T 1M4
TEL: 905-670-7769
FAX: 905-670-7781

ARROW/CANADA
1100 St. Regis Boulevard
Dorval, Quebec H9P 2T5
TEL: 514-421-7411
FAX: 514-421-7430

ARROW/CANADA
500 Boulevard St. Jean Baptiste
Suite 280
Quebec, Quebec G2E 5R9
TEL: 418-871-7500
FAX: 418-871-6816

ARROW/CANADA
8544 Baxter Place
Burnaby, British Columbia V5A 4T8
TEL: 604-421-2333
FAX: 604-421-5030

FUTURE ELECTRONICS, INC.
5195 Airport Road, Suite 200
Mississauga, Ontario L4V 1W5
TEL: 905-612-9200
FAX: 416-612-9185

FUTURE ELECTRONICS, INC.
Baxter Center
1050 Baxter Road
Ottawa, Ontario K2C 3P2
TEL: 613-820-8313
FAX: 613-820-3271

FUTURE ELECTRONICS, INC.
237 Hymus Blvd.
Pointe Claire, Quebec
H9R 5C7
TEL: 514-694-7710
TWX: 610-421-3251
Telex: 05-823554
FAX: 514-695-3707

International Representatives & Distributors

Australia

ARLEC HOLDINGS PTY. LTD
Maroondah Highway,
Mooroolbark
Victoria 3138
Australia

Austria

AVNET E2000
Waidhausenstr 19
A - 1140 Vienna, Austria
TEL: + 43 1 911 2847
FAX: + 43 1 911 3853

Belgium

MICROTRON NV
Generaal de Wittelaan 7
2800 Mechelen Belgium
TEL: + 32 15 212223
FAX: + 32 15 210069

Denmark

AVNET NORTEC ELECTRONICS AS
Transformervej 17
2730 Herlev, Denmark
TEL: + 45 44 880800
FAX: + 45 44 880888

Finland

PEREL OY
P.O. Box 230
Torpankatu 28
05801 Hyvinkaa Finland
TEL: + 35 814 87111
FAX: + 35 814 8711500

France

AVNET COMPOSANTS
79 Rue Pierre Semard
92320 Chatillon, France
TEL: + 33 1 4965 2703
FAX: + 33 1 4965 2738

SYSCOM ELECTRONIQUE
Europarc, Parc Activities
Technoloquies
65 Rue Auguste Perret
94042 Creteil Cedex, France
TEL: + 331 4377 8488
FAX: + 33 1 4377 5349

Germany

AVNET E2000
Elektronische Bauelemente
Stahlgruberring 12D - 81829
Munich, Germany
TEL: + 49 89 45 11001
FAX: + 49 89 45 110254
FAX: + 49 89 45 110129

CED DITRONIC MBS
Vetrieb Electronischer
Bauelemente und Systeme
Julius-Hoelder Str.42
D - 70597 Stuttgart, Germany
TEL: + 49 711 720 010
FAX: + 49 711 728 9780
FAX: + 49 711 7200132

CED DITRONIC GMBH
Feldkirchner Str. 12a
85551 Kircheim
Germany
TEL: + 49 899 038 551
FAX: + 49 899 030 944

Hong Kong

SEMICON PRODUCTS & SYSTEMS CO., LTD
Flat 1,2 & 2, 17 Fl., Entrepot
Centre
117 How Ming Street
Hong Kong
TEL: 011-852-2763-7788
FAX: 011-852-2763-6155

Ireland

FMG ELECTRONICS
Norebank House, Greenshill
Kilkenny, Ireland
TEL: + 35 356 64002
FAX: + 35 356 51438

Israel

TELSYS LTD
Atidim Industrial Park, Building
3
Dvora Hanevia St, Neve Sharet
Tel Aviv 61431, Israel
TEL: + 97 23 492 001
FAX: + 97 23 497 407

Italy

EXHIBO SPA
Viale Vitorio Veneto 21
20052 Monza, MI Italy
TEL: + 39 39 208 4111
FAX: + 39 39 736 9035

Japan

TEKSEL CO. LTD
Tbc 2-7-10 Higashi
Shibuya-Ku
Tokyo 150 Japan
TEL: 011-81-3-5467-9000
FAX: 011-81-3-5467-9346

JEPICO CORPORATION
Dai-Chi Seimei Bldg.
Nishi-Shinjuku 2-7-1
Shinjuku-Ku
Tokyo, 163-07 Japan
TEL: 011-81-3-3348-0611
FAX: 011-81-3-3348-0623

ADC CORPORATION
2nd Nagaoka
Bldg 7-17-3 Nishi-Gotanda
Shinagawa-Ku, Tokyo 141 Japan
TEL: 011- 81-3-3492-1251
FAX: 011-81-3-3492-1252

Korea

MAINSAIL MERCANTILE LTD
1-29 Gahoe-Dong, Chongro-Ku
C.P.O. Box 7743
Seoul 110-260, Korea
TEL: 011-82-2-745-2761
FAX: 011-82-2-745-2766

Netherlands

KONING & HARTMAN BV
Energieweg 1
2627 AP Delft, Netherlands
TEL: + 31 15 609578
FAX: + 31 15 619194
FAX: + 31 15 619114

New Zealand

ELECTRONIC COMMUNICATIONS SOLUTIONS LIMITED ECS (FORMERLY LEATHAM)
59 Marsden Street
Po Box 31306
Lower Hutt, New Zealand
TEL: 011-64-4-587-0220
FAX: 011-64-4-587-0219

Norway

AVNET NORTEC ELECTRONICS AS
Smedsvingen 4, PO Box 123
N - 1364 Hvalstad, Norway
TEL: + 47 66 846210
FAX: + 47 66 846545

Singapore

SERIAL SYSTEMS
11 Jalan Mesin #06-00
Standard Industrial Building
Singapore 1336
TEL: 011-65-2800-200
FAX: 011-65- 286-1812/6723

South Africa

ELECTRONIC BUILDING ELEMENTS EBE-LTD
PO Box 912 1222
Silverton 0127, South Africa
TEL: + 27 12 803 7680
FAX: + 27 12 803 8294

Spain

MONOLITIC S.A.
Avda. Hospital Militar, 78-80
08023 Barcelona, Spain
TEL: + 34 3 219 40 16
FAX: + 34 3 284 11 93

Sweden

KELTECH COMPONENTS AB (FORMERLY LAGER-CRANTZ)
Box 505 Kemistvagen 10A
S - 18324 Taby, Sweden
TEL: + 46 8 6308590
FAX: + 46 8 7562143

Switzerland

AVNET E2000
Boehnirainstr.11, CH - 8801
Thalwil, Switzerland
TEL: + 41 1 722 1330
FAX: + 41 1 722 1340

ESE ELEKTRONIK
Im Stetterfeld 1
CH-5608 Stetten
Switzerland
TEL: + 41 56 95 23 77
FAX: + 41 56 95 15 78

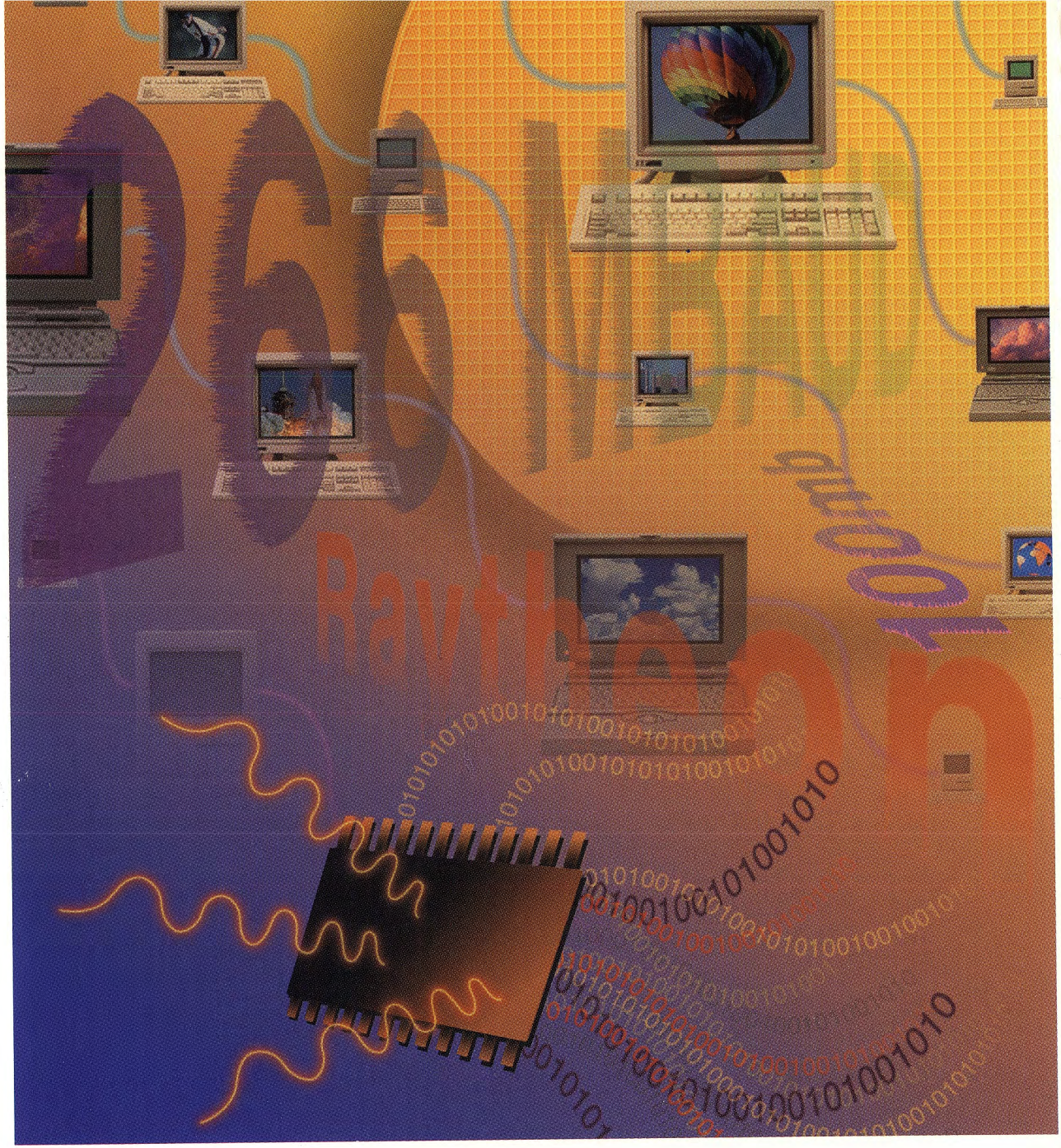
Taiwan

SEA UNION ENGINEERING ENTERPRISES LTD
3rd Fl., Hua-Nan
Building No. 162
Chang An East Road
2nd Section
Taipei, Taiwan R.O.C.
TEL: 011-886-2-7516856
FAX: 011-886-2-7516958/
7512062

United Kingdom

AMBAR COMPONENTS
17 Thame Park Road, Thame
Oxfordshire, OX9 3XD, UK
TEL: + 44 1844 261144
FAX: + 44 1844 261789

MICROELECTRONICS TECHNOLOGY LTD (METL)
Countax House
Haseley Trading Estate
Great Haseley, Oxfordshire
OX9 7PF, UK
TEL: + 44 844 278781
FAX: + 44 844 278746



Mountain View Facility
350 Ellis Street
Mountain View, CA 94043
Phone: 415 968 9211
Fax: 415 966 7742

San Diego Facility
5580 Morehouse Drive
San Diego, CA 92121
Phone: 619 457 1000
Fax: 619 455 6314
800 722 7074
Applications@lj.sd.ray.com

01/96 10M
Stock # DB 00000196